TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT

TC51V16160CJS/CFTS-60

SILICON GATE CMOS

TENTATIVE DATA

1,048,576 WORD × 16 BIT FAST PAGE DYNAMIC RAM

DESCRIPTION

The TC51V16160CJS/CFTS is the fast page dynamic RAM organized 1,048,576 words by 16 bits. The TC51V16160CJS/CFTS utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC51V16160CJS/CFTS to be packaged in 42 pin plastic SOJ and 50/44 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 3.3V±0.3V tolerance, direct interfacing capability with high performance logic families such as LVTTL.

FEATURES

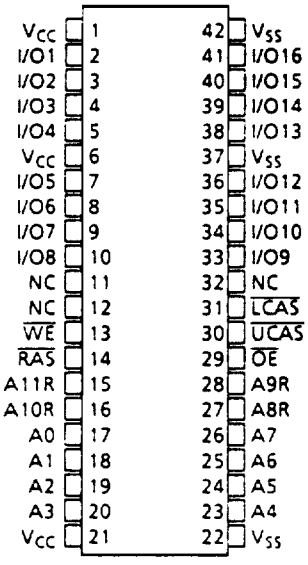
- 1,048,576 word by 16 bit organization
- Fast access time and cycle time

		TC51V16160CJS/CFTS
		-60
t_{RAC}	$\overline{RAS}$ Access Time	60ns
t_{AA}	Column Address Access Time	30ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns
t_{RC}	Cycle Time	110ns
t_{PC}	Fast Page Mode Cycle Time	40ns

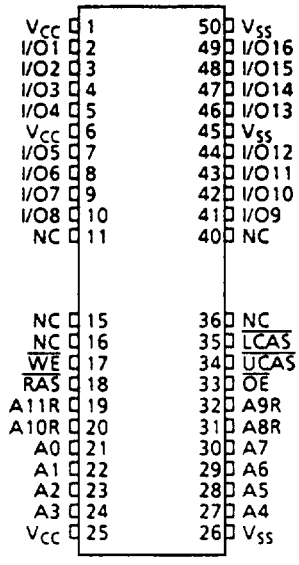
- Single power supply of 3.3V±0.3V with a built-in V_{BB} generator
- Low Power
  360mW MAX. Operating
  (TC51V16160CJS/CFTS-60)
  0.72mV MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Fast Page Mode capability
- 4096 refresh cycles/64ms
- Package TC51V16160CJS : SOJ42-P-400
  TC51V16160CFTS : TSOP50-P-400

PIN CONNECTION (TOP VIEW)

Plastic SOJ



Plastic TSOP

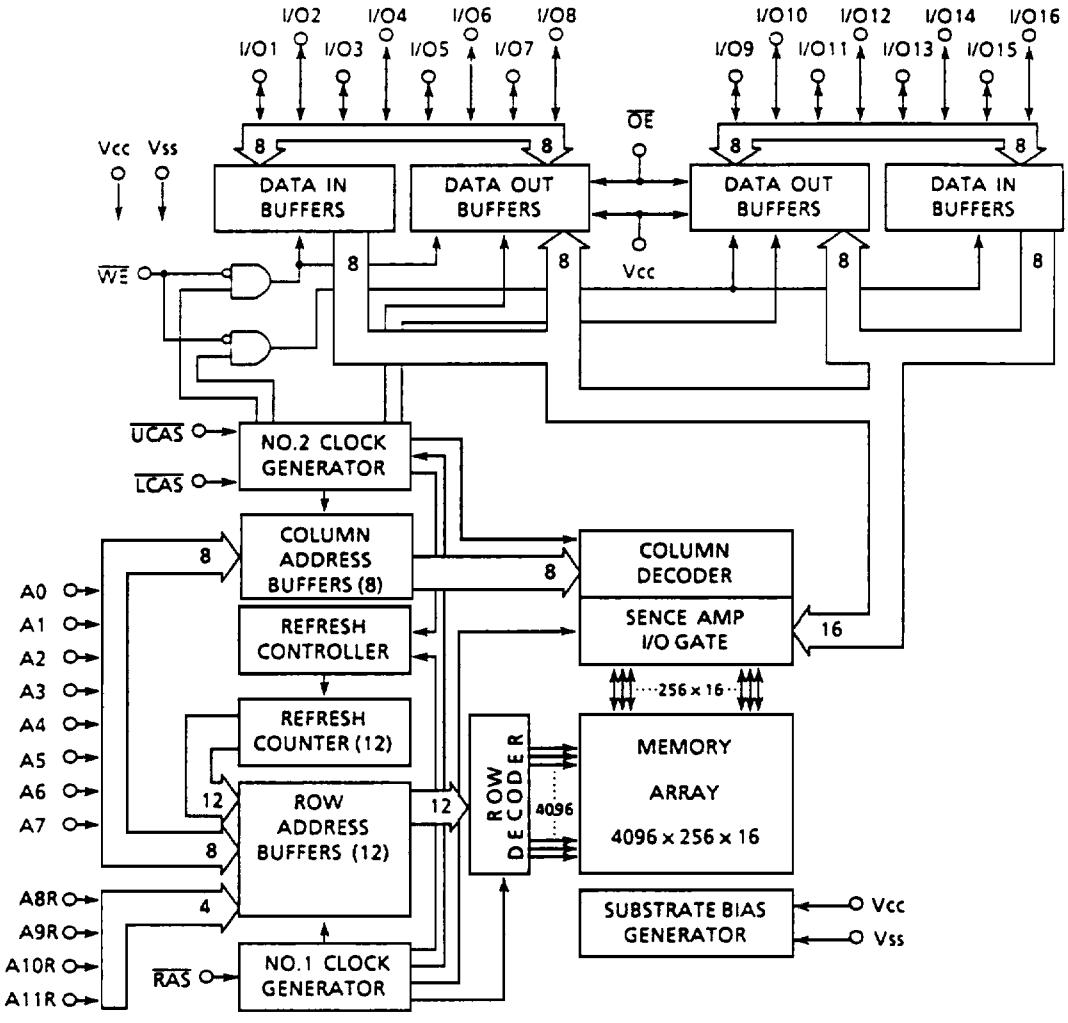


PIN NAMES

A0~A11	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe / Upper Byte Control
$\overline{LCAS}$	Column Address Strobe / Lower Byte Control
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O1~I/O16	Data Input/Output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
N.C.	No Connection

TOSHS076

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−0.3~Vcc+0.3	V	1
Output Voltage	V_{OUT}	−0.3~Vcc+0.3	V	1
Power Supply Voltage	V_{CC}	−0.3~4.6	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature (10s)	T_{SOLDER}	260	°C	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	2
V_{IH}	Input High Voltage	2.2	−	V_{CC}+0.3*	V	2
V_{IL}	Input Low Voltage	−0.3**	−	0.8	V	2

* Vcc + 1.2V at pulse width ≦ 20ns. (pulse width is measured at Vcc)

** -1.2V at pulse width ≦ 20ns. (pulse width is measured at Vss)

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	TC51V16160CJS/CFTS-60	–	100	mA	3, 4, 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{UCAS} = \overline{LCAS} = V_{IH}$)		–	1	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{UCAS} = \overline{LCAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	TC51V16160CJS/CFTS-60	–	100	mA	3, 5
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{UCAS}$, $\overline{LCAS}$, Address Cycling: $t_{PC} = t_{PC}$ MIN.)	TC51V16160CJS/CFTS-60	–	105	mA	3, 4, 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{UCAS} = \overline{LCAS} = V_{CC} - 0.2V$)		–	200	μA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	TC51V16160CJS/CFTS-60	–	100	mA	3, 5
I_{CC7}	BATTERY BACK UP CURRENT Average Power Supply Current, Battery back up Mode ($\overline{RAS}$ Cycling, $\overline{UCAS}$ or $\overline{LCAS} = \overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$, $\overline{WE}$, A0~A11 = V_{CC} – 0.2V or 0.2V, I/O1~I/O16 = V_{CC} – 0.2V, 0.2V or Hi-Z: t_{RC} = 15.6μs $t_{RAS} = t_{RAS}$ MIN~300ns)		–	800	μA	3, 6
I_{CC8}	SELF REFRESH CURRENT Average Power Supply Current, Self Refresh Mode ($\overline{RAS} = \overline{UCAS} = \overline{LCAS} = V_{IL}$, $\overline{OE}$, $\overline{WE}$, A0~A11 = V_{CC} – 0.2V or 0.2V, I/O1~I/O16 = V_{CC} – 0.2V, 0.2V or Hi-Z)		–	400	μA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ V_{CC}, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ V_{CC})		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 2mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 3.3V ± 0.3V, Ta = 0~70°c) (Notes 7, 8, 9)

SYMBOL	PARAMETER	TC51V16160CJS/CFTS -60 MIN.	TC51V16160CJS/CFTS -60 MAX.	UNIT	NOTE
t_{RC}	Rancom Read or Write Cycle Time	110	–	ns	
t_{RMW}	Reac-Modify-Write Cycle Time	172	–	ns	
t_{PC}	Fast Page Mode Cycle Time	40	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	80	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	ns	10,15,16
t_{CAC}	Access Time from $\overline{CAS}$	–	15	ns	10,15
t_{AA}	Access Time from Column Address	–	30	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	ns	10
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	ns	11
t_T	Transition Time (Rise and Fall)	3	50	ns	9
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	15	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	ns	
t_{CAH}	Column Address Hold Time	10	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	ns	12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	ns	12

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Continued)

SYMBOL	PARAMETER	TC51V16160CJS/CFTS -60 MIN.	TC51V16160CJS/CFTS -60 MAX.	UNIT	NOTE
t_{WCH}	Write Command Hold Time	10	–	ns	
t_{WP}	Write Command Pulse Width	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	10	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	10	–	ns	
t_{DS}	Data Set-Up Time	0	–	ns	13
t_{DH}	Data Hold Time	10	–	ns	13
t_{REF}	Refresh Period	–	64	ms	
t_{WCS}	Write Command Set-Up Time	0	–	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	40	–	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	85	–	ns	14
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	55	–	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	60	–	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	20	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	15	ns	10
t_{OED}	$\overline{OE}$ to Data Delay	15	–	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	15	ns	11
t_{OEH}	$\overline{OE}$ Command Hold Time	10	–	ns	
t_{ODS}	Output Disable Set-Up Time	0	–	ns	
t_{RASS}	$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	100	–	μs	
t_{RPS}	$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	110	–	ns	
t_{CHS}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	-50	–	ns	

CAPACITANCE (V_{CC} = 3.3V ± 0.3V, f = 1MHz, Ta = 0~70°c)

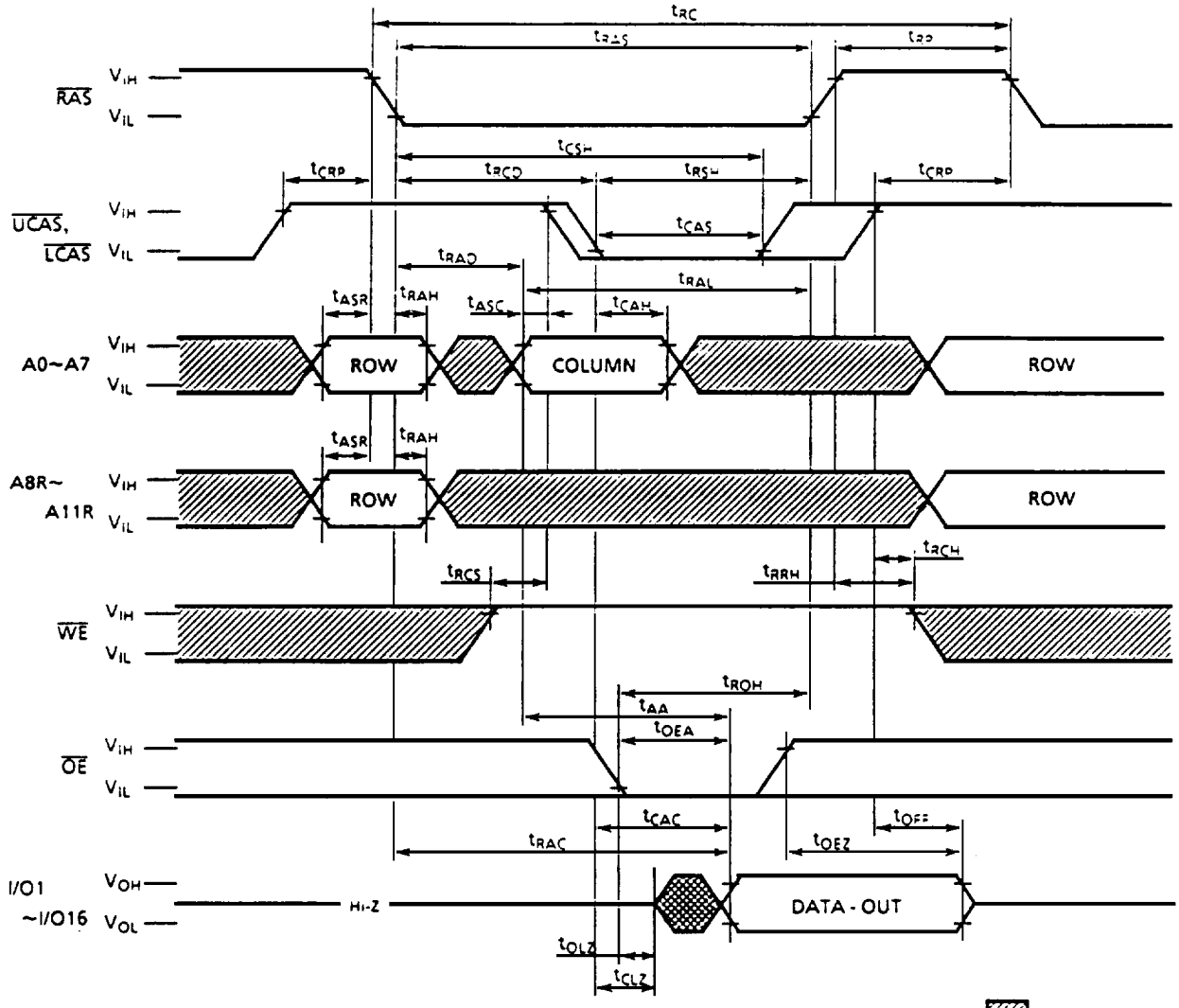
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A11)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (I/O1~I/O16)	–	7	pF

NOTES:

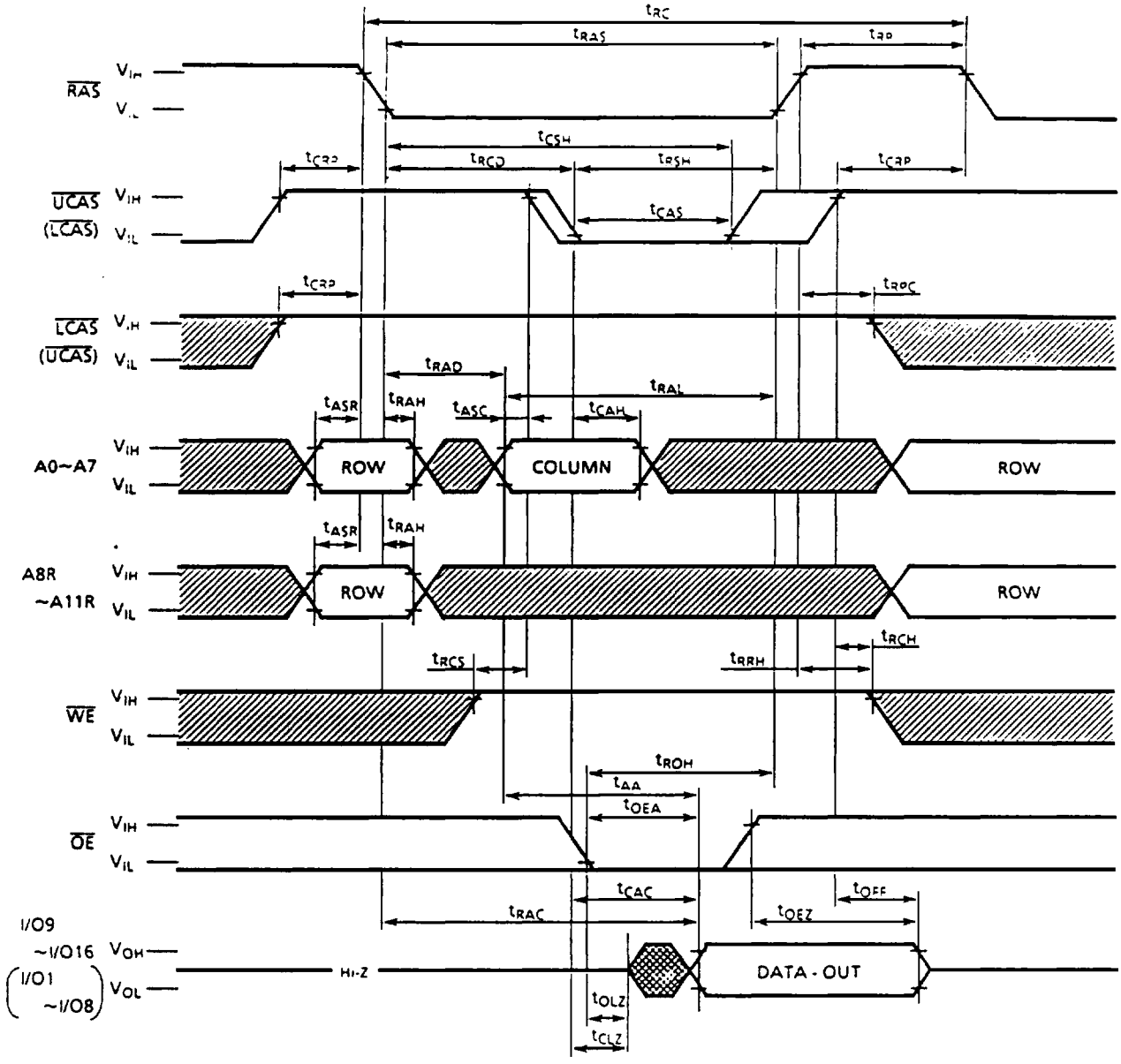
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Address can be changed once or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (tPC).
6. t_{RAS} (max.) = 300ns is only applied to refresh battery back up. t_{RAS} (max.) = 10μs is applied to functional operating.
7. An initial pause of 500μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
8. AC measurements assume $t_T=5$ns.
9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
10. Measured with a load equivalent to 100pF and at $V_{OH}=2.0V$ ($I_{OUT}=-2mA$), $V_{OL}=0.8V$ ($I_{OUT}=2mA$).
11. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{UCAS}$ or $\overline{LCAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING DIAGRAMS

READ CYCLE



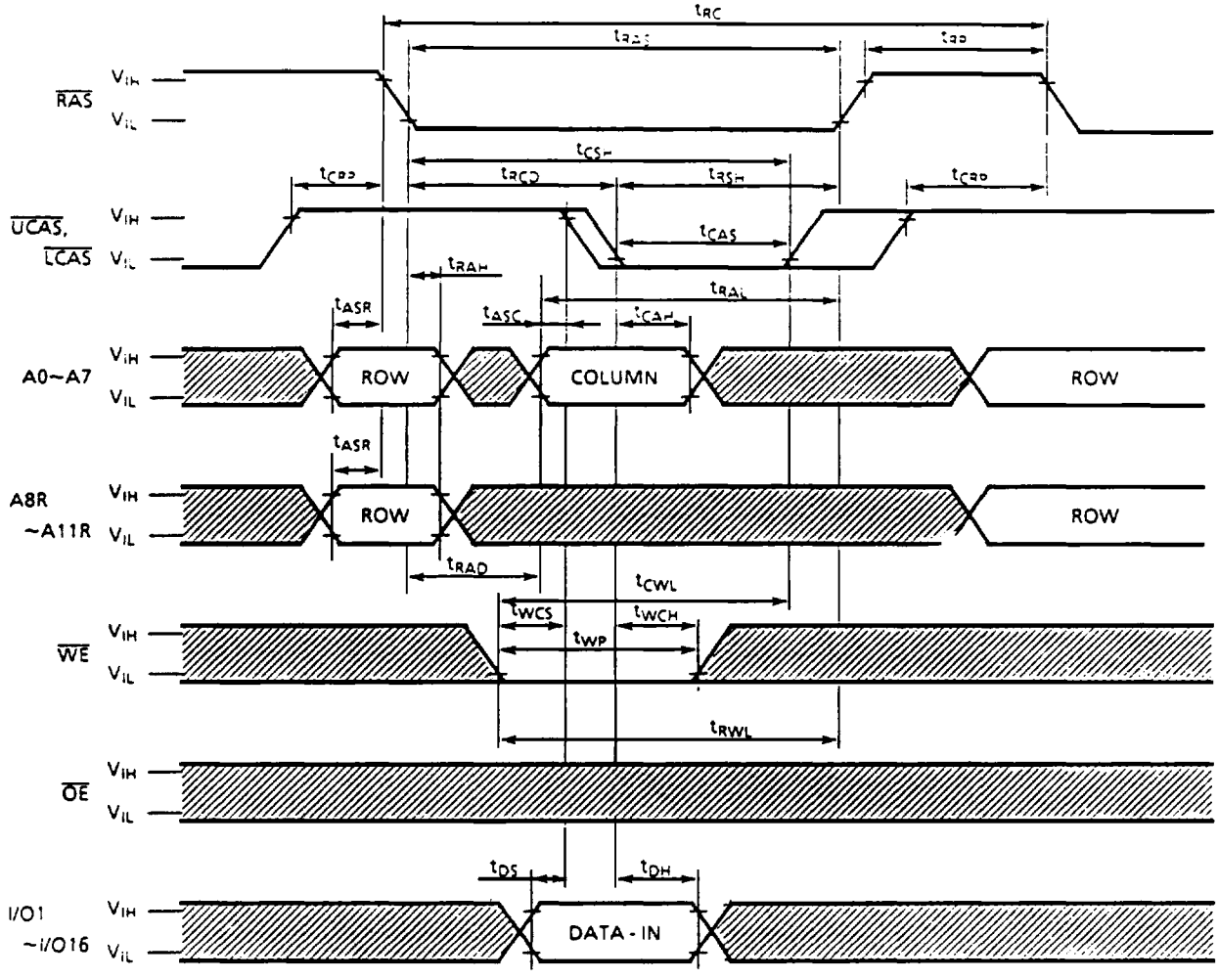
BYTE READ CYCLE



Note : D_{IN} (I/O1~I/O8) = Don't Care
D_{IN} (I/O9~I/O16) = Hi-Z
D_{OUT} (I/O1~I/O8) = Hi-Z
(D_{IN} (I/O9~I/O16) = Don't Care
D_{IN} (I/O1~I/O8) = Hi-Z
D_{OUT} (I/O9~I/O16) = Hi-Z)

: "H" or "L"
: Invalid Data

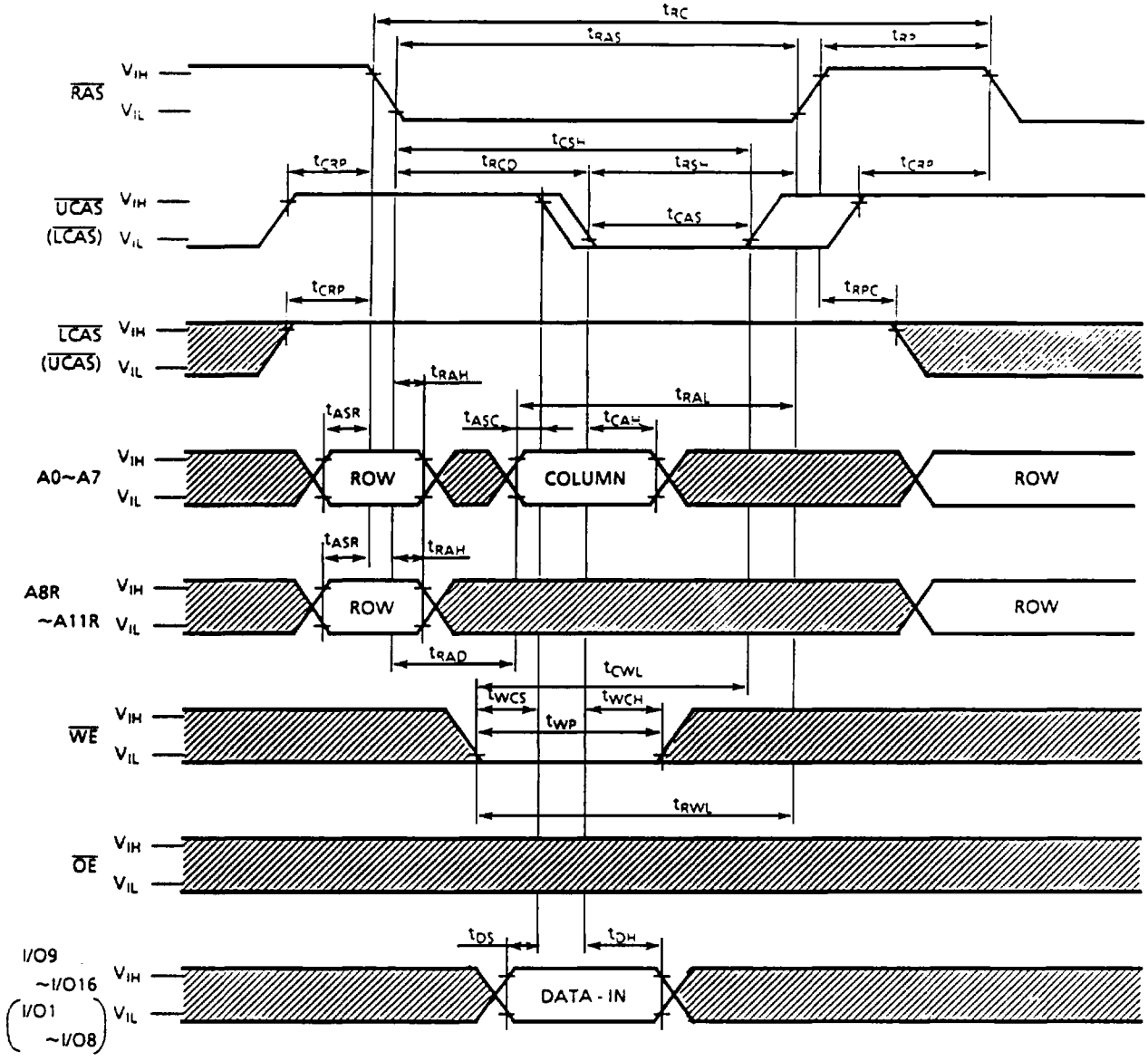
WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = Hi-Z

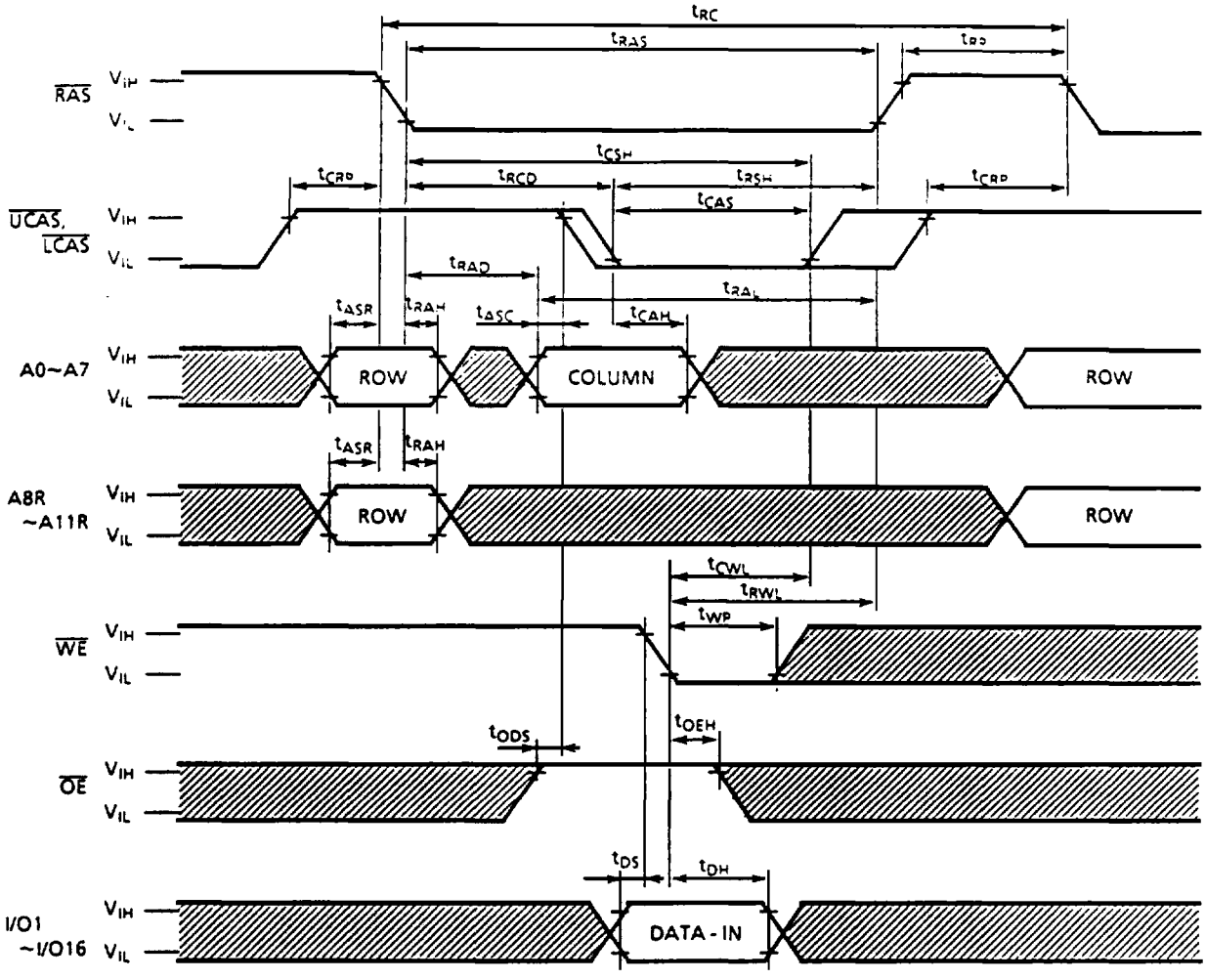
▨ : "H" or "L"

BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{IN} (I/O1~I/O8) = Don't Care
(D_{IN} (I/O9~I/O16) = Don't Care)
D_{OUT} = Hi-Z

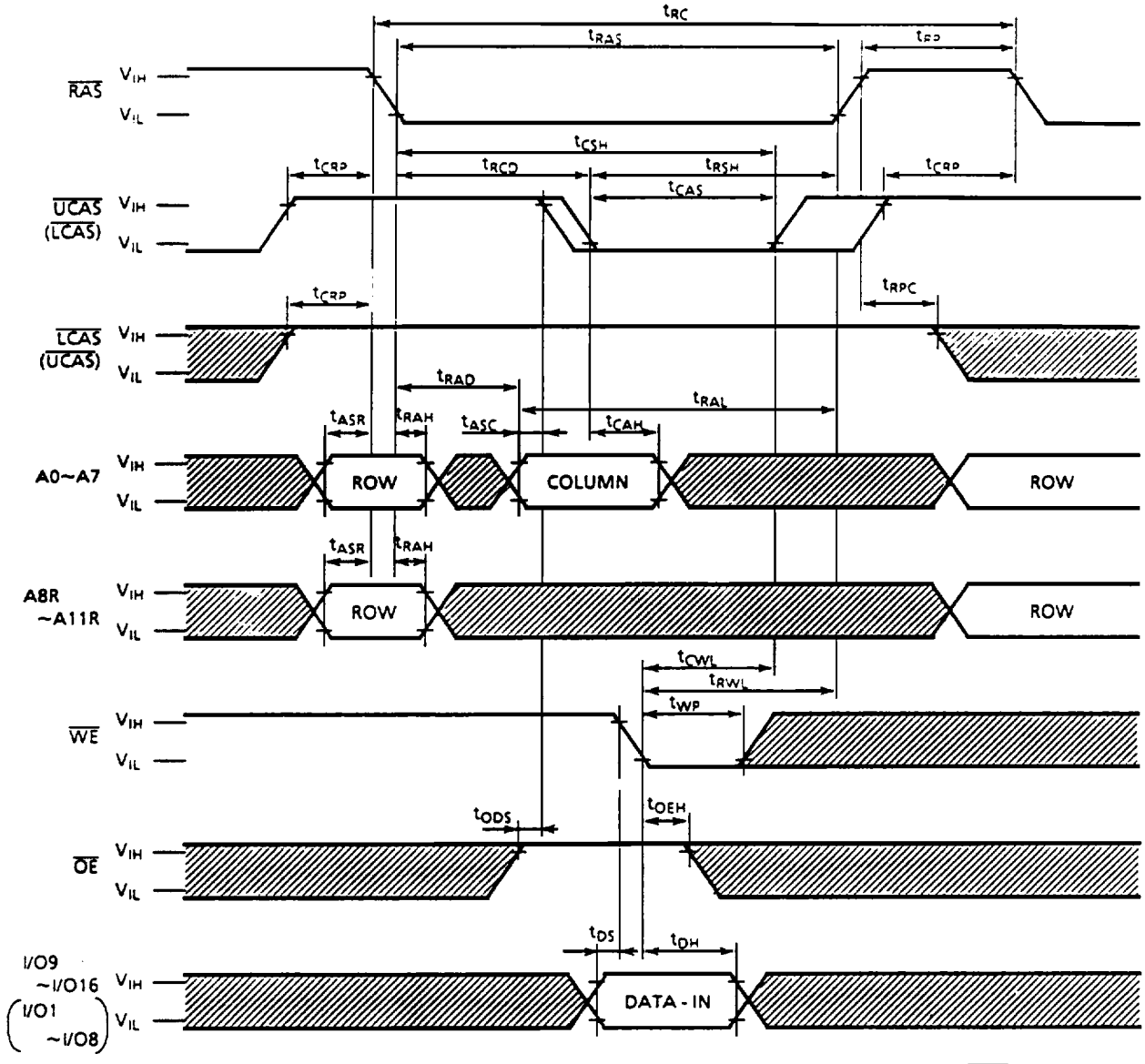
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{OUT} = Hi-Z

▨ : "H" or "L"

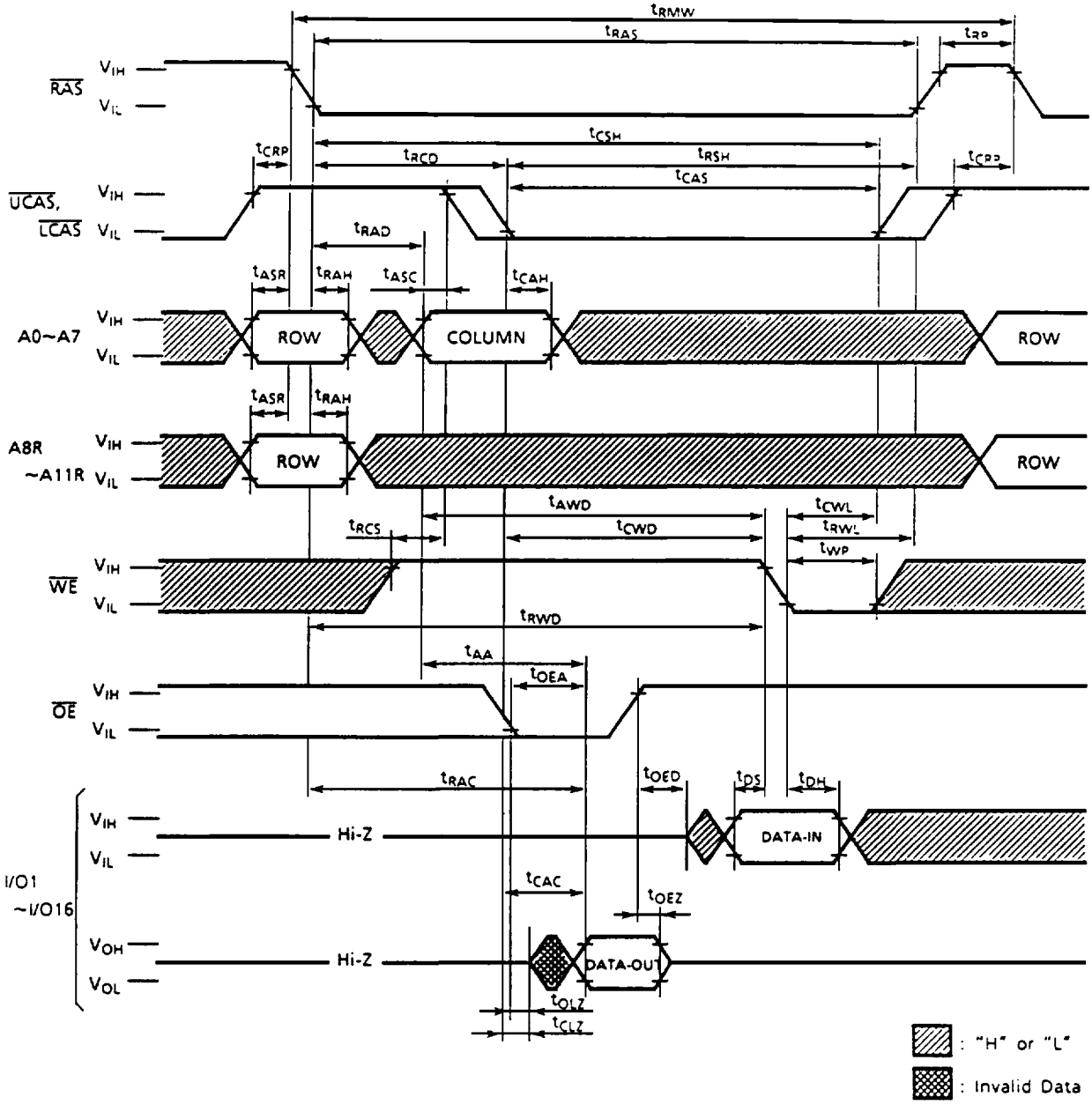
BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



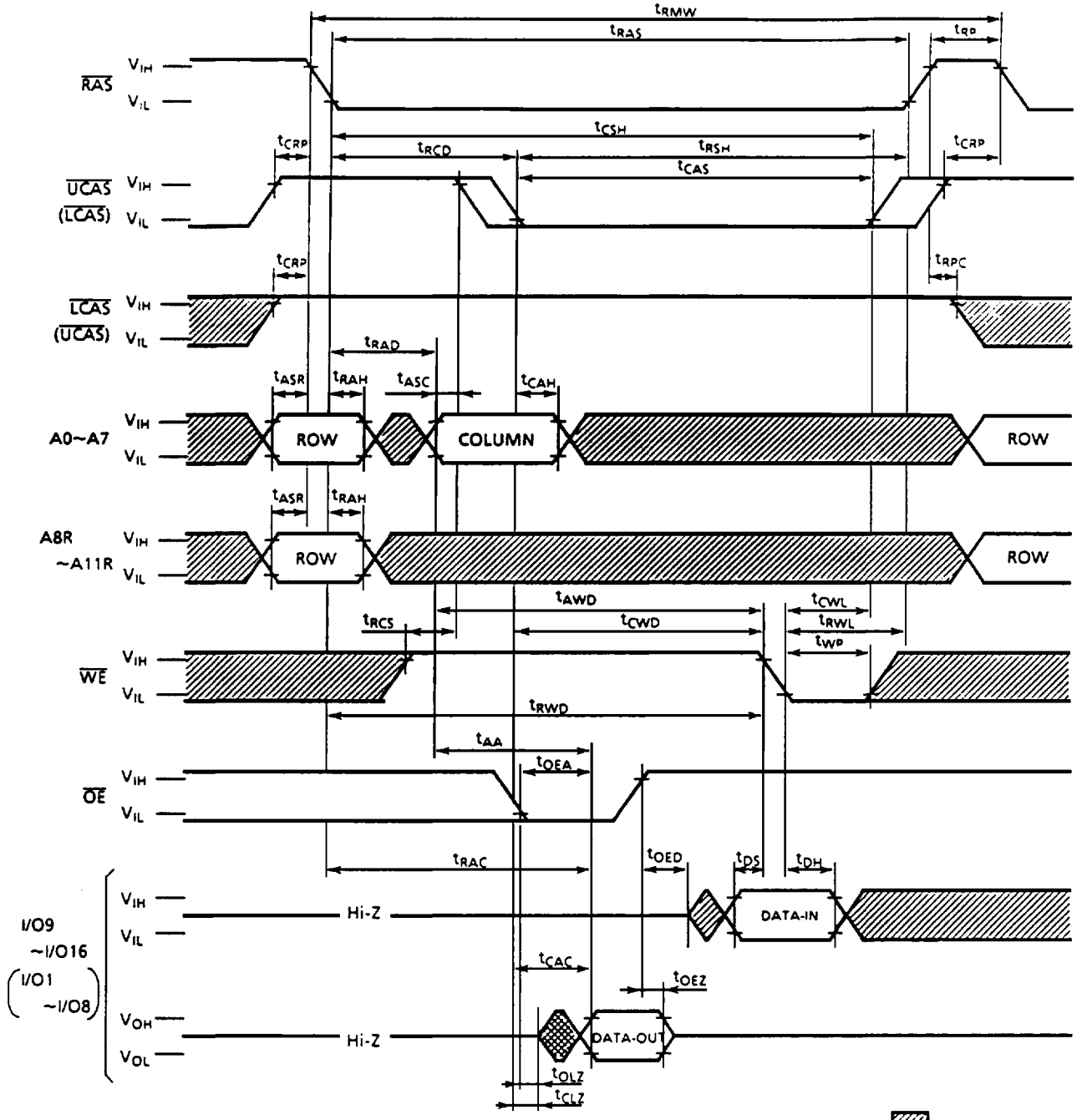
: "H" or "L"

Note: D_{IN} (I/O1~I/O8) = Don't Care
(D_{IN} (I/O9~I/O16) = Don't Care)
D_{OUT} = Hi-Z

READ-MODIFY-WRITE CYCLE



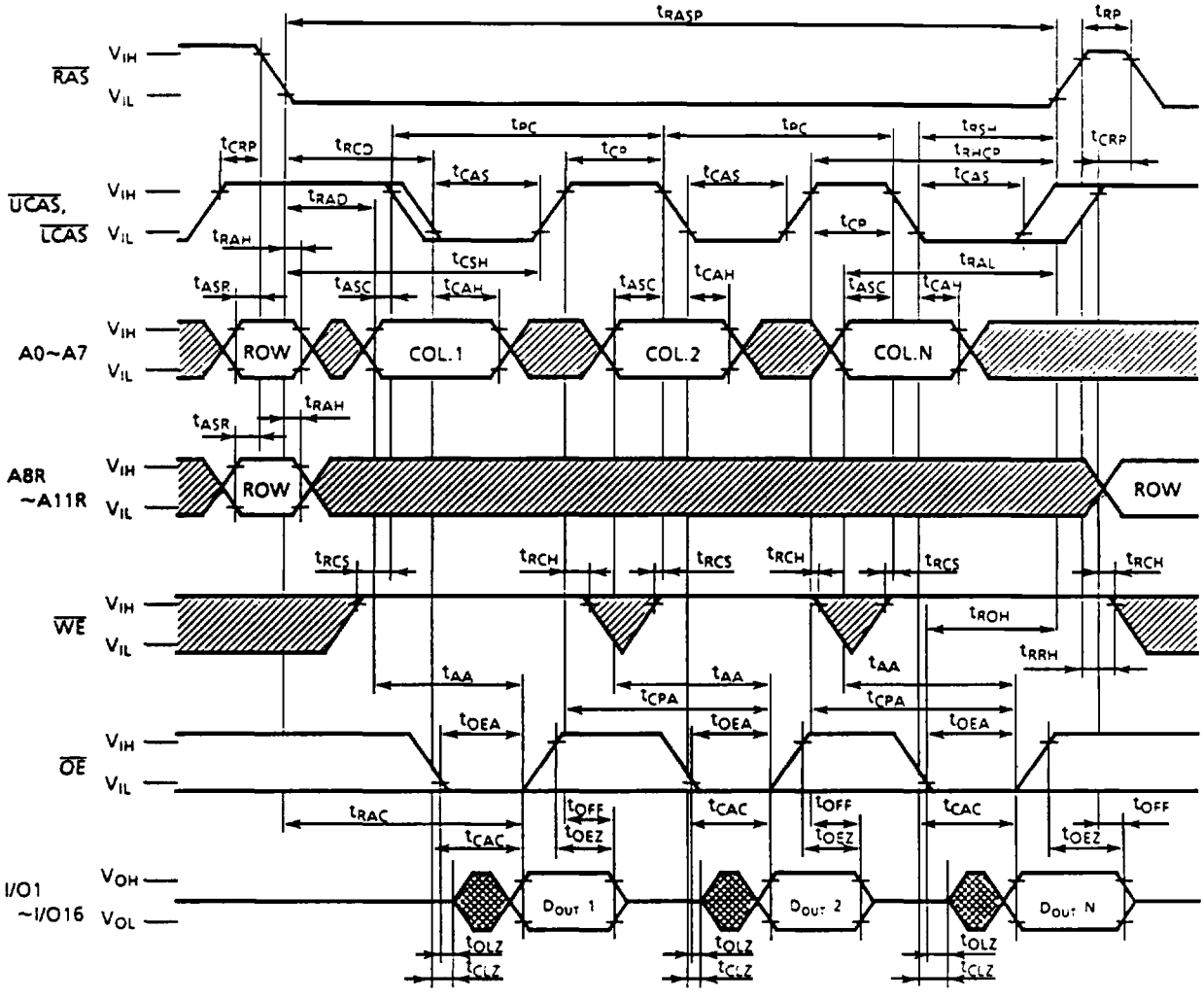
BYTE READ-MODIFY-WRITE CYCLE



Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{OUT} (I/O1~I/O8) = Hi-Z
(D_{IN} (I/O9~I/O16) = Don't Care
D_{OUT} (I/O9~I/O16) = Hi-Z)

: "H" or "L"
: Invalid Data

FAST PAGE MODE READ CYCLE

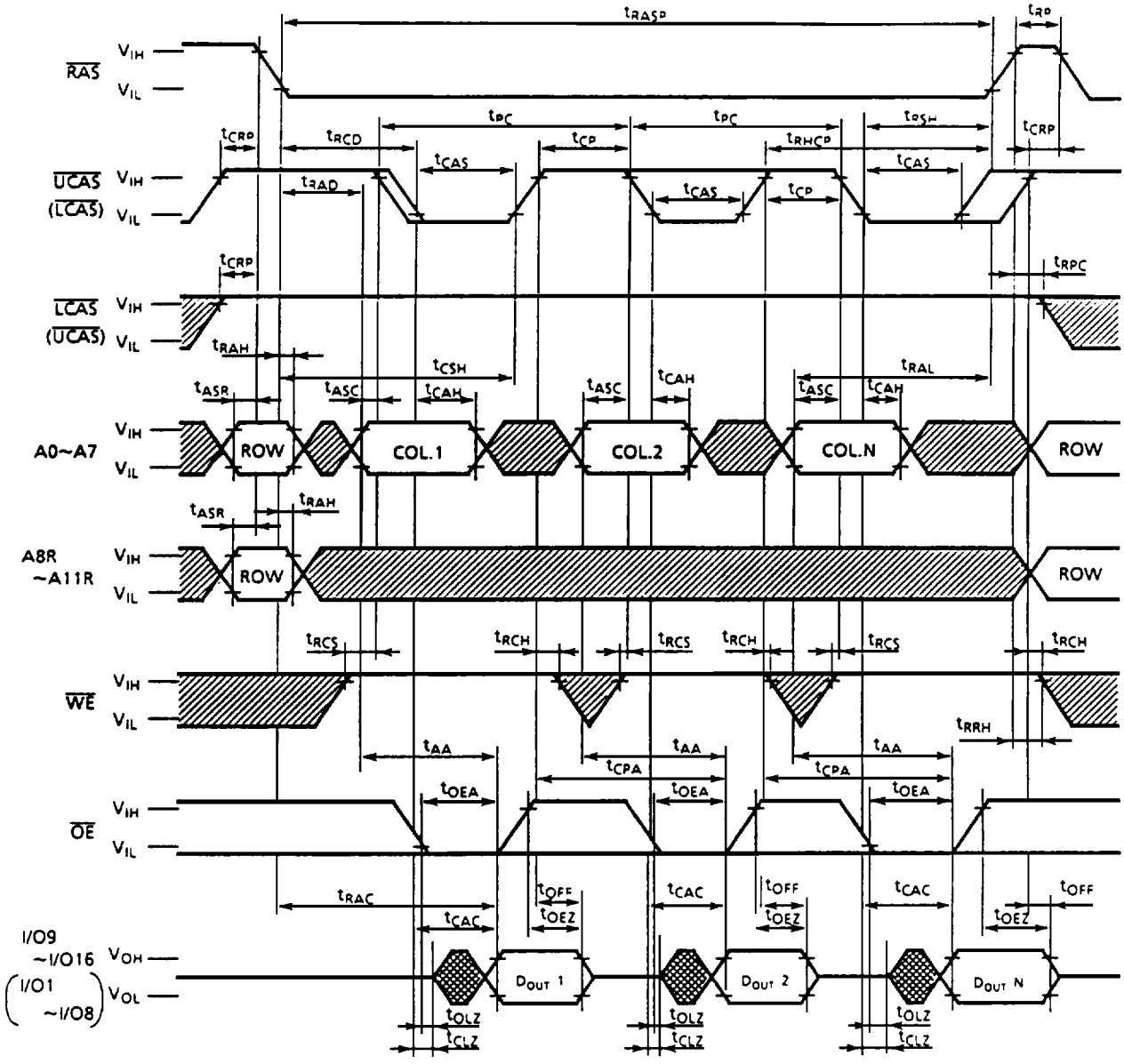


Note: D_{IN} = Hi-Z

: "H" or "L"

: Invalid Data

FAST PAGE MODE BYTE READ CYCLE

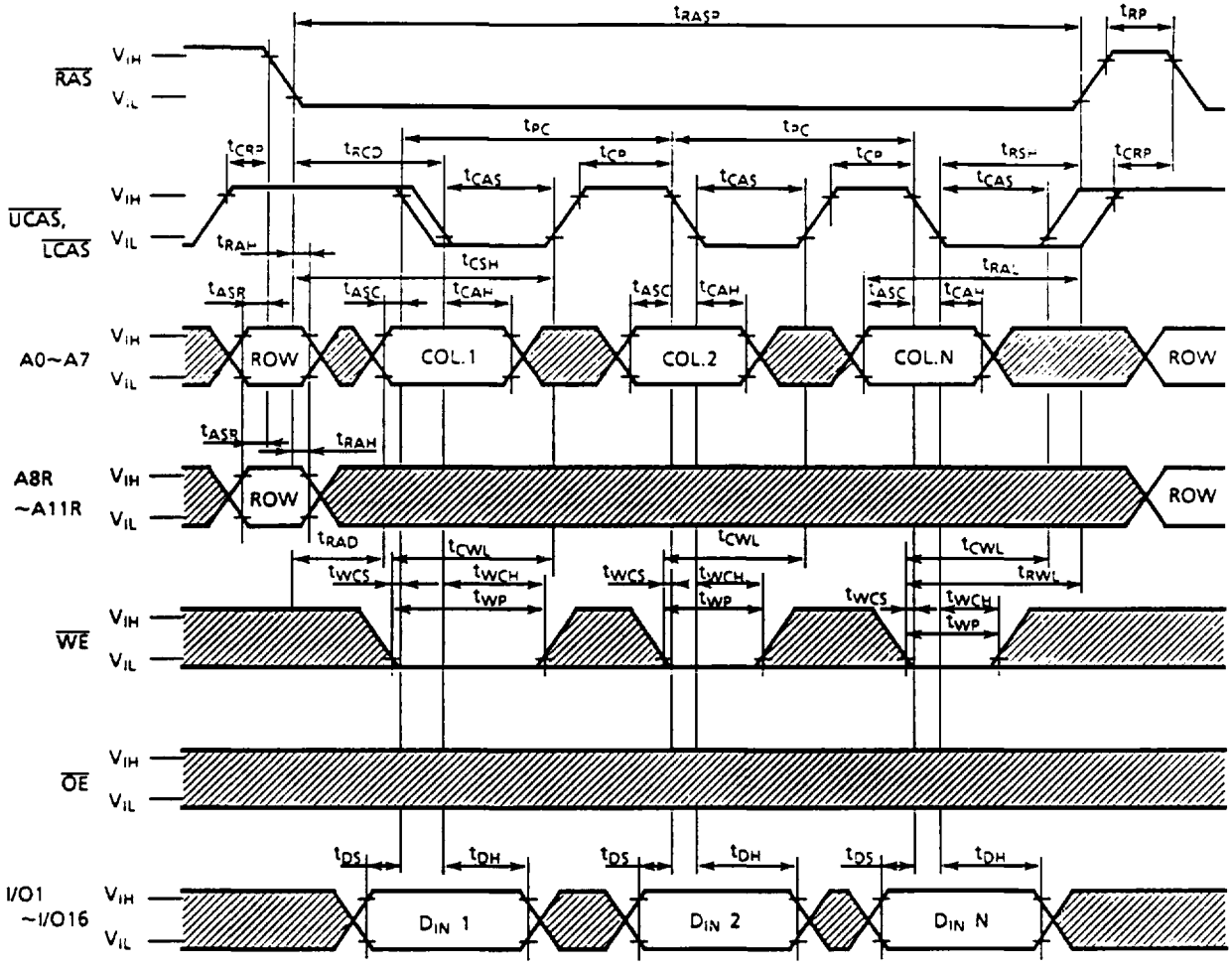


Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{OUT} (I/O1~I/O8) = Hi-Z
(D_{IN} (I/O9~I/O16) = Don't Care
D_{OUT} (I/O9~I/O16) = Hi-Z)

: "H" or "L"

: Invalid Data

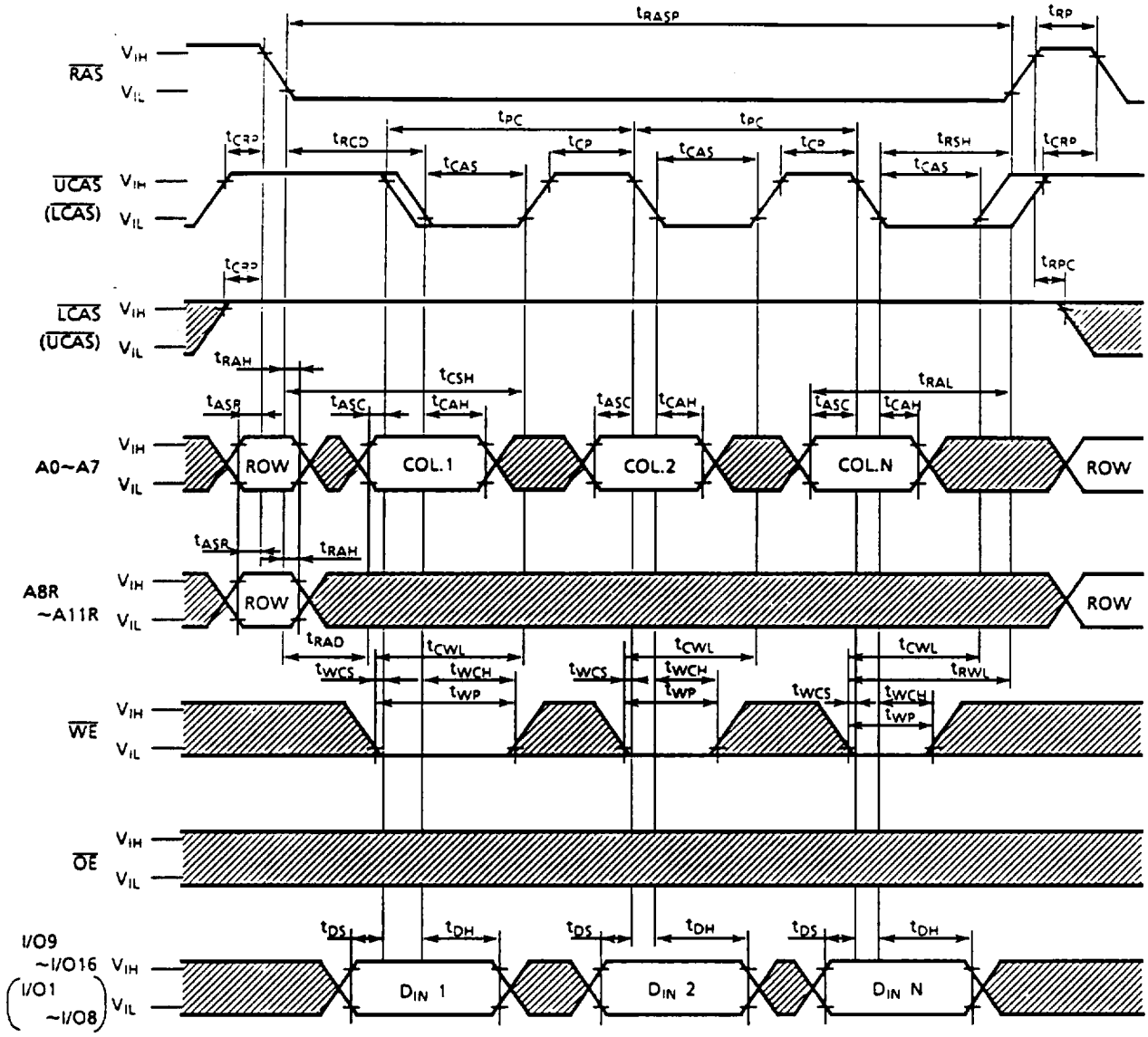
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = Hi-Z

▨ : "H" or "L"

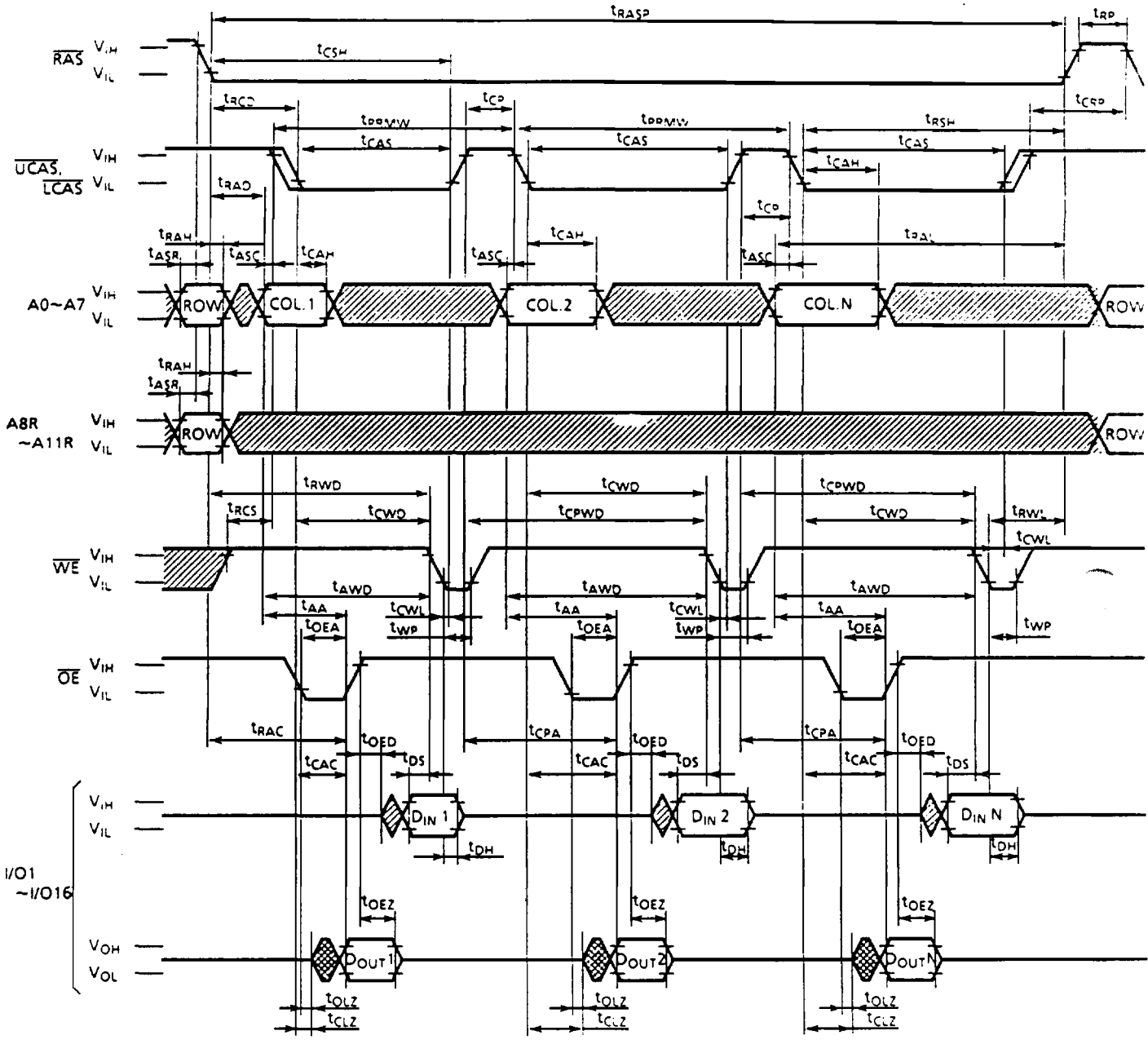
FAST PAGE MODE BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{IN} (I/O1~I/O8) = Don't Care
(D_{IN} (I/O9~I/O16) = Don't Care)
D_{OUT} = Hi-Z

▨ : "H" or "L"

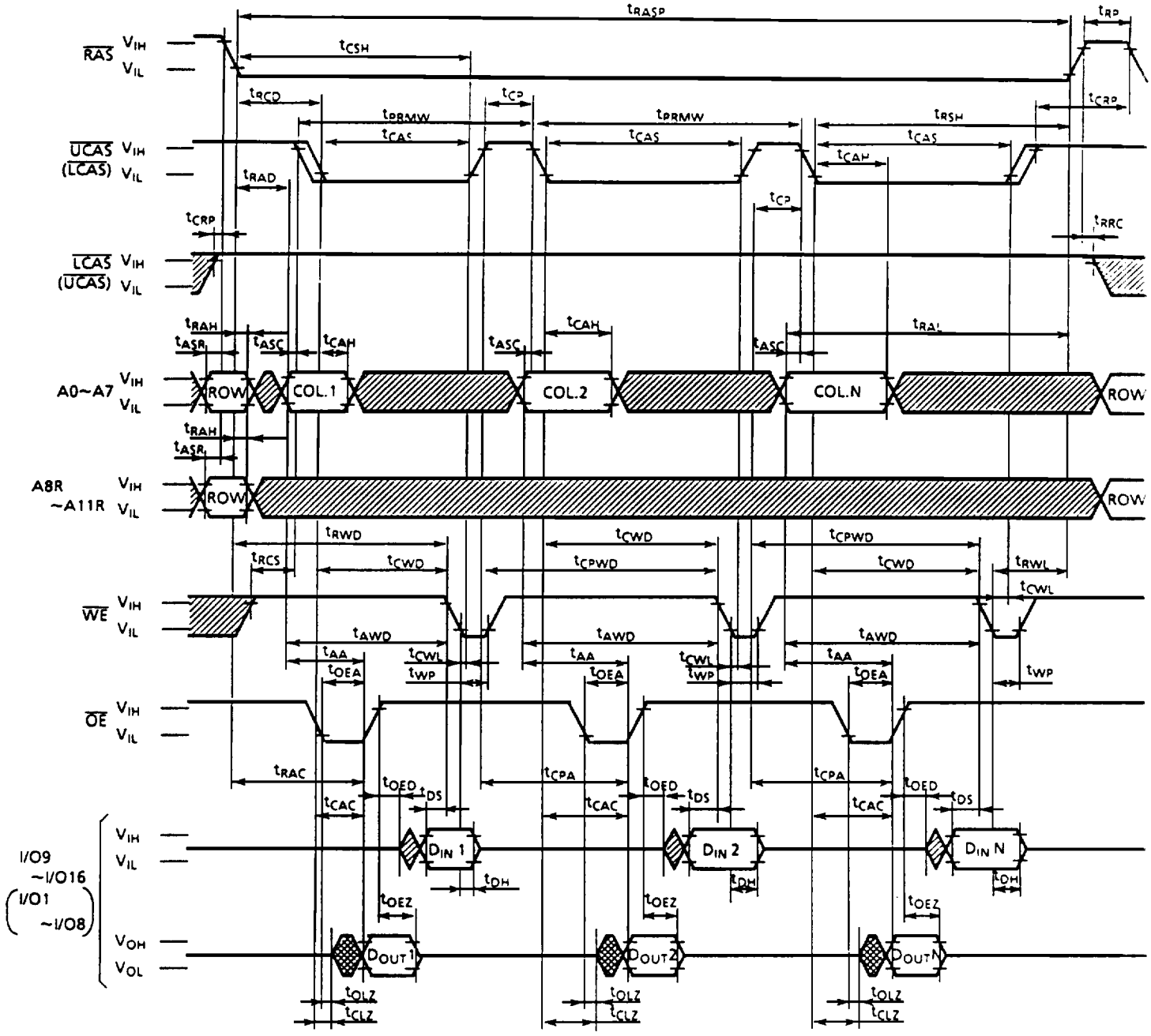
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



: "H" or "L"

: Invalid Data

FAST PAGE MODE BYTE READ-MODIFY-WRITE CYCLE

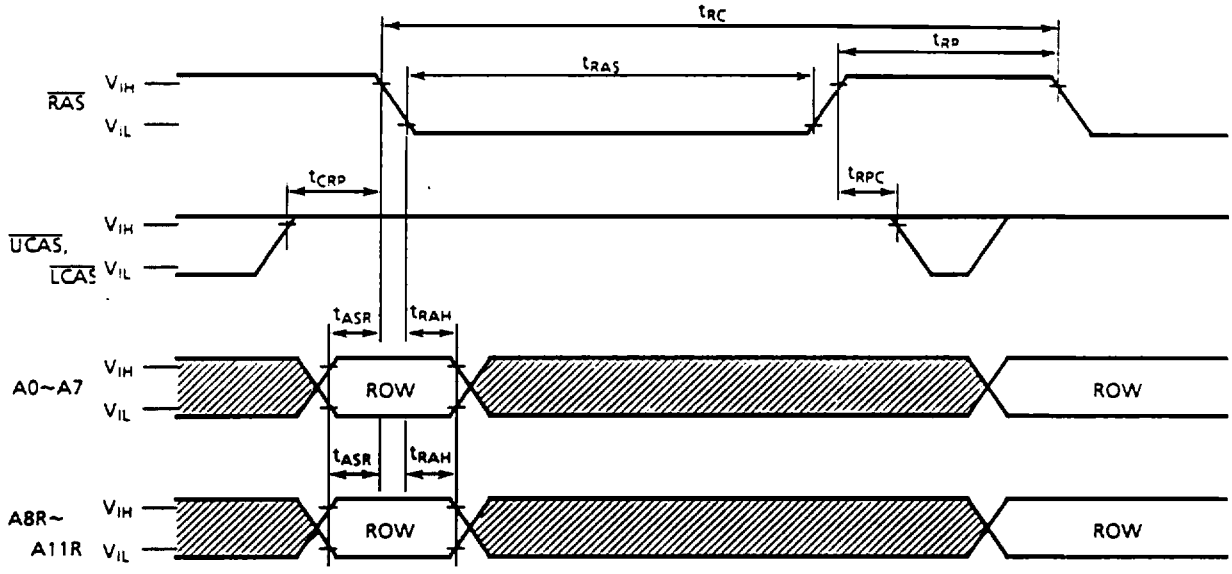


Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{OUT} (I/O1~I/O8) = Hi-Z
(D_{IN} (I/O9~I/O16) = Don't Care
D_{OUT} (I/O9~I/O16) = Hi-Z)

: "H" or "L"

: Invalid Data

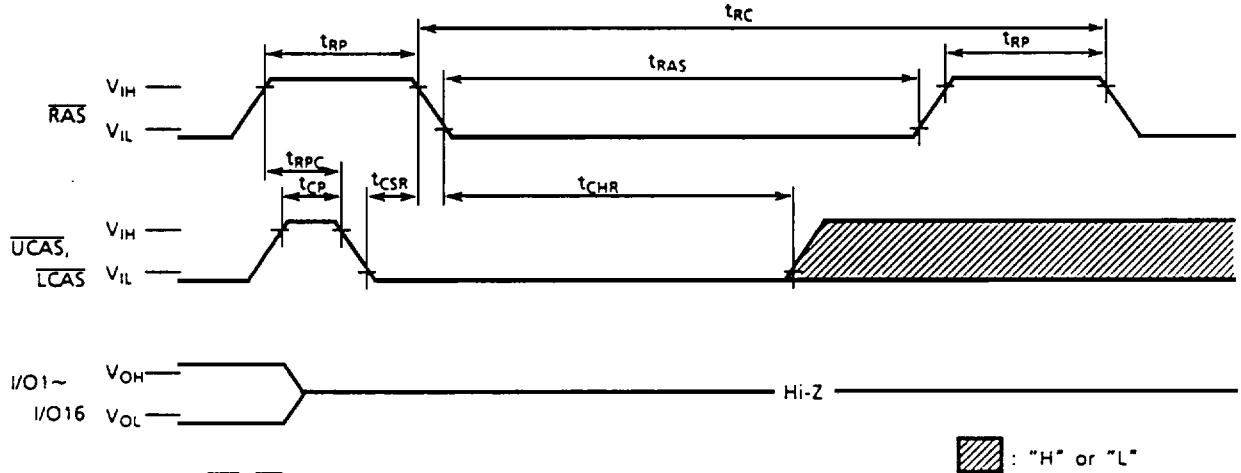
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$ = "H" or "L"
D_{IN} = "H" or "L"

▨ : "H" or "L"

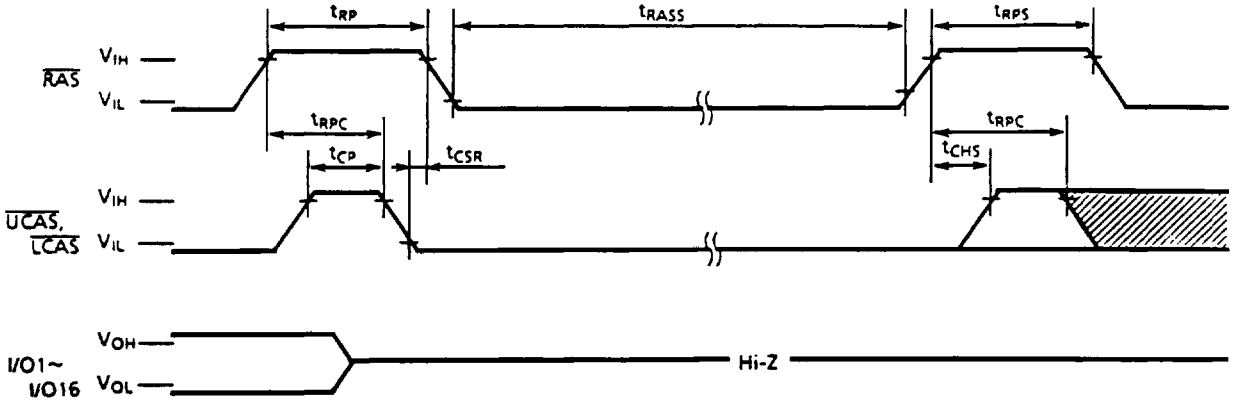
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



▨ : "H" or "L"

Note: $\overline{WE}$, $\overline{OE}$, A0~A7, A8R~A11R = "H" or "L"
D_{IN} = "H" or "L"

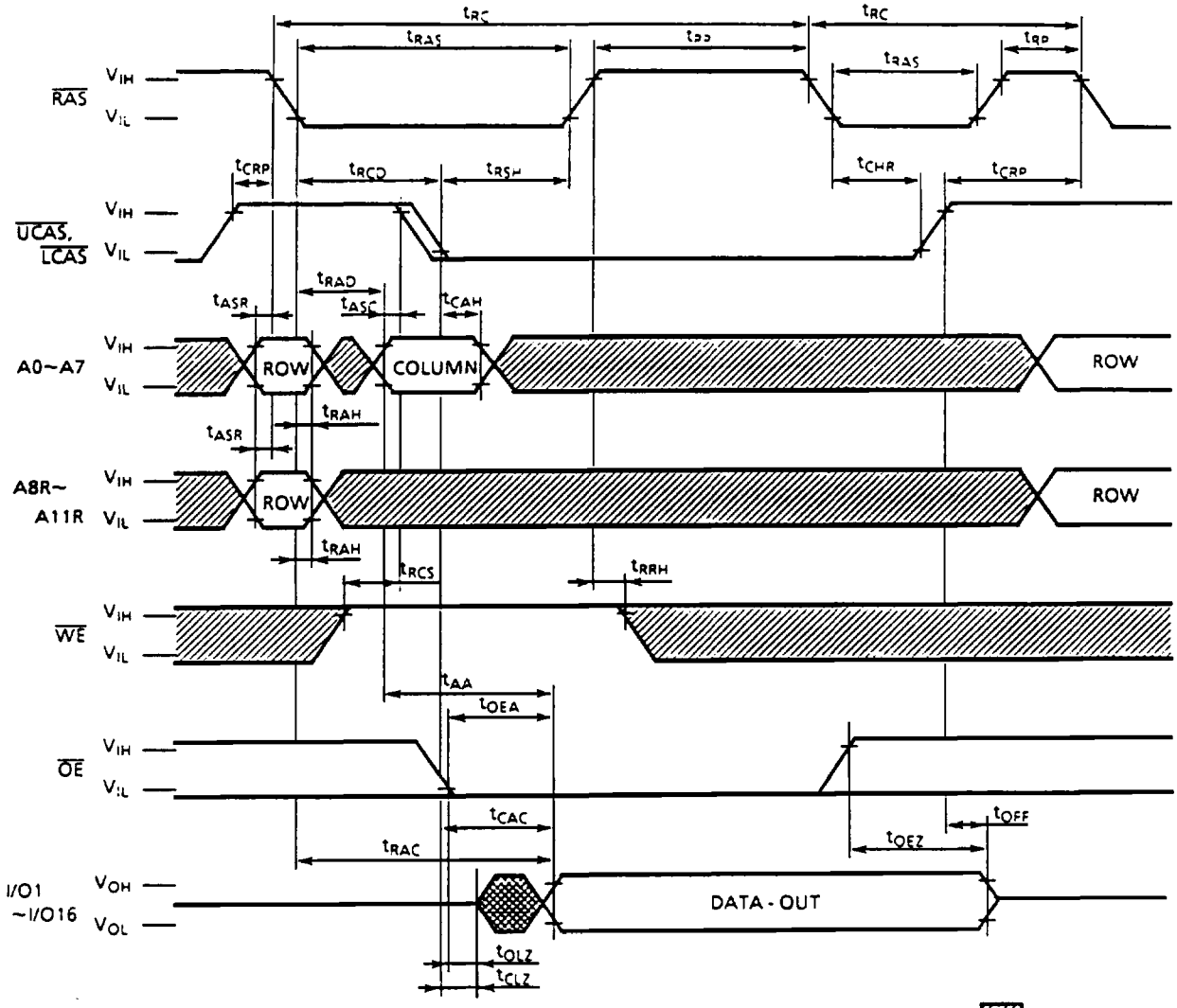
$\overline{CAS}$ BEFORE $\overline{RAS}$ SELF REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$, A0~A11 = "H" or "L"
D_{IN} = "H" or "L"

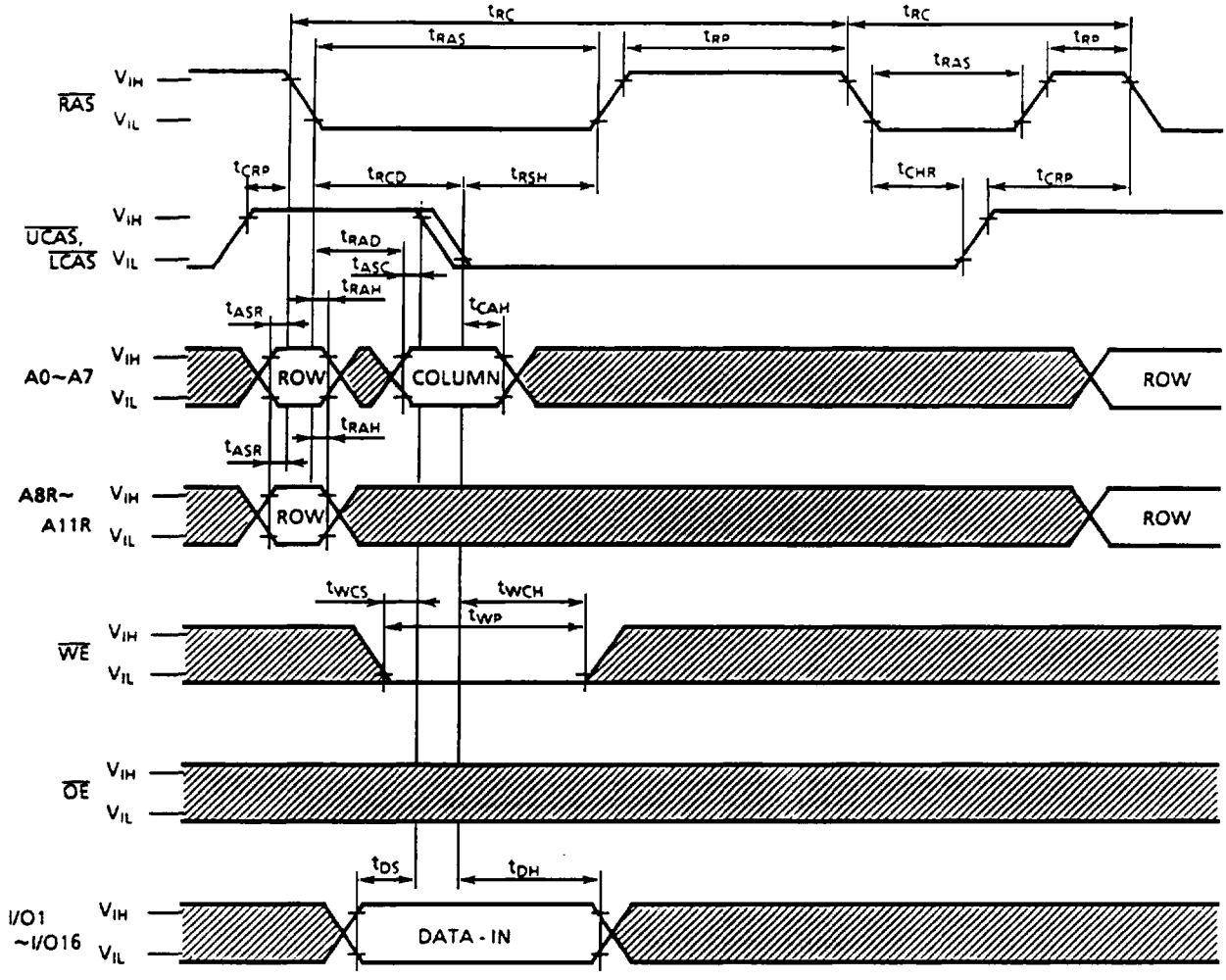
▨ : "H" or "L"

HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = Hi-Z

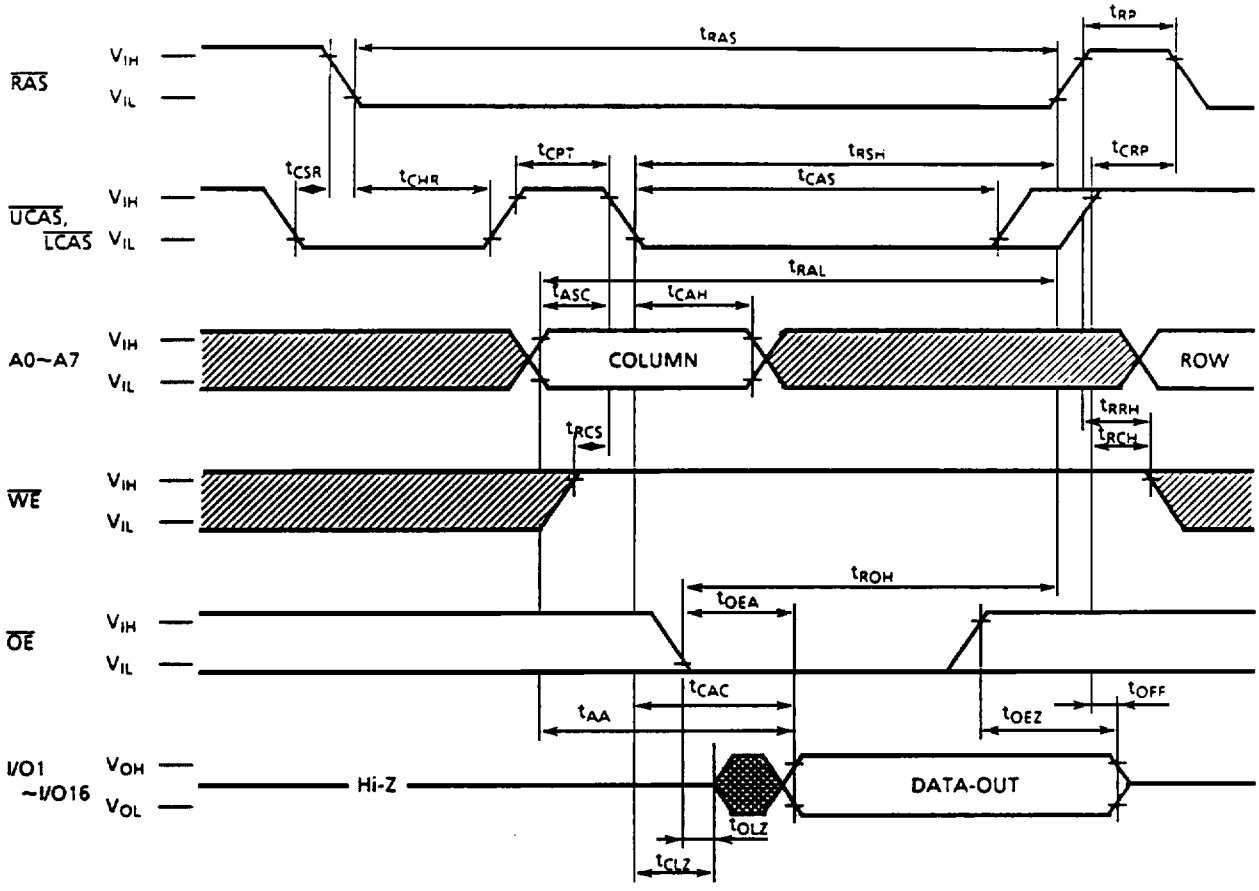
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = Hi-Z

▨ : "H" or "L"

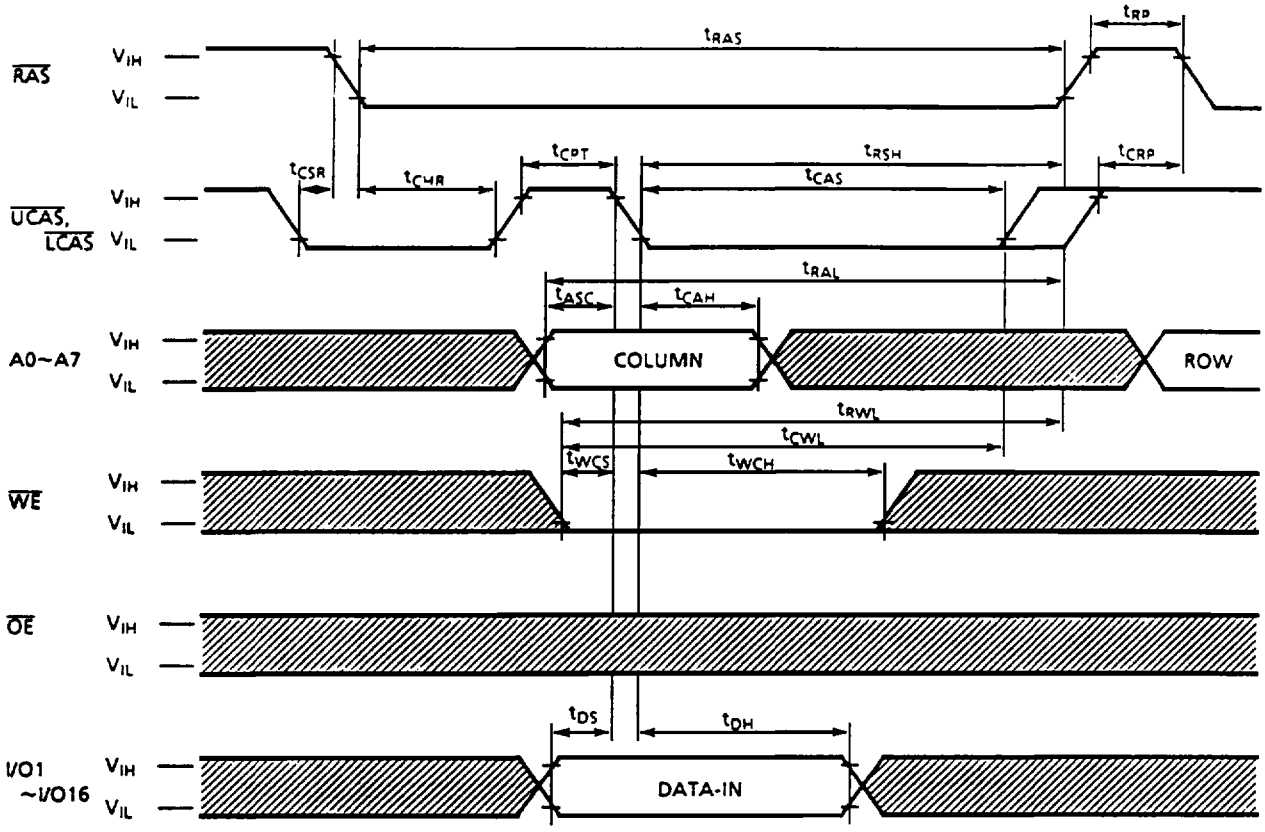
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ CYCLE



Note: A8R~A11R = "H" or "L"
D_{IN} = Hi-Z

: "H" or "L"
: Invalid Data

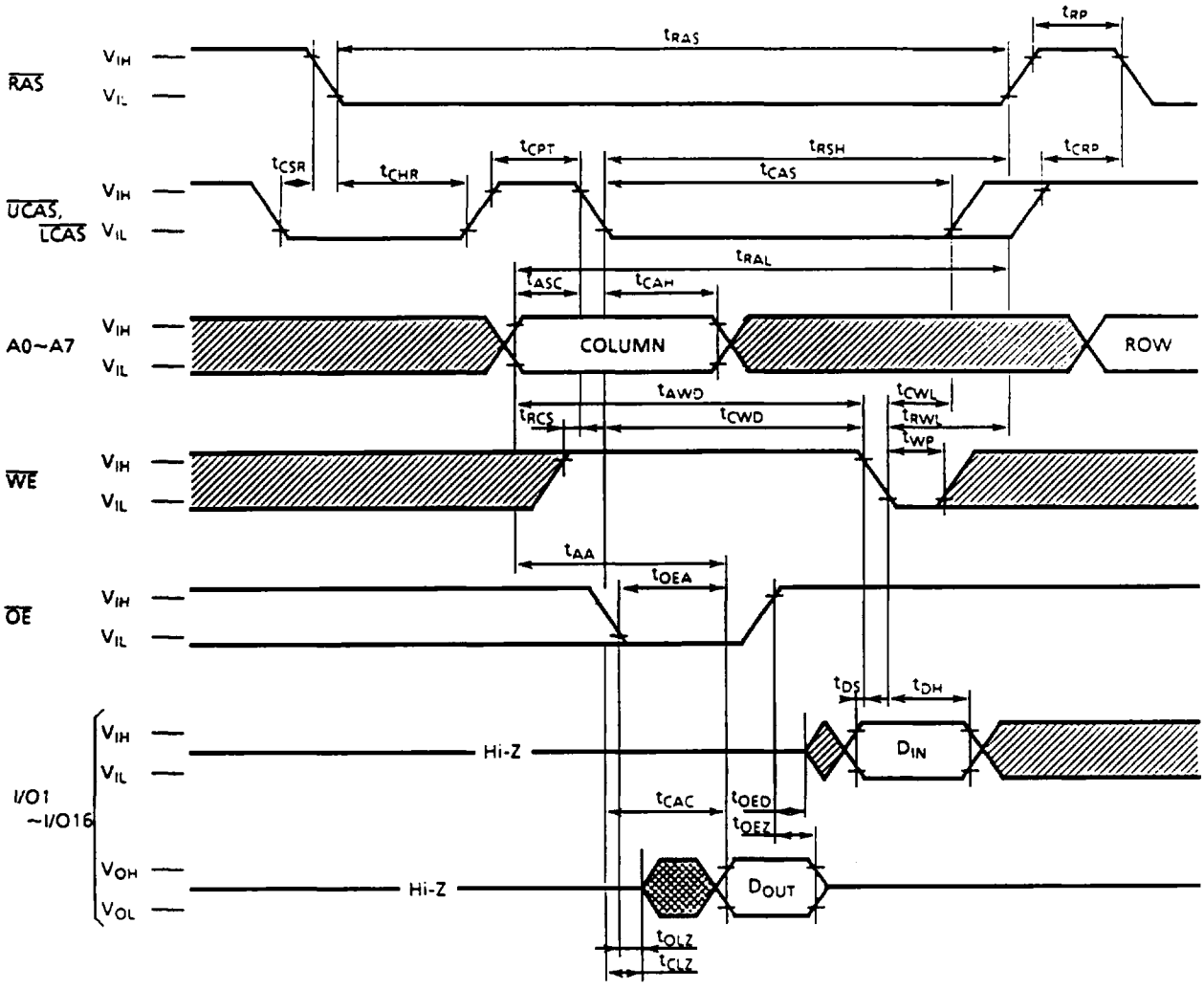
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST WRITE CYCLE



Note: A8R~A11R = "H" or "L"
D_{OUT} = Hi-Z

▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ-MODIFY-WRITE CYCLE



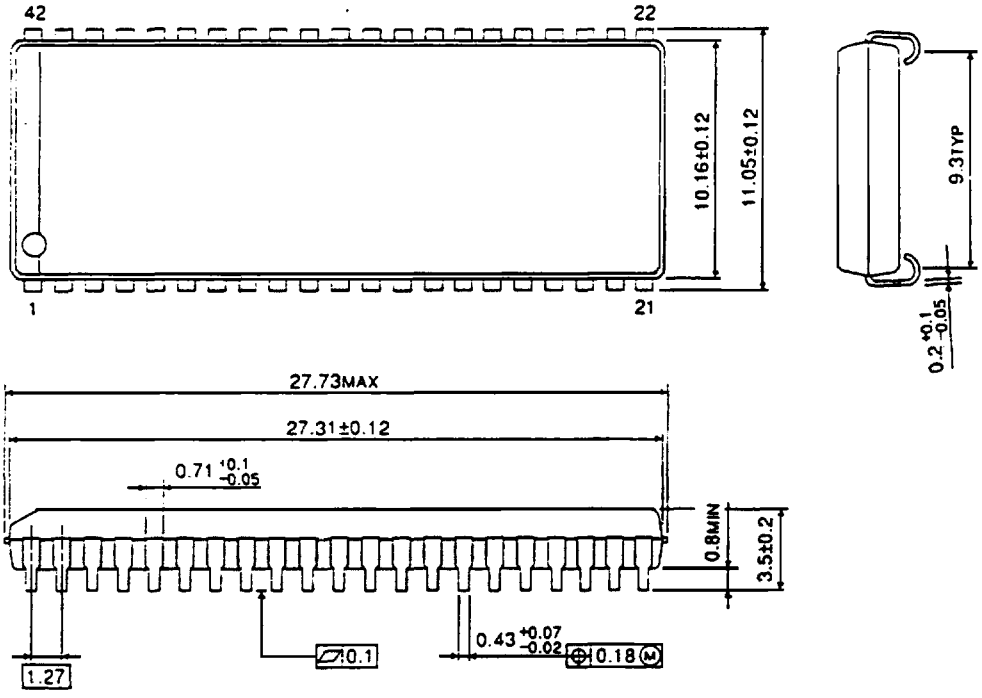
Note: A8R~A11R = "H" or "L"

: "H" or "L"

: Invalid Data

OUTLINE DRAWING (SOJ42 – P – 400)

Unit in mm



OUTLINE DRAWING (TSOP50 – P – 400)

Unit in mm