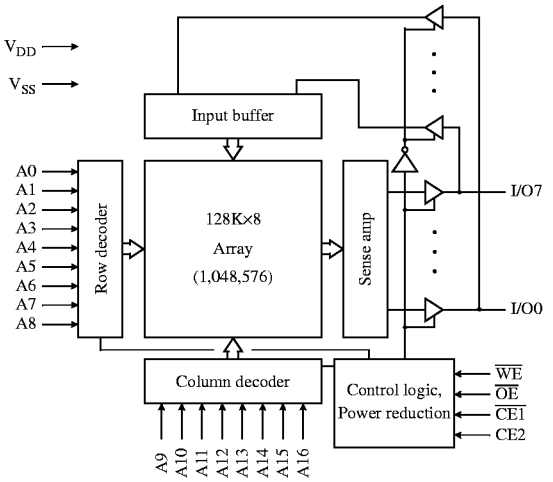
1.8V 128K×8 Intelliwatt™ low power CMOS SRAM

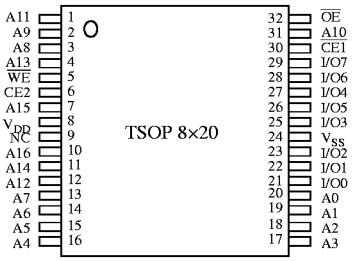
Features

- Intelliwatt active power reduction circuitry
- 1.65V to 1.95V operating range (JESD 8-7)
- Organization: 131,072 words × 8 bits
- High speed
  - 35/55/70/100 ns address access time
  - 15/25/35/50 ns output enable access time
- Low power consumption
  - Active: 36 mW max (100 ns cycle)
  - Standby: 2 µW max, CMOS I/O
  - Very low DC component in active power
- 1.2V data retention
- Easy memory expansion with $\overline{CE1}$, CE2, $\overline{OE}$ inputs
- TTL/LVTTL-compatible, three-state I/O
- JEDEC registered packaging
  - 32-pin TSOP package
  - 48-ball 8mm x 6mm CSP BGA
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA
- Industrial and commercial temperature available
- Other voltage versions available
  - 2.3V to 3.0V (AS7C251024LL)
  - 3.3V version available (AS7C31024LL)

Logic block diagram



Pin arrangement (top view)



48-CSP Ball-Grid-Array Package (shading indicates no ball)

	1	2	3	4	5	6
A	A_0	A_1	CE2	A_3	A_6	A_8
B	I/O_4	A_2	$\overline{WE}$	A_4	A_7	I/O_0
C	I/O_5		NC	A_5		I/O_1
D	V_{SS}					V_{DD}
E	V_{DD}					V_{SS}
F	I/O_6		NC	NC		I/O_2
G	I/O_7	$\overline{OE}$	$\overline{CE1}$	A_{16}	A_{15}	I/O_3
H	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}

Selection guide

	7C181024LL-35	7C181024LL-55	7C181024LL-70	7C181024LL-100	Unit
Maximum address access time	35	55	70	100	ns
Maximum output enable access time	15	25	35	50	ns
Maximum operating current	25	19	15	10	mA
Maximum CMOS standby current	1	1	1	1	µA

Functional description

The AS7C181024LL is a high performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) organized as 131,072 words × 8 bits. It is designed for portable applications where fast data access, long battery life, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 35/55/70/100 ns with output enable access times (t_{OE}) of 15/25/35/50 ns are ideal for high performance applications. Active high and low chip enables ($\overline{CE1}$, CE2) permit easy memory expansion with multiple-bank memory systems.

When $\overline{CE1}$ is HIGH or CE2 is LOW the device enters standby mode. The AS7C181024LL is guaranteed not to exceed 2µW power consumption in standby mode with the inputs static. Both devices offer data retention.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and both chip enables ($\overline{CE1}$, CE2). Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or the active-to-inactive edge of $\overline{CE1}$ or CE2 (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and both chip enables ($\overline{CE1}$, CE2), with write enable ($\overline{WE}$) HIGH. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

Low power design

In the AS7C31024LL design, priority was placed on low power, while maintaining moderately high performance. To reduce standby and data retention current, a 6-transistor memory cell was utilized. Active power was reduced considerably over traditional designs by using Intelliwatt™ power reduction circuitry. With Intelliwatt, SRAM powers down unused circuits between access operations, resulting in longer cycle times and lower duty cycles, and providing incremental power savings. During periods of inactivity, Intelliwatt SRAM power consumption can be as low as fully de-activated standby power, even though the chip is enabled. This power savings, both in active and inactive modes, results in longer battery life, and better product marketability. All chip inputs and outputs are TTL-compatible, and operation is from a single 3.3V supply. The device is packaged in common industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on any input pin	V_t	–0.5	+4.5	V
Voltage on any I/O pin	V_t	–0.5	V_{DD} + 0.4	V
Power dissipation	P_D	–	1.0	W
Storage temperature (plastic)	T_{stg}	–55	+150	°C
DC output current	I_{out}	–	20	mA

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	X	High Z	Standby (I_{SB}, I_{SB1})
X	L	X	X	High Z	Standby (I_{SB}, I_{SB1})
L	H	H	H	High Z	Output disable
L	H	H	L	D_{out}	Read
L	H	L	X	D_{in}	Write

Key: X = Don't Care, L = Low, H = High

Recommended operating conditions

Parameter	Symbol	Min	Nominal	Max	Unit
Supply voltage	V_{DD}	1.65	1.8	1.95	V
	V_{SS}	0.0	0.0	0.0	V
Input voltage	V_{IH}	2.0	–	V_{DD} + 0.5	V
	V_{IL}	–0.5	–	0.8	V

[1] V_{IL} min = –3.0V for pulse width less than $t_{RC}/2$.

DC operating characteristics [1]

Parameter	Symbol	Test conditions	-35 Min	-35 Max	-55 Min	-55 Max	-70 Min	-70 Max	-100 Min	-100 Max	Unit
Input leakage current	$\lvert I_{LI} \rvert$	V_{DD} = Max, V_{in} = GND to V_{DD}	–	1	–	1	–	1	–	1	µA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, V_{DD} = Max, V_{out} = GND to V_{DD}	–	1	–	1	–	1	–	1	µA
Operating power supply current	I_{CC}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, f = f_{max}, I_{out} = 0 mA	–	25	–	19	–	15	–	10	mA
Standby power supply current	I_{SB}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, f = f_{max}	–	500	–	400	–	300	–	200	µA
	I_{SB1}	$\overline{CE1}$ ≥ V_{DD}–0.2V or CE2 ≤0.2V, V_{in} ≤ 0.2V or V_{in} ≥ V_{DD}–0.2V, f = 0	–	1	–	1	–	1	–	1	µA
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{DD} = Min	–	0.4	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{DD} = Min	2.4	–	2.4	–	2.4	–	2.4	–	V

Capacitance [2]

(f = 1 MHz, T_a = Room temperature, V_{DD} = 3.3V)

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE1}$, CE2, $\overline{WE}$, $\overline{OE}$	V_{in} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{in} = V_{out} = 0V	7	pF

Read cycle [3,9]

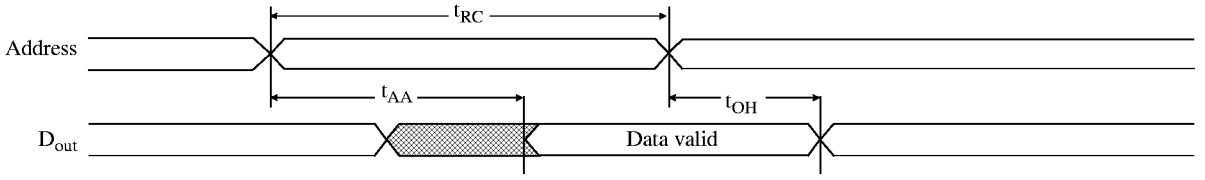
		-35		-55		-70		-100			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	35	–	55	–	70	–	100	–	ns	
Address access time	t_{AA}	–	35	–	55	–	70	–	100	ns	3
Chip enable ($\overline{CE}$) access time	t_{ACE}	–	35	–	55	–	70	–	100	ns	3
Output enable ($\overline{OE}$) access time	t_{OE}	–	15	–	25	–	35	–	50	ns	
Output hold from address change	t_{OH}	4	–	4	–	4	–	4	–	ns	5
$\overline{CE}$ Low to output in low Z	t_{CLZ}	0	–	0	–	0	–	0	–	ns	4, 5
$\overline{CE}$ High to output in high Z	t_{CHZ}	–	6	–	8	–	10	–	10	ns	4, 5
$\overline{OE}$ Low to output in low Z	t_{OLZ}	0	–	0	–	0	–	0	–	ns	4, 5
Byte select access time	t_{BA}	–	8	–	12	–	16	–	20	ns	
Byte select Low to Low-Z	t_{BLZ}	0	–	0	–	0	–	0	–	ns	4,5
Byte select High to HI-Z	t_{BHZ}	–	6	–	8	–	10	–	10	ns	4,5
$\overline{OE}$ High to output in high Z	t_{OHZ}	–	6	–	8	–	10	–	10	ns	4, 5
Power up time	t_{PU}	0	–	0	–	0	–	0	–	ns	4, 5
Power down time	t_{PD}	–	35	–	55	–	70	–	100	ns	4, 5

Key to switching waveforms

Rising input Falling input Undefined output/don't care

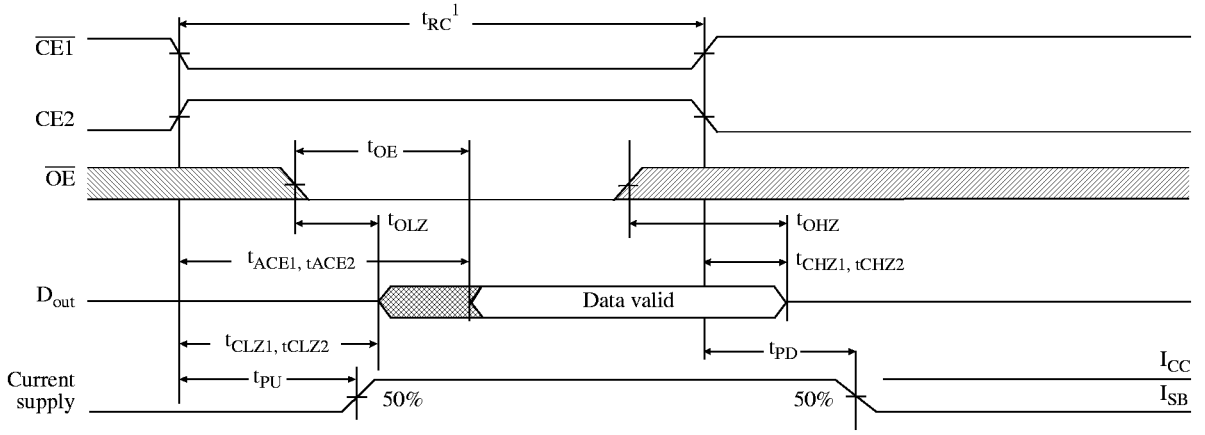
Read waveform 1 [3,6,7,9,12]

Address controlled



Read waveform 2 [3,6,8,9,12]

$\overline{CE1}$ and CE2 controlled

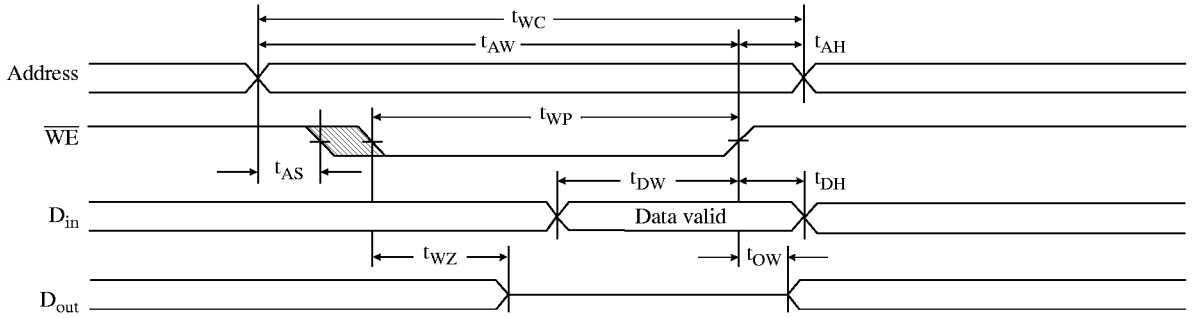


Write cycle [11]

		-15		-25		-35		-55			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t_{WC}	35	–	55	–	70	–	100	–	ns	
Chip enable ($\overline{CE}$) to write end	t_{CW}	12	–	15	–	30	–	40	–	ns	
Address setup to write end	t_{AW}	10	–	14	–	30	–	40	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	ns	
Write pulse width	t_{WP}	10	–	14	–	30	–	40	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	8	–	10	–	25	–	25	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	0	–	ns	5
Write enable to output in high Z	t_{WZ}	–	6	–	8	–	10	–	10	ns	4, 5
Output active from write end	t_{OW}	1	–	2	–	5	–	5	–	ns	4, 5
Byte select low to end of write	t_{BW}	9	–	14	–	30	–	40	–	ns	

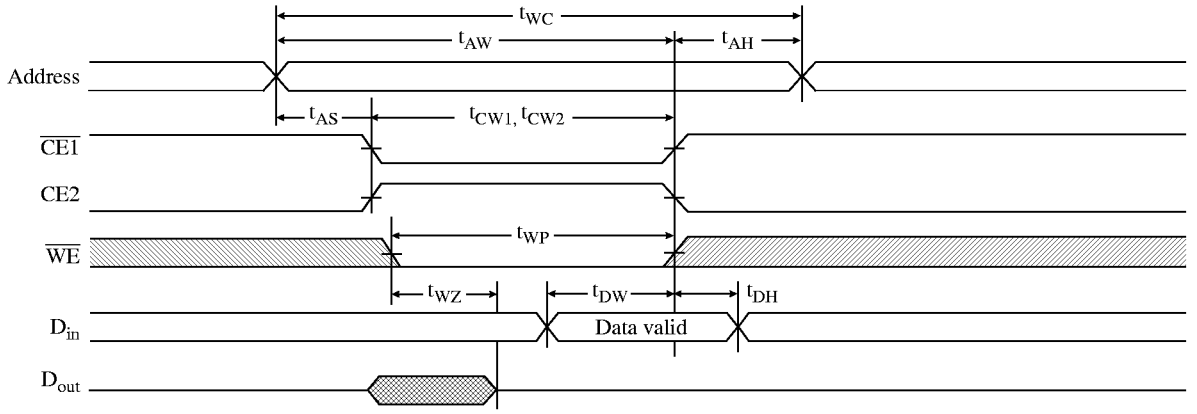
Write waveform 1 [10,11,12]

$\overline{WE}$ controlled



Write waveform 2 [10,11,12]

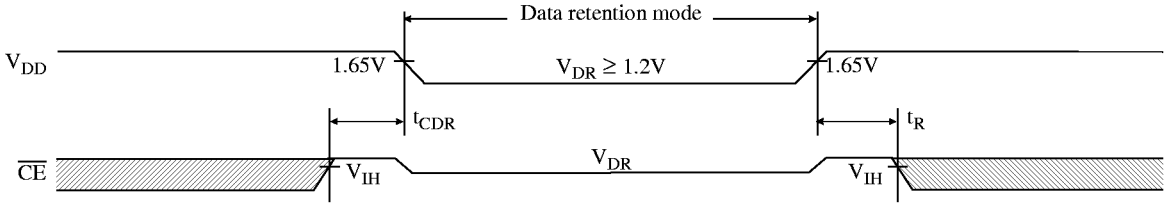
$\overline{CE1}$ and CE2 controlled



Data retention characteristics

Parameter	Symbol	Test conditions	Min	Max	Unit	Notes
V_{DD} for data retention	V_{DR}	V_{DD} = 1.2V	1.2	–	V	
Data retention current	I_{CCDR}	$\overline{CE} \geq V_{DD}-0.2V$	–	0.4	µA	5
Chip deselect to data retention time	t_{CDR}	$V_{in} \geq V_{DD}-0.2V$ *or*	0	–	ns	5
Operation recovery time	t_R	$V_{in} \leq 0.2V$	t_{RC}	–	ns	5

Data retention waveform



AC test conditions

- 3.3V output load: see Figure B, except as noted see Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

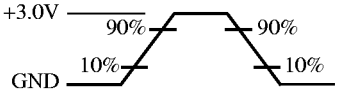


Figure A: Input waveform

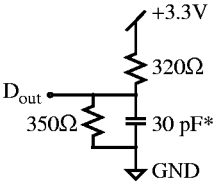
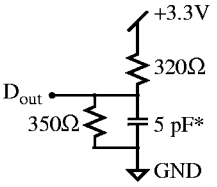


Figure B: Output load



*including scope and jig capacitance

Figure C: Output load for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{OW}

Notes

1 During V_{DD} power-up, a pull-up resistor to V_{DD} on $\overline{CE1}$ is required to meet I_{SB} specification.
2 This parameter is sampled and not 100% tested.
3 For test conditions, see AC Test Conditions, Figures A, B, C.
4 t_{CLZ} and t_{CHZ} are specified with CL = 5pF as in Figure C. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed but not tested.
6 $\overline{WE}$ is HIGH for read cycle.
7 $\overline{CE1}$ and $\overline{OE}$ are LOW and CE2 is HIGH for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition LOW.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CE1}$ or $\overline{WE}$ must be HIGH or CE2 LOW during address transitions.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 $\overline{CE1}$ and CE2 have identical timing.

AS7C181024LL ordering codes

Package \ Access time	35 ns	55 ns	70 ns	100 ns
TSOP 8×20	AS7C181024LL-35TC	AS7C181024LL-55TC	AS7C181024LL-70TC	AS7C181024LL-100TC
	AS7C181024LL-35TI	AS7C181024LL-55TI	AS7C181024LL-70TI	AS7C181024LL-100TI
CSP BGA	AS7C181024LL-35BC	AS7C181024LL-55BC	AS7C181024LL-70BC	AS7C181024LL-100BC
	AS7C181024LL-35BI	AS7C181024LL-55BI	AS7C181024LL-70BI	AS7C181024LL-100BI

AS7C181024LL part numbering system

AS7C	18	1024LL	-XX	X	X
SRAM prefix	3=3.3V CMOS 25=2.5V CMOS 18=1.8V CMOS	Device number	Access time	Package: T =TSOP 8×20 B=CSP BGA	C = Commercial temperature range, 0 ℃ to 70 ℃ I = Industrial temperature range, -40 ℃ to 85 ℃

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