Features

- Fast Read Access Time 70 ns
- Low Power CMOS Operation
 100 μA Maximum Standby

35 mA Maximum Active at 5 MHz

- JEDEC Standard Packages
 - 40-Lead 600 mil PDIP
 - 44-Lead PLCC
 - 40-Lead TSOP (10 mm X 14 mm)
- Direct Upgrade from 512K bit and 1M bit (AT27C516 and AT27C1024) EPROMs
- 5V ± 10% Power Supply
- High Reliability CMOS Technology 2,000V ESD Protection
 - 200 mA Latchup Immunity
- Rapid[™] Programming Algorithm 50 µs/word (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

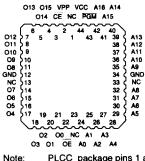
The AT27C2048 is a low-power, high performance 2,097,152 bit one-time program-mable read only memory (OTP EPROM) organized as 128K by 16 bits. It requires a single 5V power supply in normal read mode operation. Any word can be accessed in less than 70 ns, eliminating the need for speed-reducing WAIT states. The by-16 organization makes this part ideal for high-performance 16 and 32 bit microprocessor systems.

Pin Configurations

Pin Name	Function
A0 - A16	Addresses
O0 - O15	Outputs
CE	Chip Enable
ŌĒ	Output Enable
PGM	Program
NC	No Connect

Note: Both GND pins must be connected.





PLCC package pins 1 and 23 are DON'T CONNECT. PDIP Top View (continued)

VPP	С	1	4	`	vcc
CE	d	2	39	•	VCC PSIM A15 A16 A17 A10 A11 A10 A11 A10 A11 A10 A11 A10 A11 A10 A11 A10 A11 A10 A11 A10 A11 A10 A11 A10 A11 A10 A11 A10 A11 A11
O15	4	3	34	3	A16
014	4	4	37	7	A15
013	Ц	2 3 4 5 6 7	36	3	A14
012	d	6	35	5	A13
011	п	7	34	٠	A12
010	d	9	31 34 34 33 33 33	3	3 A11
09	d	9	30	2	- A10
08	C	10	3	١	A10
GND		11	30	١,	GND
07	4	12	30 21 21	•	⊐ A8
06		13	21	8	⊒ A7
05	L	14	2	7	: A6
05 04	d	15	21	8	- A5
03	d	16	-	5	D A4
02	d	17	24	٠	- A3
01 00 0F		18 19 20	2:	3	GND A8 A7 A6 A6 A A3 A A3 A A1 A A1 A A0
00	į	19	2	2	: A1
OF	_	20	,	١ ۱	- A0

TSOP Top View
Type 1

Ay	A10	()	1 0	40	39	□ A8 □	GIND
A11		_	3 2	38		7	A7
A13	A12 [4	5	36	37	B A8	A5
	A14 F	6	-		35	. ₩	
A15	F 214.	8	7	34	33	5 A2	A3
PGM		-	9	32			A1
VPP	vcc	10	11	30	31	AO	Œ
	CE 9	12	**		29	D 00	
Q15	014	14	13	28	27	02	01
013	012		15	26		P	О3
011	012 1		17	24	20	7	05
	O IV U		**			5 06	
09	06 🗄	20	19	22	21	GND	07
	-						

2 Megabit (128K x 16) OTP CMOS EPROM

Preliminary

0632A





Description (Continued)

In read mode, the AT27C2048 typically consumes 15 mA. Standby mode supply current is typically less than 10 μ A.

The AT27C2048 is available in industry standard JEDEC-approved one-time programmable (OTP) plastic, PDIP, PLCC, and TSOP packages. The device features two-line control (CE, OE) to eliminate bus contention in high-speed systems.

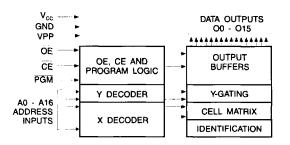
With high density 128K word storage capability, the AT27C2048 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's AT27C2048 has additional features that ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 50 μs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias55°C to +125°C
Storage Temperature65°C to +150°C
Voltage on Any Pin with Respect to Ground2.0V to +7.0V ⁽¹⁾
Voltage on A9 with Respect to Ground2.0V to +14.0V ⁽¹⁾
V _{PP} Supply Voltage with Respect to Ground2.0V to +14.0V ⁽¹⁾

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	CE	ŌĒ	PGM	Ai	VPP	Outputs
Read	VIL	VIL	X ⁽¹⁾	Ai	X ⁽¹⁾	Dout
Output Disable	Х	Vıн	X	X	X	High Z
Standby	VIH	Х	Х	Х	X ⁽⁵⁾	High Z
Rapid Program (2)	VIL	ViH	VIL	Ai	VPP	Din
PGM Verify	VIL	ViL	ViH	Ai	VPP	Dout
PGM Inhibit	ViH	Χ	X	X	V_{PP}	High Z
Product Identification (4)	VIL	VIL	Х	A9 = V _H ⁽³⁾ A0 = V _{IH} or V _{IL} A1 - A16 = V _{IL}	Vcc	Identification Code

Notes: 1. X can be VIL or VIH.

- 2. Refer to the Programming Characteristics.
- 3. $V_H = 12.0 \pm 0.5 V$.

- 4. Two identifier words may be selected. All Ai inputs are held low (V_{IL}), except A9, which is set to V_H, and A0, which is toggled low (V_{IL}) to select the Manufacturer's Identification word and high (V_{IH}) to select the Device Code word.
- Standby V_{CC} current (I_{SB}) is specified with V_{PP} = V_{CC}.
 V_{CC} > V_{PP} will cause a slight increase in I_{SB}.





DC and AC Operating Conditions for Read Operation

-		AT27C2048					
		-70	-90	-12	15		
Operating	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C		
Temperature (Case)	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C		
Vcc Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%		

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
lu _	Input Load Current	V _{IN} = 0V to V _{CC}		± 1	μА
lo_	Output Leakage Current	Vout = 0V to Vcc		± 5	μА
IPP1 (2)	V _{PP} ⁽¹⁾ Read/Standby Current	VPP = VCC		10	μА
Isa	V _{CC} ⁽¹⁾ Standby Current	I _{SB1} (CMOS) CE = V _{CC} ± 0.3V		100	μΑ
שטי	VCC Standby Current	$\frac{I_{SB2} \text{ (TTL)}}{CE} = 2.0 \text{ to V}_{CC} + 0.5 \text{V}$		1	mA
lcc	V _{CC} Active Current	f = 5 MHz,lout = 0 mA, $\overline{CE} = V_{IL}$		35	mA
VIL	Input Low Voltage		-0.6	8.0	V
ViH	Input High Voltage		2.0	V _{CC} + 0.5	V_
Vol	Output Low Voltage	l _{OL} ≈ 2.1 mA		0.4	V
Voн	Output High Voltage	I _{OH} = -400 μA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

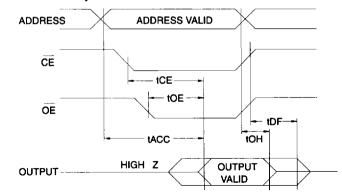
AC Characteristics for Read Operation

			AT27C2048								
				70_		90	_	12		15	
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Units
tacc (3)	Address to Output Delay	CE = OE = V _I L		70		90		120		150	ns
tce (2)	CE to Output Delay	OE = VIL		70		90		120		150	ns
toE (2, 3)	OE to Output Delay	CE = V _{IL}		40		40		40		50	ns
tpr (4, 5)	OE or CE High to Output Float, whicheve	er occurred first		30		30		35		40	ns
toн ⁽⁴⁾	Output Hold from Address, CE or OE, wh	nichever occurred first	7		0		0		0		ns

Notes: 2, 3, 4, 5. See the AC Waveforms for Read Operation diagram.

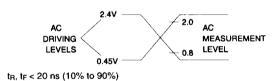
V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{CC}.

AC Waveforms for Read Operation (1)



- Notes: 1. Timing measurement references are 0.8V and 2.0V.
 Input AC drive levels are 0.45V and 2.4V, unless
 otherwise specified.
 - 2. OE may be delayed up to tce toe after the falling edge of CE without impact on tce.
- 3. OE may be delayed up to tACC tOE after the address is valid without impact on tACC.
- 4. This parameter is only sampled and is not 100% tested.
- 5. Output float is defined as the point when data is no longer driven

Input Test Waveforms and Measurement Levels



Output Test Load



Note: CL = 100 pF including jig capacitance.

Pin Capacitance (f = 1 MHz T = 25°C) (1)

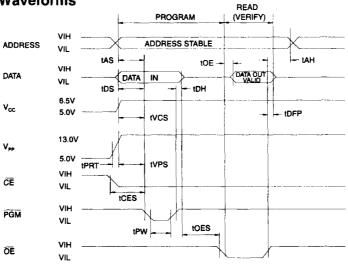
	Тур	Max	Units	Conditions	
CIN	4	10	pF	V _{IN} = 0V	
Соит	8	12	pF	V _{OUT} = 0V	

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.





Programming Waveforms (1)



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH} .

- 2. toe and topp are characteristics of the device but must be accommodated by the programmer.
- 3. When programming the AT27C2048, a 0.1 μ F capacitor is required across Vpp and ground to suppress spurious voltage transients.

DC Programming Characteristics

 $T_A = 25 \pm 5$ °C, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

		Limits					
Symbol	Parameter	Test Conditions	Min	Max	Units		
ILI	Input Load Current	V _{IN} = V _{IL} , V _{IH}		± 10	μА		
VIL	Input Low Level		-0.6	0.8	V		
ViH	Input High Level		2.0	V _{CC} + 0.5	٧		
Vol	Output Low Voltage	l _{OL} = 2.1 mA		0.4	V		
Vон	Output High Voltage	I _{OH} = -400 μA	2.4		٧		
Icc2	V _{CC} Supply Current (Program and Verify)			50	mA		
Ipp2	Vpp Supply Current	CE = VIL		30	mA		
Vات	A9 Product Identification Voltage		11.5	12.5	٧		

AC Programming Characteristics

 $T_A = 25 \pm 5^{\circ}C$, $V_{CC} = 6.5 \pm 0.25V$, $V_{PP} = 13.0 \pm 0.25V$

	Darramatar Test	Lin	nits		
Sym- bol	Parameter Conditions* (1)	Min	Max	Units	
tas	Address Setup Time	2		μS	
toes	OE Setup Time	2		μS	
tos	Data Setup Time	2		μS	
tan	Address Hold Time	0		μS	
toH	Data Hold Time	2		μS	
tDFP	OE High to Output Float Delay ⁽²⁾	0	130	ns	
tvps	V _{PP} Setup Time	2		μS	
tvcs	V _{CC} Setup Time	2		μs	
tpw	PGM Program Pulse Width (3)	47.5	52.5	μS	
toE	Data Valid from OE		150	ns	
t _{PRT}	VPP Pulse Rise Time During Programming	50		ns	

*AC Conditions of Test:

Input Hise and Fall Times (10% to 90%	6)20 ns
Input Pulse Levels	0.45V to 2.4V
Input Timing Reference Level	0.8V to 2.0V
Output Timing Reference Level	0.8V to 2.0V

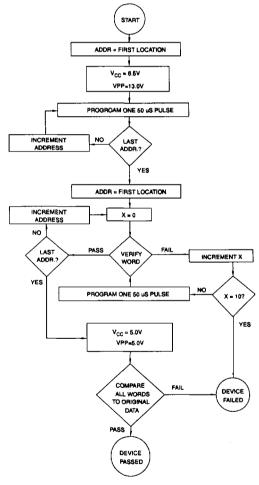
- Notes: 1. VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.
 - 2. This parameter is only sampled and is not 100% tested. Ouput Float is defined as the point where data is no longer driven — see timing diagram.
 - 3. Program Pulse width tolerance is 50 µsec ± 5%.

Atmel's 27C2048 Integrated **Product Identification Code**

	Pins					Hex					
Codes	ΑO	015-08	07	O 6	O 5	04	ОЗ	02	01	00	Data
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	1	1	1	1	0	1	1	1	00F7

Rapid Programming Algorithm

A 50 µs \overline{CE} pulse width is used to program. The address is set to the first location. VCC is raised to 6.5V and VPP is raised to 13.0V. Each address is first programmed with one 50 µs CE pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 50 µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. Vpp is then lowered to 5.0V and Vcc to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.







Ordering Information

t _{ACC} (ns)	lcc (mA)		0.4101				
	Active	Standby	Ordering Code	Package	Operation Range		
70	35	0.1	AT27C2048-70JC AT27C2048-70PC AT27C2048-70VC	44J 40P6 40V	Commercial (0°C to 70°C)		
	35	0.1	AT27C2048-70JI AT27C2048-70PI AT27C2048-70VI	44J 40P6 40V	Industrial (-40°C to 85°C)		
90	35	0.1	AT27C2048-90JC AT27C2048-90PC AT27C2048-90VC	44J 40P6 40V	Commercial (0°C to 70°C)		
	35	0.1	AT27C2048-90JI AT27C2048-90PI AT27C2048-90VI	44J 40P6 40V	Industrial (-40°C to 85°C)		
120	35	0.1	AT27C2048-12JC AT27C2048-12PC AT27C2048-12VC	44J 40P6 40V	Commercial (0°C to 70°C)		
	35	0.1	AT27C2048-12JI AT27C2048-12PI AT27C2048-12VI	44J 40P6 40V	Industrial (-40°C to 85°C)		
150	35	0.1	AT27C2048-15JC AT27C2048-15PC AT27C2048-15VC	44J 40P6 40V	Commercial (0°C to 70°C)		
	35	0.1	AT27C2048-15JI AT27C2048-15PI AT27C2048-15VI	44J 40P6 40V	Industrial (-40°C to 85°C)		

Package Type				
44J	44J 44 Lead, Plastic J-Leaded Chip Carner (PLCC)			
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)			
40V	40 Lead, Plastic Thin Small Outline Package (TSOP) 10 x 14 mm			

AT27C2048