T-51-10-12

MP574A

Complete 12-Bit, 20µsec Analog-to-Digital Converter with Microprocessor Interface

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FEATURES

- **Complete 12-Bit A/D Converter with Reference Clock and Three-state Outputs**
- **Full 8- or 16-Bit Microprocessor Bus Interface**
- **200 ns Bus Access Time**
- **Guaranteed Linearity Over Temperature**
- **No Missing Codes Over Temperature**
- **ESD Protection: 1500 V Minimum**
- **Fast Conversion (20 µsec)**
- **Precision Reference for Long Term Stability and Low Gain T.C.**
- **Low Power: 240 mW typ.**
- **Guaranteed Performance at ±12 V and ±15 V**
- **PDIP, CDIP, SOIC & PLCC Packages Available**

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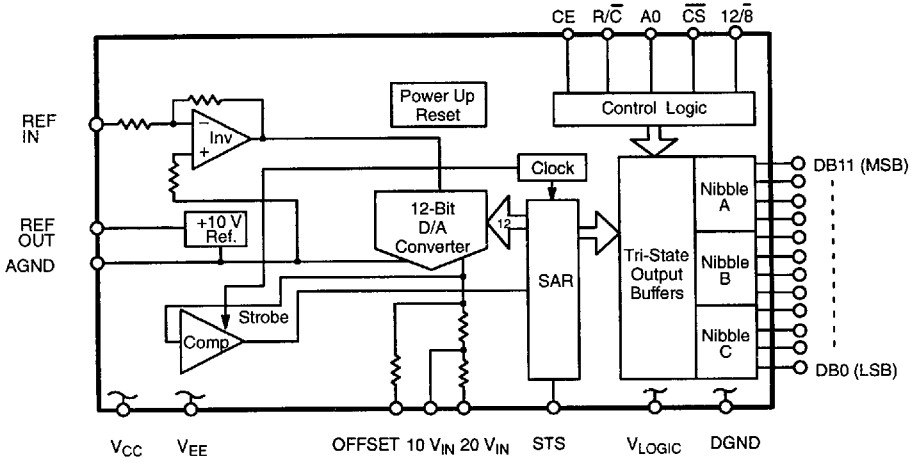
GENERAL DESCRIPTION

The MP574A is a complete 12-bit A/D converter with 3-state output buffers for direct interfacing to 8- and 16-bit microprocessor busses. Implemented in advanced BiCMOS, the converter combines a SAR, a 12-bit decoded D/A, a comparator and a precision reference with the appropriate control logic to achieve an accurate conversion in 20µs. The 12/$\overline{8}$ mode control TTL is microprocessor compatible, such that users may switch freely between the full 12-bit and short cycled 8-bit formats.

A unique comparator input design reduces kickback noise to the source and the proprietary decoded D/A section assures no missing codes for all grades. The reference has enough output drive that no buffer is required at REF IN, even with 12 VDC operation. Precision thin film scaling and offset resistors are laser trimmed to provide the four calibrated ranges, 0 to +10 V and 0 to +20 V in the unipolar mode and ±5 V and ±10 V for bipolar applications.

Specified for operation over the commercial (0 to 70°C) and military (–55 to +125°C) temperature ranges, the MP574A is available in Plastic (PDIP) and Ceramic (CDIP) dual-in-line, Surface Mount (SOIC), and Plastic leaded chip carrier (PLCC) packages.

SIMPLIFIED BLOCK DIAGRAM



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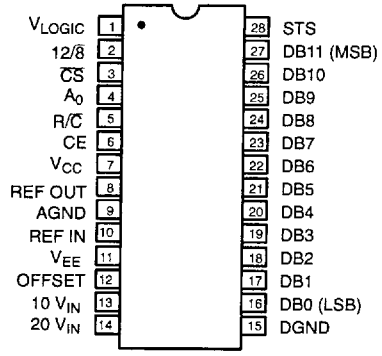
ORDERING INFORMATION

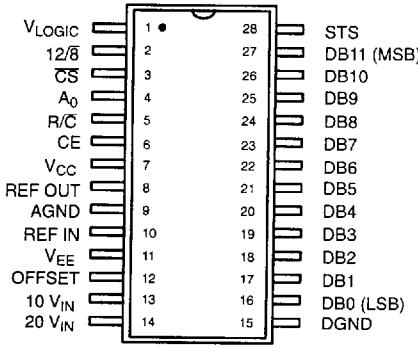
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	0 to 70°C	MP574AJN	±1	±1	±0.3
Plastic Dip	0 to 70°C	MP574AKN	±1/2	±1	±0.3
SOIC	0 to 70°C	MP574AJS	±1	±1	±0.3
SOIC	0 to 70°C	MP574AKS	±1/2	±1	±0.3
PLCC	0 to 70°C	MP574AJP	±1	±1	±0.3
PLCC	0 to 70°C	MP574AKP	±1/2	±1	±0.3
Ceramic Dip	−55 to +125°C	MP574ASD/883*	±1	±1	±0.3
Ceramic Dip	−55 to +125°C	MP574ATD*	±1	±1/2	±0.3
Ceramic Dip	−55 to +125°C	MP574ATD/883*	±1	±1/2	±0.3
Ceramic Dip	−55 to +125°C	MP574AUD*	±1	±1/2	±0.3
Ceramic Dip	−55 to +125°C	MP574AUD/883*	±1	±1/2	±0.3

*Contact factory for availability.

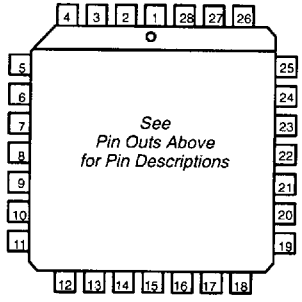
PIN CONFIGURATIONS



28 Pin PDIP, CDIP (0.600")
N28, D28



28 Pin SOIC, (Jedec, 0.300")
S28



28 Pin PLCC
P28

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PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	V_{LOGIC}	+5 V Logic Supply
2	12/$\overline{8}$	Select format of Output Bits (8 or 12) (TTL-compatible.)
3	$\overline{CS}$	Chip Select. Enables conversion on falling clock edge.
4	A0	Access high 8 bits or low 4 bits plus 4 zeroes (read mode).
5	R/$\overline{C}$	Read/Convert: main control for Stand-Alone operation.
6	CE	Chip Enable. Enables conversion on rising clock edge.
7	V_{CC}	+12 V to +15 V
8	REF OUT	Output from internal +10 V reference.
9	AGND	Analog Ground
10	REF IN	Input for Voltage Reference
11	V_{EE}	−12 V to −15 V
12	OFFSET	Voltage input for Bipolar operation, or zero adjust
13	10 V_{IN}	Input for 0 to +10 V or −5 V to +5 V operation. *
14	20 V_{IN}	Input for 0 to +20 V or −10 V to +10 V operation
15	DGND	Digital Ground
16-27	Output Data Bits	DB0 (LSB) to DB11 (MSB)
28	STS	Status

DEFINING THE CONTROL FUNCTIONS

FUNCTION	DEFINITION	FUNCTION
CE	Chip Enable	1. Typically used as clock synchronization with µp 2. Must be high (1) for a conversion to start 3. Must be high (1) to read data on the output 4. ↑ Transition may be used to initiate conversion
$\overline{CS}$	Chip Select	1. Typically the address pin when used with a microprocessor. 2. Must be low (0) for a conversion to start or read data at the output 3. ↓ Transition may be used to initiate conversion
R/$\overline{C}$	Read/Convert	1. ↓ Initiate conversion 2. ↑ Initiate read
A0	Address	1. Selects conversion mode 12 Bits if low (0) 8 Bits if high (1) 2. In read mode Ao selects the output format. If low (0) then 8 MSBs (high and middle byte) are enabled. If high (1) then the 4 LSBs are enabled.
12/$\overline{8}$	Output Format	1. Usually hard-wired 2. Normal 12 Bit format if high (1) 3. 8-Bit format as set by Ao if low (0)

* When not in use, NC to avoid noise pick-up.

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ELECTRICAL CHARACTERISTICS

(@ +25°C with V_{CC} = +15 V, V_{LOGIC} = +5 V, V_{EE} = −15 V unless otherwise indicated)

Description	MP574AJN/P Min	Typ	Max	MP574AKN/P Min	Typ	Max	Units
RESOLUTION	12			12			Bits
LINEARITY ERROR @ +25°C			±1			±1/2	LSB
Tmin to Tmax			±1			±1/2	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed) Tmin to Tmax	12			12			Bits
UNIPOLAR OFFSET (Adjustable to zero)			±2			±1	LSB
BIPOLAR OFFSET (1) (Adjustable to zero)			±4			±4	LSB
FULL-SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF OUT to REF IN) (Adjustable to zero)			±0.3			±0.3	% of F_S
TEMPERATURE RANGE	0		+70	0		+70	°C
TEMPERATURE COEFFICIENTS (using internal reference) Tmin to Tmax							
Unipolar Offset			±2(10)			±1(5)	LSB(ppm/°C)*
Bipolar Offset			±2(10)			±1(5)	LSB(ppm/°C)*
Full-Scale Calibration			±9(50)			±5(27)	LSB(ppm/°C)*
POWER SUPPLY REJECTION Max change in Full Scale Calibration							
V_{CC} = 15 V ±1.5 V or 12 V ±0.6 V			±2			±1	LSB
V_{LOGIC} = 5 V ±0.5 V			±1/2			±1/2	LSB
V_{EE} = −15 V ±1.5 V or −12 V ±0.6 V			±2			±1	LSB
ANALOG INPUT							
Input Ranges							
Bipolar, 10 V_{IN}	−5		+5	−5		+5	V
20 V_{IN}	−10		+10	−10		+10	V
Unipolar, 10 V_{IN}	0		+10	0		+10	V
20 V_{IN}	0		+20	0		+20	V
Input Impedance							
10 V_{IN}	3	5	7	3	5	7	kΩ
20 V_{IN}	6	10	14	6	10	14	kΩ
DIGITAL CHARACTERISTICS (2)							
Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A0, 12/$\overline{8}$)							
Logic "1" Voltage	+2.0		+5.5	+2.0		+5.5	V
Logic "0" Voltage	−0.5		+0.8	−0.5		+0.8	V
Current	−5		+5	−5		+5	µA
Capacitance		5			5		pF
Outputs (DB11-DB0, STS)							
Logic "1" Voltage (I_{SOURCE} ≤ 500µA)	+2.4			+2.4			V
Logic "0" Voltage (I_{SINK} ≤ 1.6mA)			+0.4			+0.4	V
Leakage (DB11-DB0, High-Z State)	−5		+5	−5		+5	µA
Capacitance		5			5		pF

* ppm information for reference only.

Specifications subject to change without notice

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ELECTRICAL CHARACTERISTICS (CON'T)

Description	MP574AJN/P Min	MP574AJN/P Typ	MP574AJN/P Max	MP574AKN/P Min	MP574AKN/P Typ	MP574AKN/P Max	Units
POWER SUPPLIES							
Operating Range							
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	V
V_{CC}	+11.4		+16.5	+11.4		+16.5	V
V_{EE}	−11.4		−16.5	−11.4		−16.5	V
Operating Current							
I_{LOGIC}		3	6		3	6	mA
I_{CC}		7	10		7	10	mA
I_{EE}		8	12		8	12	mA
POWER DISSIPATION		240	360		240	360	mW
INTERNAL REFERENCE VOLTAGE	9.95	10.0	10.05	9.95	10.0	10.05	V
Output current (available for external loads) (External load should not change during conversion)	1.5	5		1.5	5		mA

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NOTES:

(1) Bipolar offset zero transition.
(2) Detailed timing specifications appear in the timing section.

Specifications subject to change without notice

ABSOLUTE MAXIMUM RATINGS (1, 2) (T_A = +25°C unless otherwise noted)

V_{CC} to DGND ..... 0 to +16.5 V
V_{EE} to DGND ..... 0 to −16.5 V
V_{LOGIC} to DGND ..... 0 to +7 V
AGND to DGND ..... ±1 V
Control Inputs (CE, $\overline{CS}$, A0, 12/$\overline{8}$, R/$\overline{C}$) to DGND ..... −0.5 V to V_{LOGIC} +0.5 V
Analog Inputs (REF IN, OFFSET, 10 V_{IN}) to AGND ..... ±16.5 V
20 V_{IN} to AGND ..... ±24 V
REF OUT ..... Indefinite short to DGND, Momentary short to V_{CC}
Package Power Dissipation Rating to 75°C
PDIP, CDIP, SOIC, PLCC 1000mW
Derates above 75°C ..... 14mW/°C
Lead Temperature, Soldering ..... +300°C, 10 Sec
Storage Temperature ..... −65°C to +150°C

NOTES:

(1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
(2) Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

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APPLICATION DATA

The MP574A is a complete A/D converter system, with its own built-in reference and clock. It may be used by itself ("stand-alone" operation), or it may be interfaced with a microprocessor which can control both conversion and formatting of output.

Successful application of the MP574A requires careful attention to four main areas:

1) Physical layout.
2) Connection/Trimming according to mode of operation.
3) Conditioning of input signals.
4) Controlling and Timing considerations.

Physical Layout

The 12-bit accuracy of the MP574A represents a dynamic range of 72dB. In order that this be preserved, thorough precautions must be taken to avoid any interfering signals, whether conducted or radiated. It is therefore recommended that one:

- Avoid placing the chip and its analog signals near logic traces. In general, using a double sided printed circuit card with a good ground plane on the component side is recommended. Routing analog signals between ground traces will help isolate digital control logic. If these lines cross, do so at right angles.
- Power supplies should be quiet and well regulated. Grounds should be tied together at the package and back to the system ground with a single path. Bypass the supplies at the device with a 0.01 to 0.1μF ceramic cap and a 10-47 μF tantalum type, in parallel.
- Use well-regulated and filtered power supplies.

Connection/Trimming

There are two modes of operation, each with two submodes, Unipolar, 0 to +10 V or 0 to +20 V; and Bipolar, −5 V to +5 V or −10 V to +10 V. If the accuracy of the MP574A as supplied is sufficient for the application, connect the device as shown in *Figure 1.and Figure 2.*

If greater accuracy is required, the part may be trimmed. The procedure is as follows:

Unipolar Mode: Connect MP574A as shown in *Figure 3.* R1 is used to adjust the converter offset so that an input voltage equivalent to 1/2 LSB will produce the first change in the output codes (0000 0000 0000 to 0000 0000 0001). This input is 1.22 mV for the 10 V scale (pin 13) or 2.44 mV for the 20 V scale (pin 14). Using one of these inputs, R1 should be adjusted until the output flickers between the above code values.

Having trimmed zero scale (adjusted the offset), the all −"1"s level can be set using R2 (gain adjust). Apply an input of 9.9963V to pin 13 (or 19.9927V to pin 14). This is 1.5 or 1 1/2 LSB less than 10 V (20 V). Adjust R2 until the output flickers between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Mode: In the bipolar mode the user can either adjust the ± full scale limits, or adjust the zero transition and gain (+ full scale), as is best suited to the end application.

1. To set ± full scale: Connect MP574A as shown in *Figure 4.* Apply −4.9988 V to pin 13 (or −9.9976 V to pin 14) and adjust R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Then apply +4.9963 V to pin 13 (or +9.9927 V to pin 14) and adjust R2 for flicker between output codes 1111 1111 1110 and 1111 1111 1111.
2. To set Zero Transition and Gain: Connect MP574A as shown in *Figure 4.* Apply 0.0000V to pin 13 (for +5 V full scale applications) or pin 14 (for +10 V full scale systems) and adjust R1 until the output code flickers between 0111 1111 1111 and 1000 0000 0000. Then apply +4.9963 V to pin 13 (or +9.9927 V to pin 14) and adjust R2 for flicker between output codes 1111 1111 1111 and 1111 1111 1110.

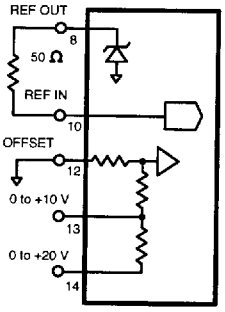

Figure 1. Unipolar Operation

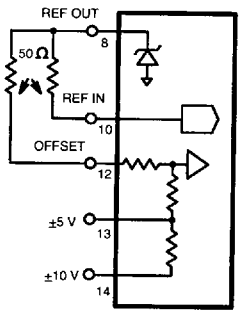

Figure 2. Bipolar Operation

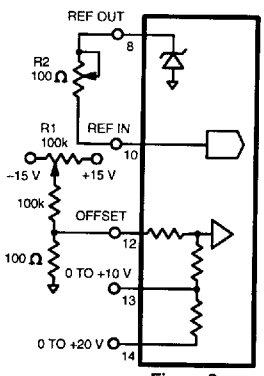

Figure 3. Unipolar Operation with Trim Adjustments

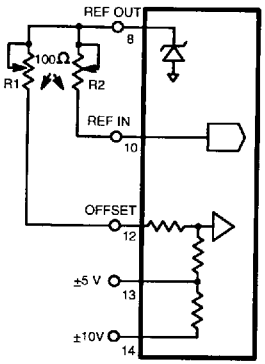

Figure 4. Bipolar Operation with Trim Adjustments

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Control and Timing Considerations

The MP574A can be operated in the stand-alone mode, with one line for control and everything else hard-wired; or under microprocessor control, where changes can be made dynamically. There are 5 control lines: CE, $\overline{CS}$, R/$\overline{C}$ Ao and 12/$\overline{8}$ with their functions described in the box "Defining the Control Functions". The role each line plays in control is shown in the MP574A Truth Table.

TRUTH TABLE

CONTROL INPUTS					MP574A OPERATION
CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A0	
0	X	X	X	X	No Operation
X	1	X	X	X	No Operation
1	0	↓	X	0	Initiates 12-Bit Conversion
1	0	↓	X	1	Initiates 8-Bit Conversion
↑	0	0	X	0	Initiates 12-Bit Conversion
↑	0	0	X	1	Initiates 8-Bit Conversion
1	↓	0	X	0	Initiates 12-Bit Conversion
1	↓	0	X	1	Initiates 8-Bit Conversion
1	0	↑	1	X	Enables 12-Bit Parallel Output
1	0	↑	0	0	Enables 8 MSB's
1	0	↑	0	1	Enables 4 LSB's and 4 Trailing Zeros

TIMING

The MP574A is easily interfaced to a wide variety of microprocessors and other digital systems. Discussion of the timing requirements of the MP574A control signals will provide the system designer with useful insight into the operation of the device.

Figure 5. shows a complete timing diagram for the MP574A convert start operation. R/$\overline{C}$ should be low before both CE and $\overline{CS}$ are asserted; If R/$\overline{C}$ is high, a read operation will momentarily occur, possibly resulting in system bus contention.

Either CE or $\overline{CS}$ may be used to initiate a conversion. We recommend using CE, however, as it includes one less propagation delay than $\overline{CS}$. As shown in *Figure 5.*, CE is used. If $\overline{CS}$ is used to trigger the conversion the specified set-up times will be longer.

Once a conversion is started and the STS line goes high, convert start commands will be ignored until the conversion cycle is completed. The output data buffers cannot be enabled during conversion. However, all inputs and outputs which change during conversion can introduce noise.

CONVERT START TIMING – FULL CONTROL MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DSC}	STS Delay from CE	–	80	200	ns
t_{HEC}	CE Pulse Width	50	40	–	ns
t_{SSC}	$\overline{CS}$ to CE Setup	50	20	–	ns
t_{HSC}	$\overline{CS}$ Low During CE High	50	25	–	ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0	–	ns
t_{HRC}	R/$\overline{C}$ Low During CE High	50	25	–	ns
t_{SAC}	A0 CE Setup	0	0	–	ns
t_{HAC}	A0 Valid During CE High	50	30	–	ns
t_C	Conversion Time 8-Bit Cycle 12-Bit Cycle	 6 12	 9 16	 15 20	 µs µs

Figure 6. shows the timing for data read operations. The MP574A features fast access times and short data latency times. This simplifies the interface to faster microprocessors. During data read operations, access time is measured from the point where CE and R/$\overline{C}$ both are high (assuming $\overline{CS}$ is already low).

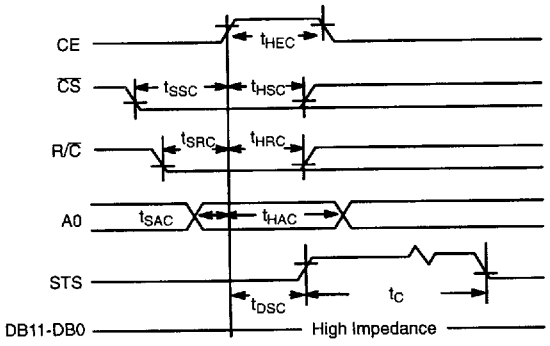

Figure 5. Convert Start Timing

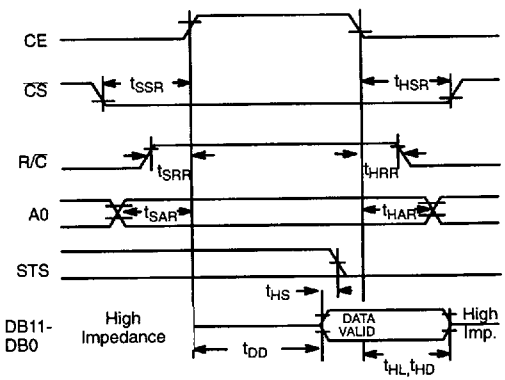

Figure 6. Read Cycle Timing

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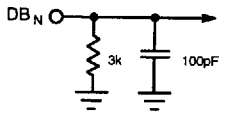
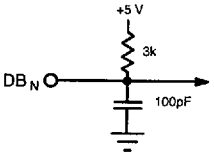
READ TIMING – FULL CONTROL MODE

Symbol	Parameter	Min	Typ	Max	Units
$t_{DD}1$	Access Time (from CE)	–	80	150	ns
t_{HD}	Data Valid after CE Low	25	35	–	ns
$t_{HL}2$	Output Float Delay	–	60	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50	0	–	ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0	0	–	ns
t_{SAR}	A0 to CE Setup	50	25	–	ns
t_{HSR}	$\overline{CS}$ Valid After CE Low	0	0	–	ns
t_{HRR}	R/$\overline{C}$ High After CE Low	0	0	–	ns
t_{HAR}	A0 Valid After CE Low	50	25	–	ns

1. t_{DD} is measured with the load circuit of *Figure 7.* and defined as the time required for an output to cross 0.4 V or 2.4 V.
2. t_{HL} is defined as the time required for the data lines to change 0.5 V when loaded with the circuit of *Figure 8.*

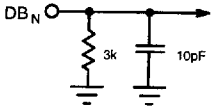


a. High-Z to Logic 1

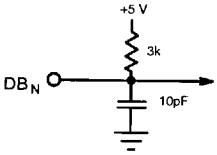


b. High-Z to Logic 0

Figure 7. Load Circuit for Access Time Test



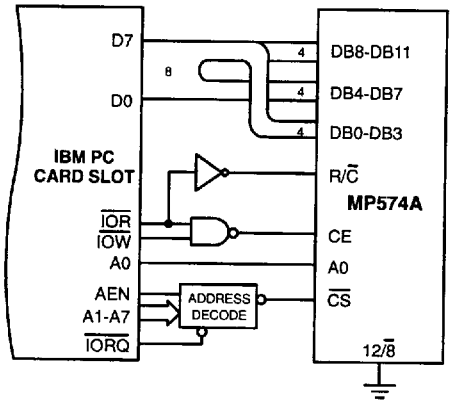
a. Logic 1 to High-Z



b. Logic 0 to High-Z

Figure 8. Load Circuit for Output Float Delay Test

IBM PC - MP574A INTERFACE



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"STAND-ALONE" OPERATION

The MP574A can be used in a "stand-alone" mode, which is useful in systems not requiring full computer bus interface capability.

In this mode, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A0 are wired low, and conversion is controlled by R/$\overline{C}$. The three-state buffers are enabled when R/$\overline{C}$ is high and a conversion starts when R/$\overline{C}$ goes low. This gives rise to two possible control signals – a high pulse or a low pulse. Operation with a low pulse is shown in *Figure 9.* In this case, the outputs are forced into the high impedance state in response to the falling edge of R/$\overline{C}$ and return to valid logic levels after the conversion cycle is completed. The STS line goes high 300 ns after R/$\overline{C}$ goes low and returns low 300 ns after data is valid.

If conversion is initiated by a high pulse as shown in *Figure 10.*, the data lines are enabled during the time when R/$\overline{C}$ is high. The falling edge of R/$\overline{C}$ starts the next conversion and the data lines return to tri-state (and remain three-state) until the next high pulse of R/$\overline{C}$.

CONDITIONING OF INPUT SIGNALS

It is important that the signal being applied to the MP574A input not change during a conversion cycle (it should be stable to within 1/2 LSB). During the successive approximation process (12 iterations), the output of the internal DAC cycles at approximately 600 kHz, until a final value is reached. Since the DAC output is tied to the device inputs (*see Block Diagram*), the input buffer should have low impedance at 600 kHz.

3

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50	30	–	ns
t_{DS}	STS Delay from R/$\overline{C}$	–	60	200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	20	25	–	ns
t_{HL}	Output Float Delay	–	100	150	ns
t_{HS}	STS Delay After Data Valid	300	–	1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150	50	–	ns
t_{DDR}	Data Access Time	–	90	150	ns

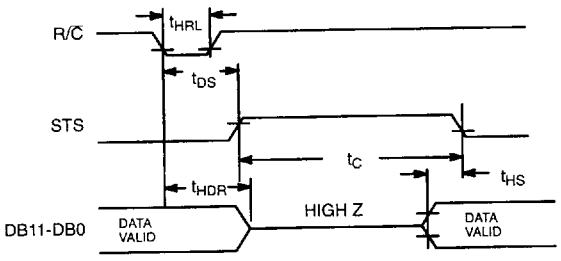

Figure 9. Low Pulse for R/$\overline{C}$ - Outputs Enabled After Conversion

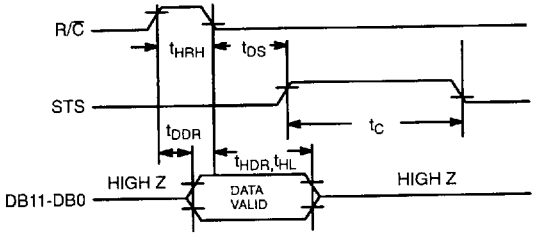

Figure 10. High Pulse for R/$\overline{C}$ - Outputs Enabled While R/$\overline{C}$ High, Otherwise High-Z