REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R143-97.	96-12-10	Monica L. Poelking
B	Incorporate Revision A. Update boilerplate to MIL-PRF-38535 requirements. – LTG	01-09-04	Thomas M. Hess
C	Add appendix A. – LTG	02-01-31	Thomas M. Hess
D	Add device types 02 and 03. Delete RHA level "H" for device type 01. Add test circuit to figure 4. Add figure B-1 to appendix A. Update boilerplate and editorial changes throughout. - LTG	04-05-26	Thomas M. Hess
E	Make corrections for pin numbers 6 and 7 in figure 1, terminal connections. Editorial changes throughout. - LTG	05-12-06	Thomas M. Hess
F	Correct radiation features in section 1.5 and add footnote 8/. Correct footnotes 2/ and 7/ in Table IA. Correct paragraph 4.4.4.1. Correct SEP test limits in the table IB. Update boilerplate paragraphs to current MIL-PRF-38535 requirements. - MAA	09-09-09	Thomas M. Hess
G	Make corrections to table IA, output voltage tests V_{OH} and V_{OL}, change condition V_{IN} - jak	11-01-26	Thomas M. Hess
H	Add footnote 5 to figure 4. Add equivalent circuit to figure 4 - jak	12-07-09	Thomas M. Hess

REV																				
SHEET																				
REV	H	H	H	H	H	H	H	H	H	H	H	H	H	H						
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28						

REV STATUS	REV	H	H	H	H	H	H	H	H	H	H	H	H	H
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Thanh V. Nguyen

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
96-04-12

REVISION LEVEL
H

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, RADIATION HARDENED, DUAL J-$\overline{K}$ FLIP-FLOP WITH CLEAR AND PRESET, MONOLITHIC SILICON

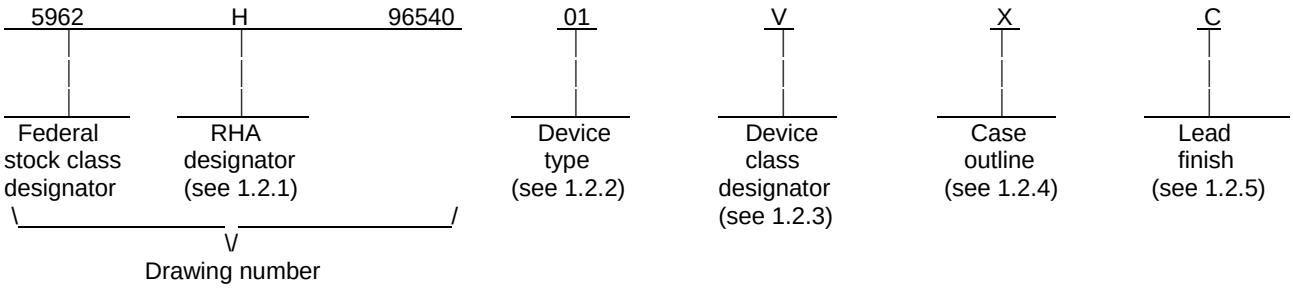
SIZE	CAGE CODE	
A	**67268**	**5962-96540**

SHEET 1 OF 28

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACS109	Radiation hardened, dual J-$\overline{K}$ flip-flop with clear and preset
02	54ACS109E	Enhanced radiation hardened, dual J-$\overline{K}$ flip-flop with clear and preset
03	54ACS109E	Enhanced radiation hardened, dual J-$\overline{K}$ flip-flop with clear and preset

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
X	CDFP4-F16	16	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{DD}) ..... -0.3 V dc to +7.0 V dc
DC input voltage range (V_{IN}) ..... -0.3 V dc to V_{DD} + 0.3 V dc
DC output voltage range (V_{OUT}) ..... -0.3 V dc to V_{DD} + 0.3 V dc
DC input current, any one input (I_{IN}) ..... ±10 mA
Latch-up immunity current (I_{LU}) ..... ±150 mA
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Lead temperature (soldering, 5 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}):
  Case outlines E and X (device type 01) ..... See MIL-STD-1835
  Case outline X (device types 02 and 03) ..... 15°C/W
Junction temperature (T_J) ..... +175°C
Maximum package power dissipation (P_D):
  Device type 01 ..... 1.0 W
  Device types 02 and 03 ..... 3.3 W 4/

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{DD}):
  Device types 02 and 03 ..... +3.0 V dc to +5.5 V dc
  Device type 01 ..... +4.5 V dc to +5.5 V dc
Input voltage range (V_{IN}) ..... +0.0 V dc to V_{DD}
Output voltage range (V_{OUT}) ..... +0.0 V dc to V_{DD}
Maximum input rise and fall time at V_{DD} = 4.5 V (t_r, t_f) ..... 1 ns/V 5/
Case operating temperature range (T_C) ..... -55°C to +125°C

1.5 Radiation features. 6/

Maximum total dose available:
  Device type 01 (dose rate = 50 – 300 rads (Si)/s) ..... 5×10^5 Rad (Si) 7/
  Device type 02 (effective dose rate = 1rad (Si)/s) ..... 1×10^6 Rad (Si) 8/
  Device type 03 (dose rate = 50 – 300 rads (Si)/s) ..... 5×10^5 Rads (Si) 7/
Single event phenomenon (SEP):
  Device type 01:
    No SEU occurs at effective LET (see 4.4.4.4) ..... ≤ 80 MeV/(mg/cm^2) 9/
    No SEL occurs at effective LET (see 4.4.4.4) ..... ≤ 120 MeV/(mg/cm^2) 9/
  Device types 02 and 03:
    No SEU occurs at effective LET (see 4.4.4.4) ..... ≤108 MeV/(mg/cm^2) 9/
    No SEL occurs at effective LET (see 4.4.4.4) ..... ≤ 120 MeV/(mg/cm^2) 9/
Dose rate upset (20 ns pulse) (device types 01, 02 and 03) ..... ≥ 1×10^9 Rads (Si)/s 9/ 10/
Dose rate induced latch-up ..... None 9/
Dose rate survivability (device types 01, 02 and 03) ..... ≥ 1×10^{12} Rads (Si)/s 9/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise specified, all voltages are referenced to V_{SS}.
3/ The limits for the parameters specified herein shall apply over the full specified V_{DD} range and case temperature range of -55°C to +125°C unless otherwise specified.
4/ Per MIL-STD-883 method 1012.1 section 3.4.1, P_D (Package) = $\dfrac{(T_J(\max) - T_C(\max))}{\theta_{JC}}$.
5/ Derate system propagation delays by difference in rise time to switch point for t_r or t_f > 1 ns/V.
6/ Radiation testing is performed on the standard evaluation circuit.
7/ Device types 01 and 03 are tested in accordance with MIL-STD-883, method 1019, condition A.
8/ Device type 02 is irradiated at dose rate = 50 - 300 rads (Si)/s in accordance with MIL-STD-883, method 1019, condition A, and is guaranteed to a maximum total dose specified. The effective dose rate after extended room temperature anneal = 1 rad (Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for this device only applies to the specified effective dose rate, or lower, environment.
9/ Limits are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.
10/ This limit is applicable for device types 01, 02, 03 with $V_{DD} \geq 4.5$ V. Device types 02 and 03 do not meet this limit at $V_{DD} < 4.5$ V.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuits. The switching waveforms and test circuits shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are described in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime 's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 38 (see MIL-PRF-38535, appendix A).

TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ Unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits 3/		Unit
						Min	Max	
High level input voltage	V_{IH}		02, 03	3.0 V	1, 2, 3	2.1		V
			All	4.5 V	1, 2, 3	3.15		
			All	5.5 V	1, 2, 3	3.85		
Low level input voltage	V_{IL}		02, 03	3.0 V	1, 2, 3		0.9	V
			All	4.5 V	1, 2, 3		1.35	
			All	5.5 V	1, 2, 3		1.65	
High level output voltage	V_{OH}	For all inputs affecting output under test, $V_{IN} = V_{DD}$ or V_{SS} For all other inputs $V_{IN} = V_{DD}$ or V_{SS} $I_{OH} = -100\ \mu A$	02, 03	3.0 V	1, 2, 3	2.75		V
		For all inputs affecting output under test, $V_{IN} = V_{DD}$ or V_{SS} For all other inputs $V_{IN} = V_{DD}$ or V_{SS} $I_{OH} = -100\ \mu A$	All	4.5 V	1, 2, 3	4.25		V
Low level output voltage	V_{OL}	For all inputs affecting output under test, $V_{IN} = V_{DD}$ or V_{SS} For all other inputs $V_{IN} = V_{DD}$ or V_{SS} $I_{OL} = +100\ \mu A$	02, 03	3.0 V	1, 2, 3		0.25	V
		For all inputs affecting output under test, $V_{IN} = V_{DD}$ or V_{SS} For all other inputs $V_{IN} = V_{DD}$ or V_{SS} $I_{OL} = +100\ \mu A$	All	4.5 V	1, 2, 3		0.25	V
Input current high	I_{IH}	For input under test, $V_{IN} = V_{DD}$ For all other inputs $V_{IN} = V_{DD}$ or V_{SS}	All	5.5 V	1, 2, 3		+1.0	µA
Input current low	I_{IL}	For input under test, $V_{IN} = V_{SS}$ For all other inputs $V_{IN} = V_{DD}$ or V_{SS}	All	5.5 V	1, 2, 3		-1.0	µA
Output current (source) 4/	I_{OH}	For output under test $V_{OUT} = V_{DD} - 0.4$ V; For all other inputs, $V_{IN} = V_{DD}$ or V_{SS}	02, 03	3.0 V and 3.6 V	1, 2, 3	-6.0		mA
		For output under test $V_{OUT} = V_{DD} - 0.4$ V; For all other inputs, $V_{IN} = V_{DD}$ or V_{SS}	All	4.5 V and 5.5 V	1, 2, 3	-8.0		mA
Output current (sink) 4/	I_{OL}	For output under test $V_{OUT} = 0.4$ V; For all other inputs $V_{IN} = V_{DD}$ or V_{SS}	All	3.0 V and 3.6 V	1, 2, 3	+6.0		mA
		For output under test $V_{OUT} = 0.4$ V; For all other inputs $V_{IN} = V_{DD}$ or V_{SS}	All	4.5 V and 5.5 V	1, 2, 3	+8.0		mA
Quiescent supply current	I_{DDQ}	$V_{IN} = V_{DD}$ or V_{SS}	All	5.5 V	1, 2, 3		10.0	µA
Short circuit output current 5/ 6/	I_{OS}	For output under test $V_{OUT} = V_{DD}$ and V_{SS}	02, 03	3.0 V	1, 2, 3		±100	mA
			All	5.5 V	1, 2, 3		±200	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ Unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Input capacitance	C_{IN}	f = 1 MHz, see 4.4.1c	All	0.0 V	4		15.0	pF
Output capacitance	C_{OUT}	f = 1 MHz, see 4.4.1c	All	0.0 V	4		15.0	pF
Switching power dissipation 7/	P_{SW}	C_L = 50pF, per switching output	02, 03	3.0 V and 3.6 V	4, 5, 6		0.8	mW/ MHz
			All	4.5 V and 5.5 V	4, 5, 6		2.0	mW/ MHz
Functional test 8/		See 4.4.1b	02, 03	3.0 V and 3.6 V	7, 8	L	H	
		See 4.4.1b	All	4.5 V and 5.5 V	7, 8	L	H	
Propagation delay time, CLKn to Qn or $\overline{Qn}$ 9/	t_{PLH1}	C_L = 30pF minimum See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	4.0	23.0	ns
			02, 03	4.5 V and 5.5 V	9, 10, 11	4.0	19.0	
		C_L = 50pF minimum See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	4.0	27.0	ns
			All	4.5 V and 5.5 V	9, 10, 11	4.0	23.0	
	t_{PHL1}	C_L = 30pF minimum See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	5.0	27.0	ns
			02, 03	4.5 V and 5.5 V	9, 10, 11	5.0	23.0	
		C_L = 50pF minimum See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	5.0	31.0	ns
			All	4.5 V and 5.5 V	9, 10, 11	5.0	27.0	
Propagation delay time, $\overline{PREn}$ to Qn 9/	t_{PLH2}	C_L = 30pF minimum See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	1.0	16.0	ns
			02, 03	4.5 V and 5.5 V	9, 10, 11	1.0	12.0	
		C_L = 50pF minimum See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	1.0	20.0	ns
			All	4.5 V and 5.5 V	9, 10, 11	1.0	16.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ Unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Propagation delay time, $\overline{PREn}$ to $\overline{Qn}$ 9/	t_{PHL2}	C_L = 30pF minimum See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	1.0	19.0	ns
			02, 03	4.5 V and 5.5 V	9, 10, 11	1.0	15.0	
		C_L = 50pF minimum See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	1.0	23.0	ns
			All	4.5 V and 5.5 V	9, 10, 11	1.0	19.0	
Propagation delay time, $\overline{CLRn}$ to $\overline{Qn}$ 9/	t_{PLH3}	C_L = 30pF minimum See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	2.0	16.0	ns
			02, 03	4.5 V and 5.5 V	9, 10, 11	2.0	12.0	
		C_L = 50pF minimum See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	2.0	20.0	ns
			All	4.5 V and 5.5 V	9, 10, 11	2.0	16.0	
Propagation delay time, $\overline{CLRn}$ to Qn 9/	t_{PHL3}	C_L = 30pF minimum See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	2.0	19.0	ns
			02, 03	4.5 V and 5.5 V	9, 10, 11	2.0	15.0	
		C_L = 50pF minimum See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	2.0	23.0	ns
			All	4.5 V and 5.5 V	9, 10, 11	2.0	19.0	
Maximum clock frequency	f_{MAX}	C_L = 50pF minimum See figure 4	02, 03	3.0 V	9, 10, 11		62.0	MHz
		C_L = 50pF minimum See figure 4	All	4.5V and 5.5 V	9, 10, 11		62.0	
Setup time, data high or low before CLKn↑	t_{S1}	C_L = 50pF minimum See figure 4	02, 03	3.0 V	9, 10, 11	5.0		ns
		C_L = 50pF minimum See figure 4	All	4.5 V and 5.5 V	9, 10, 11	5.0		
Setup time $\overline{PREn}$ or $\overline{CLRn}$, inactive before CLKn↑	t_{S2}	C_L = 50pF minimum See figure 4	02, 03	3.0 V	9, 10, 11	5.0		ns
		C_L = 50pF minimum See figure 4	All	4.5 V and 5.5 V	9, 10, 11	5.0		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ Unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Hold time, data high or low after CLKn↑ 10/	t_h	C_L = 50pF minimum See figure 4	02, 03	3.0 V	9, 10, 11	3.0		ns
		C_L = 50pF minimum See figure 4	All	4.5 V and 5.5 V	9, 10, 11	3.0		
CLKn pulse width, high or low	t_{W1}	C_L = 50pF minimum See figure 4	02, 03	3.0 V	9, 10, 11	8.0		ns
		C_L = 50pF minimum See figure 4	All	4.5 V and 5.5 V	9, 10, 11	8.0		
$\overline{PREn}$ or $\overline{CLRn}$ pulse width, low	t_{W2}	C_L = 50pF minimum See figure 4	02, 03	3.0 V	9, 10, 11	8.0		ns
		C_L = 50pF minimum See figure 4	All	4.5 V and 5.5 V	9, 10, 11	8.0		

1/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table IA herein. Output terminals not designated shall be high level logic, low level logic, or open, except for the I_{DDQ} test, the output terminals shall be open. When performing the I_{DDQ} test, the current meter shall be placed in the circuit such that all current flows through the meter.

2/ RHA device type 01 and 03 devices supplied to this drawing have been characterized through all levels M, D, P, L, R, F and G of irradiation. RHA device type 03 devices supplied to this drawing have been characterized through all levels M, D, P, L, R, F and G of irradiation.

Device type 01 is tested in accordance with MIL-STD-883, method 1019, condition A for RHA level "G".

Device type 02 is irradiated at dose rate = 50 - 300 rads (Si)/s in accordance with MIL-STD-883, method 1019, condition A, and is guaranteed to a maximum total dose specified. The effective dose rate after extended room temperature anneal = 1 rad (Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for this device only applies to the specified effective dose rate, or lower, environment. Device 02 is tested for RHA level "H".

Device type 03 is tested in accordance with MIL-STD-883, method 1019, condition A for RHA level "G".

Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A=+25°C.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to V_{SS} and the direction of current flow respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

4/ This test is guaranteed based on characterization data but not tested.

5/ This parameter is supplied as design limit but not guaranteed or tested.

6/ No more than one output should be shorted at a time for a maximum duration of one second.

7/ This value is calculated during the design/qualification process and is supplied as a design limit but is not tested. The power dissipation per switching output (P_{SW}) is calculated for a logic device by using power dissipation equation P_{TOTAL}. To determine total power use the formula:

$P_{TOTAL} = (N_{SWO} \times P_{SW/OUTPUT} \times f)$ Wherein, N_{SWO} = number of switching outputs, $P_{SW/OUTPUT}$ = Power dissipation per switching output in mW/MHz from Table IA and f is the operating frequency that the outputs are switching.

TABLE IA. Electrical performance characteristics – Continued.

8/ The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. For V_{OUT} measurements, L ≤ 0.5 V and H ≥ 4.0 V and are tested at V_{DD} = 4.5 V and V_{DD} = 5.5 V; L ≤ 0.5 V and H ≥ 2.5 V and are tested at V_{DD} = 3.0 V and V_{CC} = 3.6 V.

9/ For propagation delay tests, all paths must be tested.

10/ Based on characterization, hold time (t_h) of 0 ns can be assumed if the data setup time (t_{S1}) is ≥ 10 ns. This is guaranteed but not tested.

TABLE IB. SEP test limits. 1/ 2/

Device type	V_{DD} = 4.5 V for device type 01 3/ V_{DD} = 3.0 V for device types 02 and 03		Bias for Latch-up test V_{DD} = 5.5 V no latch-up LET = 4/ 5/ [MeV/(mg/cm^2)]
	Effective LET no upsets [MeV/(mg/cm^2)]	Maximum device cross section	
01	LET ≤ 80	6 x 10^{-9} cm^2/bit 6/	≤ 120
02, 03	LET ≤ 108	7/	≤ 120

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Tested for upsets at operating temperature, T_A = +25°C ± 10°C.
4/ Tested at operating temperature, T_A = +125°C ± 10°C for latch-up.
5/ Tested to LET of ≥ 120 MeV/(mg/cm^2) with no latch-up (SEL).
6/ The bit error cross section is established from a “hard” D flip-flop that is based on the Weibull distribution from SEU testing, and is performed on the Standard Evaluation Circuit (SEC).
7/ Tested to LET of ≥ 120 MeV/(mg/cm^2) with no single event upsets (SEU).

Device type	All		
Case outlines	E and X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{CLR1}$	9	$\overline{Q2}$
2	J1	10	Q2
3	$\overline{K1}$	11	$\overline{PRE2}$
4	CLK1	12	CLK2
5	$\overline{PRE1}$	13	$\overline{K2}$
6	Q1	14	J2
7	$\overline{Q1}$	15	$\overline{CLR2}$
8	V_{SS}	16	V_{DD}

FIGURE 1. Terminal connections.

Inputs					Outputs	
$\overline{PREn}$	$\overline{CLRn}$	CLKn	Jn	$\overline{Kn}$	Qn	$\overline{Qn}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H 1/	H 1/
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	Toggle
H	H	↑	L	H	No change	No change
H	H	↑	H	H	H	L
H	H	L	X	X	No change	No change

H = High voltage level
L = Low voltage level
X = Irrelevant
↑ = Low-to-high clock transition
1/ The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} maximum. In addition, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

FIGURE 2. Truth table.

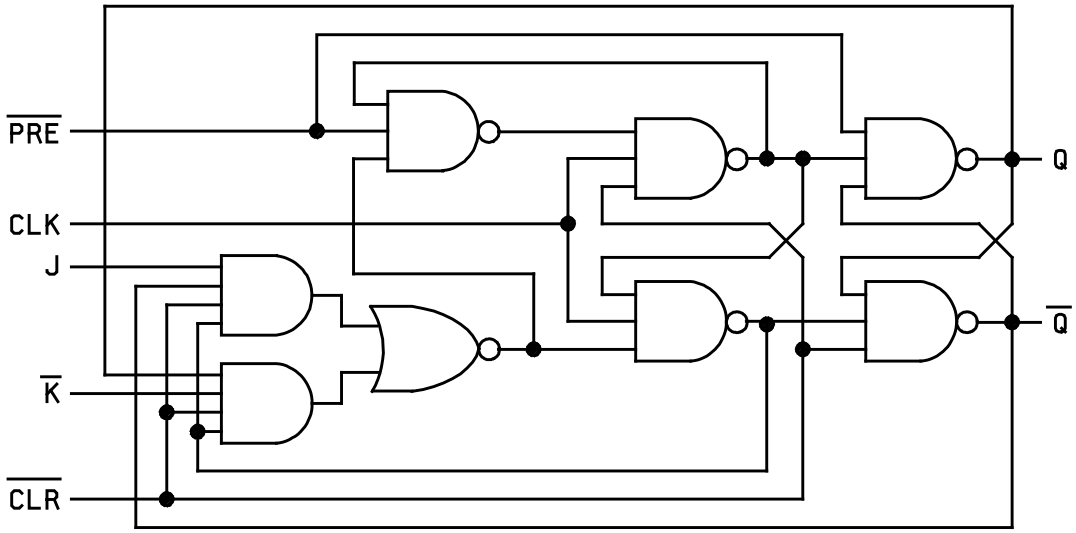


FIGURE 3. Logic diagram.

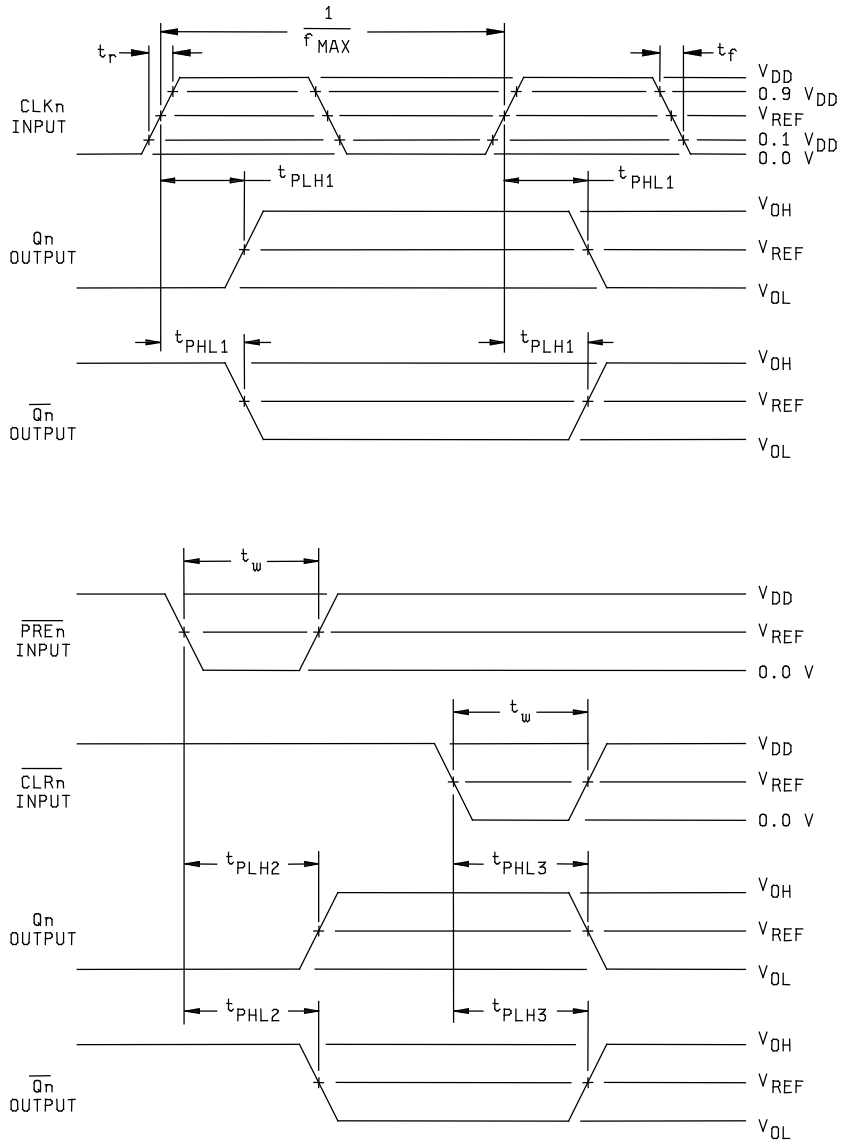
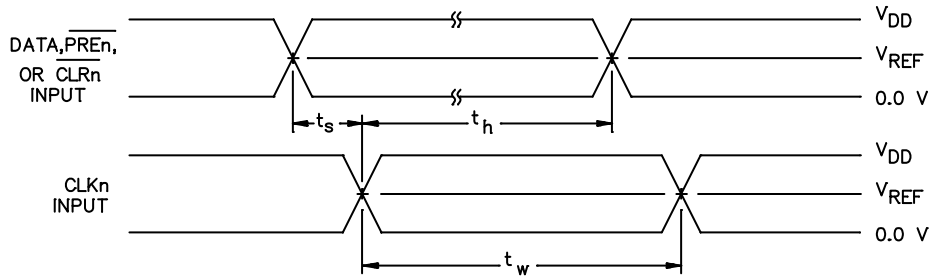
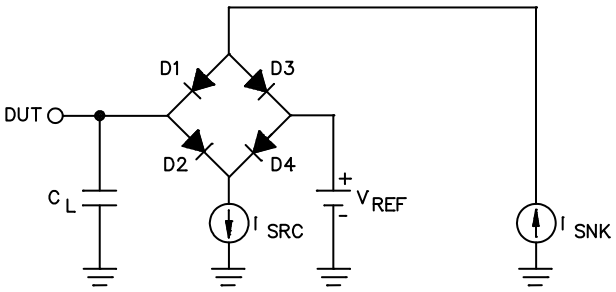
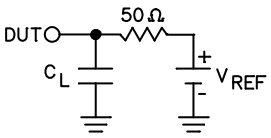


FIGURE 4. Switching waveforms and test circuits.





TEST CIRCUIT A
OR EQUIVALENT



TEST CIRCUIT B
OR EQUIVALENT

NOTES:
1. $V_{REF} = V_{DD}/2$.
2. C_L = 50 pF or 30 pF minimum or equivalent (includes test jig and probe capacitance).
3. I_{SRC} is set to -1.0 mA and I_{SNK} is set to 1.0 mA for t_{PHL} and t_{PLH} measurements. Note, either test circuit A or B may be used for these measurements.
4. Input signal from pulse generator: V_{IN} = 0.0 V to V_{DD}; f ≤ 10 MHz; t_r = 1.0 V/ns ±0.3 V/ns; t_f = 1.0 V/ns ±0.3 V/ns; t_r and t_f shall be measured from 0.1 V_{DD} to 0.9 V_{DD} and from 0.9 V_{DD} to 0.1 V_{DD}, respectively.
5 Equivalent test circuit means that DUT performance will be correlated and remain guaranteed to the applicable test circuit, above, whenever a test platform change necessitates a deviation from the applicable test circuit.

FIGURE 4. Switching waveforms and test circuits - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} and C_{OUT} shall be measured only for the initial test and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz. For C_{IN} and C_{OUT}, test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein.

4.4.4.1.1 Accelerated annealing testing. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latch-up testing. When required by the customer, dose rate induced latch-up testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing for class M devices shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11 3/
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 2, 3, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1 and 7.
2/ PDA applies to subgroups 1, 7, and delta's.
3/ Delta limits, as specified in table IIB herein, shall be required where specified, and the delta values shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameters	Symbol	Delta limits
Output voltage low	V_{OL}	±100 mV
Output voltage high	V_{OH}	±100 mV

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related an effects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 microns in silicon.

e. The upset test temperature shall be +25°C. The latchup test temperature shall be at the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990 or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEU).

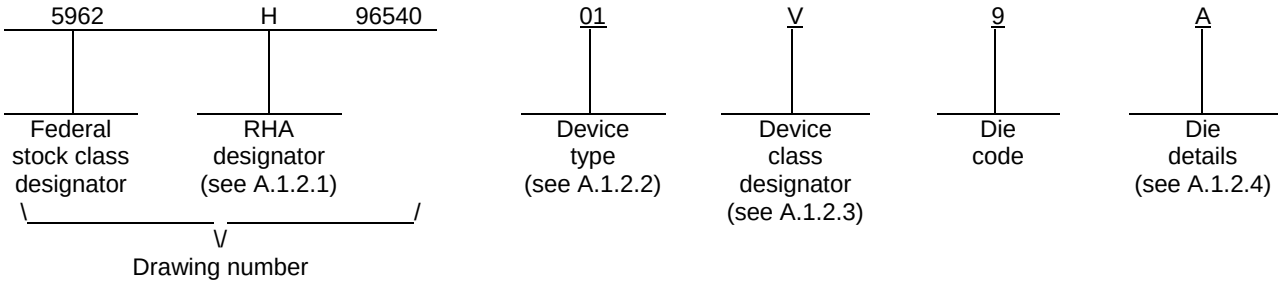
d. Number of transients (SET).

e. Occurrence of latchup (SEL).

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACS109	Radiation hardened, dual J-$\overline{K}$ flip-flop with clear and preset
02	54ACS109E	Enhanced radiation hardened, dual J-$\overline{K}$ flip-flop with clear and preset
03	54ACS109E	Enhanced radiation hardened, dual J-$\overline{K}$ flip-flop with clear and preset

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1, B-1
02	B-1
03	B-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1, B-1
02	B-1
03	B-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1, B-1
02	B-1
03	B-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1, B-1
02	B-1
03	B-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specifications, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

A.2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figures A-1 and B-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figures A-1 and B-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figures A-1 and B-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figures A-1 and B-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

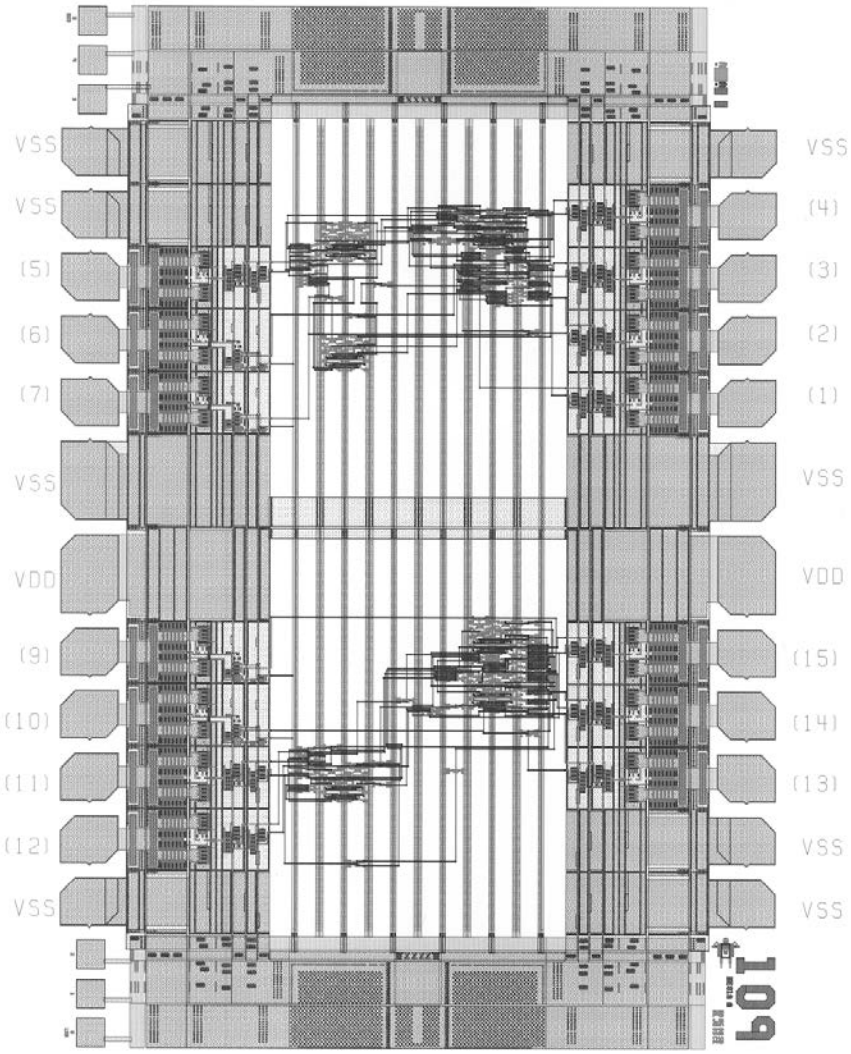
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614) 692-0547.

A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.



NOTE: Pad numbers reflect terminal numbers when placed in case outlines E and X (see figure 1).

FIGURE A-1. Die bonding pad locations and electrical functions

Die physical dimensions.

Die size:	111 x 81 mils
Die thickness:	17 ±1 mils

Interface materials.

Top metallization:	Si Al Cu
Thickness	9.0kÅ – 12.5kÅ
Backside metallization:	None

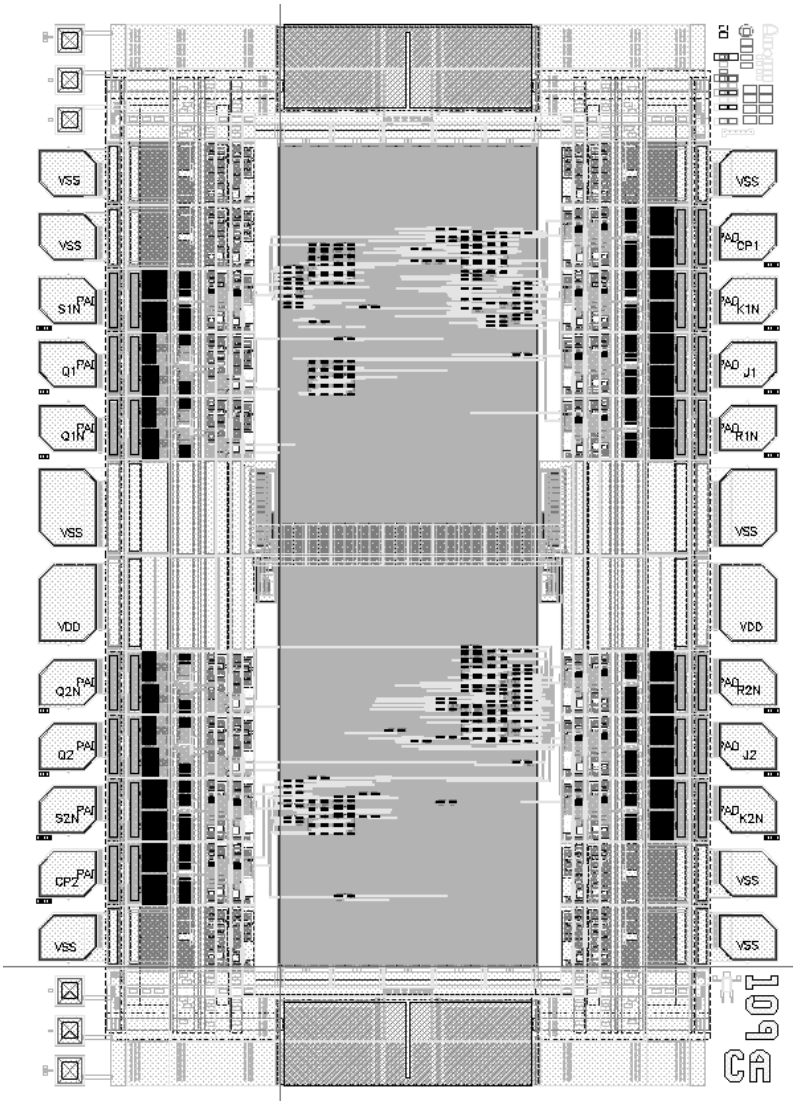
Glassivation.

Type:	PSG
Thickness:	9.0kÅ – 11.0kÅ
Substrate:	Epitaxial Layer on Single Crystal Silicon

Assembly related information.

Substrate potential:	Tied to V_{DD}
Special assembly instructions:	Bond finger #16 (V_{DD}) first. Do not wire bond the six probe ID pads.

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.



NOTE: Pad numbers reflect terminal numbers when placed in case outline X (see figure 1).

FIGURE B-1. Die bonding pad locations and electrical functions.

Die physical dimensions.

Die size:	111 x 81 mils
Die thickness:	17 ±1 mils

Interface materials.

Top metallization:	Si Al Cu
Thickness	9.0kÅ – 12.5kÅ
Backside metallization:	None

Glassivation.

Type:	Nitride
Thickness:	9.0kÅ – 11.0kÅ
Substrate:	Epitaxial Layer on Single Crystal Silicon

Assembly related information.

Substrate potential:	Tied to V_{SS}
Special assembly instructions:	Bond finger #8 (V_{SS}) first. Do not wire bond the six probe ID pads.

FIGURE B-1. Die bonding pad locations and electrical functions - Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 12-07-09

Approved sources of supply for SMD 5962-96540 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H9654001Q9A	3/	54ACS109
5962H9654001QEA	3/	54ACS109
5962H9654001V9A	3/	54ACS109
5962H9654001VEA	3/	54ACS109
5962G9654001Q9B	65342	UT54ACS109-Q-DIE
5962G9654001QXA	65342	UT54ACS109UQAG
5962G9654001QXC	65342	UT54ACS109UQCG
5962G9654001V9B	65342	UT54ACS109-V-DIE
5962G9654001VXA	65342	UT54ACS109UVAG
5962G9654001VXC	65342	UT54ACS109UVCG
5962H9654002Q9B	65342	UT54ACS109E-Q-DIE
5962H9654002QXA	65342	UT54ACS109EUQAH
5962H9654002QXC	65342	UT54ACS109EUQCH
5962H9654002V9B	65342	UT54ACS109E–V-DIE
5962H9654002VXA	65342	UT54ACS109EUVAH
5962H9654002VXC	65342	UT54ACS109EUVCH
5962G9654003Q9B	65342	UT54ACS109E-Q-DIE
5962G9654003QXA	65342	UT54ACS109EUQAG
5962G9654003QXC	65342	UT54ACS109EUQCG
5962G9654003V9B	65342	UT54ACS109E-V-DIE
5962G9654003VXA	65342	UT54ACS109EUVAG
5962G9654003VXC	65342	UT54ACS109EUVCG

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

DATE:

Vendor CAGE number	Vendor name and address
65342	Aeroflex Colorado Springs, Inc. 4350 Centennial Boulevard Colorado Springs, Colorado 80907-3486