P54/74FCT651T/AT/CT — P54/74FCT652T/AT/CT OCTAL TRANSCEIVER/REGISTER

FEATURES

- Function, Pinout and Drive Compatible with the FCT and F Logic
- FCT-C speed at 5.4ns max. (Com'l) FCT-A speed at 6.3ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Power-off disable feature
- Matched Rise and Fall times
- Fully Compatible with TTL Input and Output Logic Levels
- 64 mA Sink Current (Com'l), 48 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)
- Independent Register for A and B Buses
- Multiplexed Real-Time and Stored Data Transfer
- Bidirectional Bus Transceiver and Registers
- Manufactured in 0.7 micron PACE Technology™

DESCRIPTION

THE 'FCT651T and 'FCT652T consist of bus tranciever circuits, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. GAB and $\overline{GBA}$ control pins are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data and a high selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{GBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

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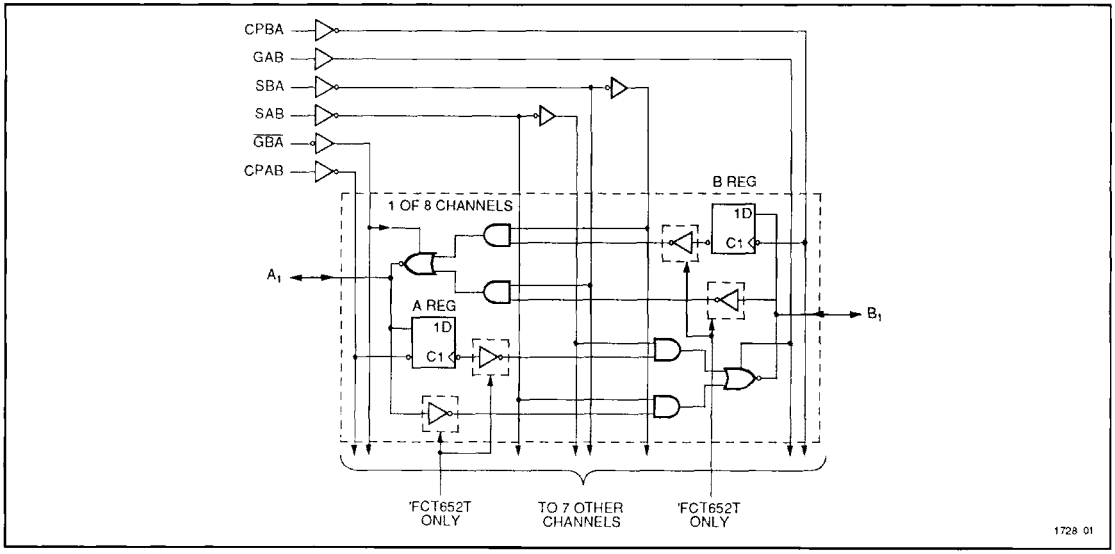
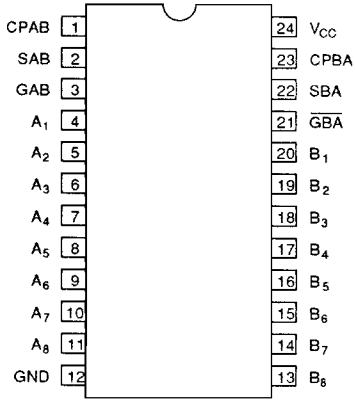
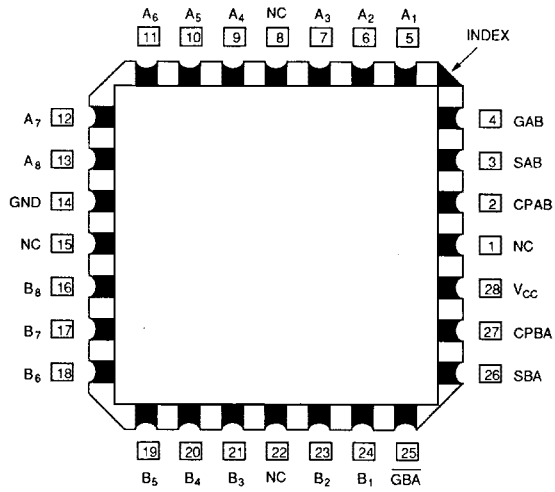
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP (D4, P4)
SOIC (S4)



LCC (L5-1)

1727 02

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1728 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1728 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1728 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1728 Tbl 04

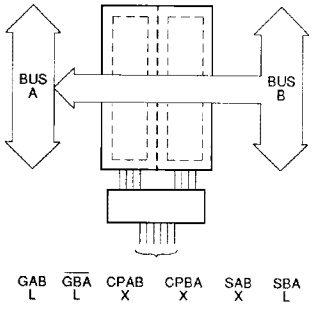
DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis[3]			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.55	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.55	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current (Except I/O Pins)				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current (Except I/O Pins)				–5	µA	MAX	V_{IN} = 0.5V
I_{IH}	Input HIGH Current (I/O Pins only)				15	µA	MAX	V_{OUT} = 2.7V
I_{IL}	Input LOW Current (I/O Pins only)				–15	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
$C_{I/O}$	I/O Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1728 Tbl 05

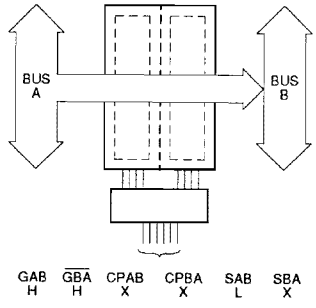
Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.



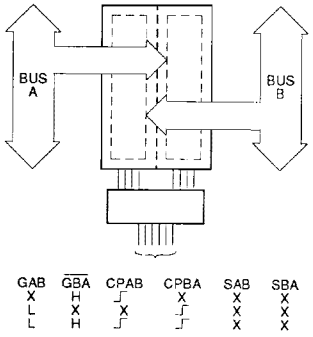
REAL-TIME TRANSFER BUS B TO BUS A

1727 03



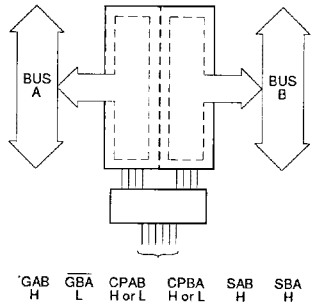
REAL-TIME TRANSFER BUS A TO BUS B

1727 04



STORAGE FROM A AND/OR B

1727 05



TRANSFER STORED DATA TO A AND/OR B

1727 06

Note:
1. Cannot transfer data to A bus and B bus simultaneously.

FUNCTION TABLES

Inputs						Data I/O		Operation or Function	
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_1 thru A_8	B_1 thru B_8	'FCT651T	'FCT652T
L L	H H	H or L ↓	H or L ↓	X X	X X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data
X H	H H	↓ ↓	H or L ↓	X X[2]	X X	Input Input	Unspecified[1] Output	Store A, Hold B Store A in both registers	Store A, Hold B Store A in both registers
L L	X L	H or L ↓	↓ ↓	X X	X X[2]	Unspecified[1] Output	Input Input	Hold A, Store B Store B in both registers	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real-Time $\overline{B}$ Data to A Bus Stored $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus Stored B Data to A Bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real-Time $\overline{A}$ Data to B Bus Stored $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored B Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

Notes:

1728 Tbl 06

1. The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.
   H = HIGH, L = LOW, X = Don't Care, ↓ LOW-to-HIGH Transition

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open GAB = GND, $\overline{GBA}$ = GND, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, GAB = GND, $\overline{GBA}$ = GND, SAB = CPAB = GND, SBA = V_{CC}, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, GAB = GND, $\overline{GBA}$ = GND, SAB = CPAB = GND, SBA = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND
		7.0	12.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 5MHz, GAB = $\overline{GBA}$ = GND, SAB = CPAB = GND, SBA = V_{CC}, V_{IN} = 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		9.2	21.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 5MHz, GAB = $\overline{GBA}$ = GND, SAB = CPAB = GND, SBA = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND

1728 Tbl 07

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} * D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

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AC CHARACTERISTICS

Symbol	Parameter	'FCT651T/652T				'FCT651AT/652AT				'FCT651CT/652CT				Units	Fig. No.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	2.0	11.0	2.0	9.0	2.0	7.7	2.0	6.3	1.5	6.0	1.5	5.4	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus	2.0	15.0	2.0	14.0	2.0	10.5	2.0	9.8	1.5	8.9	1.5	7.8	ns	1, 5
t_{PHZ} t_{PLZ}	Output Disable Time Enable to Bus	2.0	11.0	2.0	9.0	2.0	7.7	2.0	6.3	1.5	7.7	1.5	6.3	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	2.0	10.0	2.0	9.0	2.0	7.0	2.0	6.3	1.5	6.3	1.5	5.7	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	2.0	12.0	2.0	11.0	2.0	8.4	2.0	7.7	1.5	7.0	1.5	6.2	ns	1, 7, 8

1728 Tbl 08

Note:
1. AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.

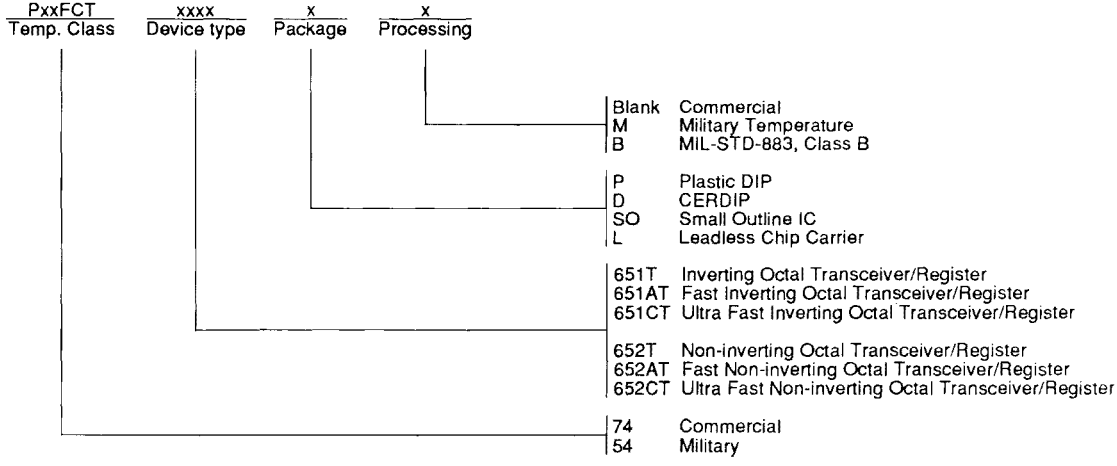
AC OPERATING REQUIREMENTS

Symbol	Parameter	'FCT651T/652T				'FCT651AT/652AT				'FCT651CT/652CT				Units	Fig. No.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_s(H) t_s(L)	Setup Time HIGH or LOW Bus to Clock	4.5	—	4.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	1, 4
t_h(H) t_h(L)	Hold Time HIGH or LOW Bus to Clock	2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	1, 4
t_w(H) t_w(L)	Clock Pulse Width, HIGH or LOW	6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns	1, 5

1728 Tbl 09

Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. With one data channel toggling, t_w(L) = t_w(H) = 4.0ns and t_r = t_f = 1.0ns.

ORDERING INFORMATION



1728 07