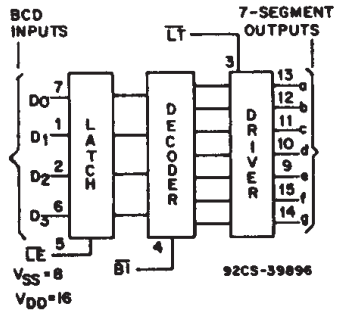
File Number 1786

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS279

CD54/74HC4511
CD54/74HCT4511

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

BCD-to-7 Segment Latch/ Decoder/Drivers

Type Features:

- *High-output sourcing capability–7.5 mA @ 4.5 V, 10 mA @ 6 V (HC4511)*
- *Input latches for BCD code storage*
- *Lamp test and blanking capability*

The RCA CD54/74HC4511 and CD54/74HCT4511 are BCD-to-7 segment latch/decoder/drivers having four address inputs (D_0-D_3), active "Low" blanking and lamp test inputs, and a latch enable input which, when "High", enables the latches to store the BCD inputs. When Latch Enable is "Low", the latches are disabled, making the outputs transparent to the BCD inputs.

These devices have standard-size output transistors but are capable of sourcing (at standard V_{OH} levels) up to 7.5 mA at 4.5 V. The HC types can supply up to 10 mA at 6 V.

The CD54HC/HCT4511 are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT4511 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

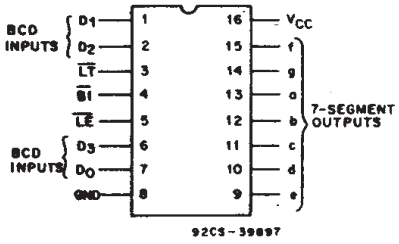
TRUTH TABLE

$\overline{LE}$	$\overline{BI}$	$\overline{LT}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	Display
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	Blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	Blank
H	H	H	X	X	X	X								

X = Don't Care
*Depends on BCD code previously applied when $\overline{LE}$ = L
Note: Display is blank for all illegal input codes (BCD > HLLH)

Family Features:

- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: −40 to +85°C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity:
  N_{IL}=30%, N_{IH}=30% of V_{CC}; @ V_{CC}=5 V
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  V_{IL}=0.8 V max., V_{IH}=2 V min.
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

This data sheet is applicable to the CD54HC4511 and CD74HCT4511. The CD54HCT4511 was not acquired from Harris Semiconductor. See SCHS214 for information on the CD74HCT4511.

CD54/74HC4511
CD54/74HCT4511

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O <$ V_{CC} +0.5 V) ..... ±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = −55 to +100°C (PACKAGE TYPE F,H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F,H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = −40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F,H ..... −55 to +125°C
PACKAGE TYPE E,M ..... −40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

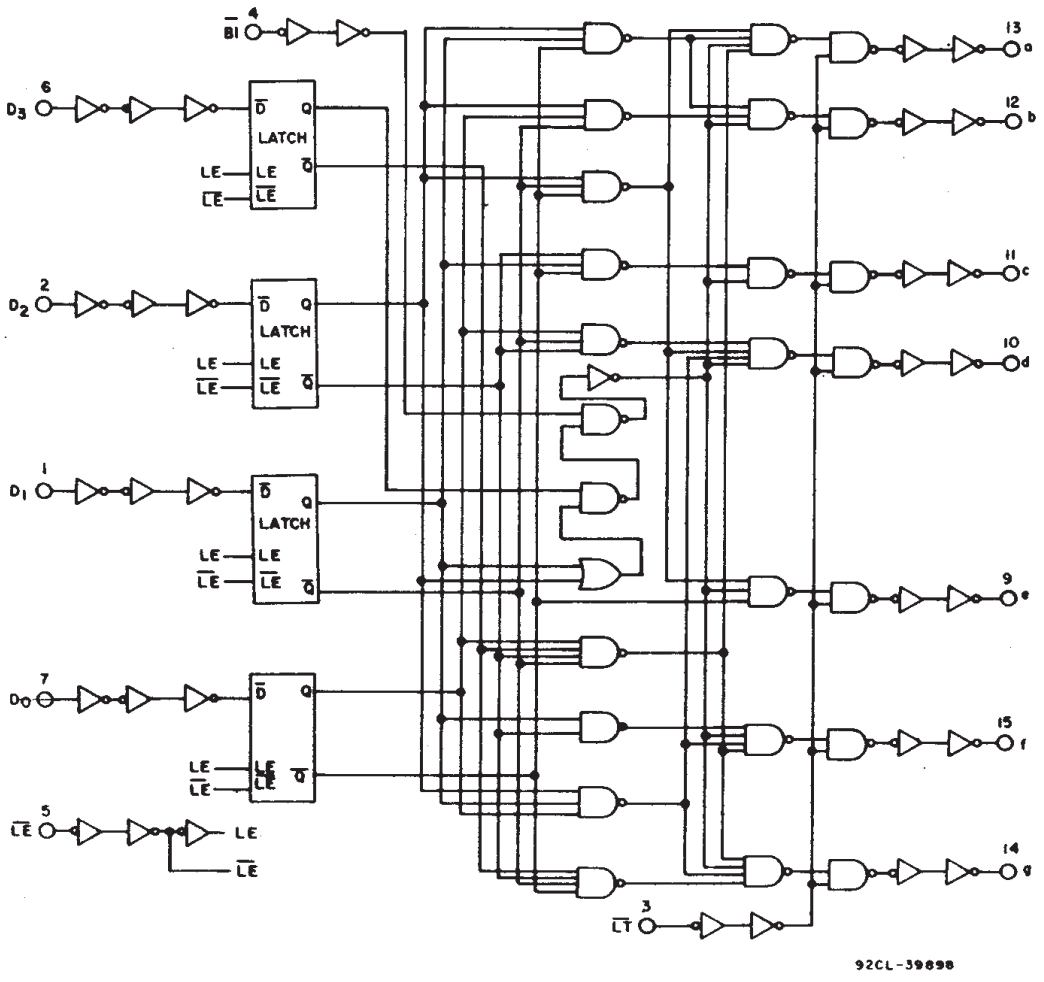


Fig. 1 - Logic diagram.

CD54/74HC4511
CD54/74HCT4511

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4511/CD54HC4511										CD74HCT4511/CD54HCT4511									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads Non-Standard Output	V_{IL} or V_{IH}	-7.5	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-10	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads Standard Output	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
$\overline{LT}$, $\overline{LE}$	1.5
$\overline{BI}$, Dn	0.3

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC4511
CD54/74HCT4511

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r,t_f=6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay:	t_{PLH}	15	25	25	ns
D_n to Output	t_{PHL}				
	t_{PLH}	15	23	23	
$\overline{LE}$ to Output	t_{PHL}				
	t_{PLH}	15	18	18	
$\overline{BI}$ to Output	t_{PHL}				
	t_{PLH}	15	13	13	
$\overline{LT}$ to Output	t_{PHL}				
Power Dissipation Capacitance*	C_{PD}	—	114	110	pF

*C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where f_i = input frequency

f_o = output frequency

C_L = output load capacitance

V_{CC} = supply voltage.

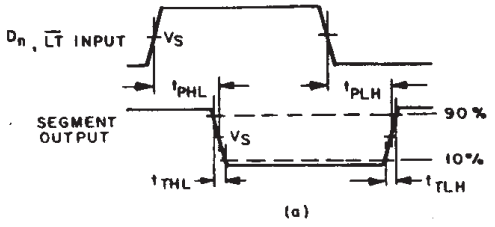
PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITIONS	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
	V_{CC} (V)	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Setup Time, t_{SU}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
D_n to $\overline{LE}$	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
	6	14	—	—	—	17	—	—	—	20	—	—	—	
Hold Time, t_H	2	3	—	—	—	3	—	—	—	3	—	—	—	
D_n to $\overline{LE}$	4.5	3	—	5	—	3	—	5	—	3	—	5	—	
	6	3	—	—	—	3	—	—	—	3	—	—	—	
Latch Enable	2	80	—	—	—	100	—	—	—	120	—	—	—	MHz
Pulse Width, t_W	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
	6	14	—	—	—	17	—	—	—	20	—	—	—	

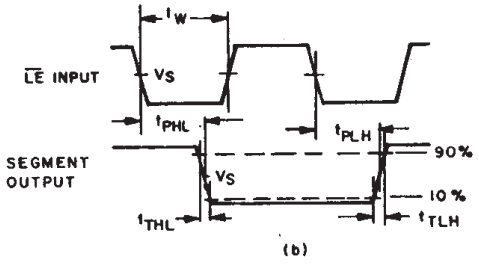
CD54/74HC4511
CD54/74HCT4511

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

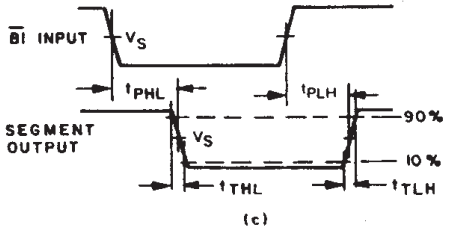
CHARACTERISTIC		V_{CC}	LIMITS												UNITS
			25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, D_n to Output	t_{PLH}	2	—	300	—	—	—	375	—	—	—	450	—	—	ns
	t_{PHL}	4.5	—	60	—	60	—	75	—	75	—	90	—	90	
		6	—	51	—	—	—	64	—	—	—	77	—	—	
$\overline{LE}$ to Output	t_{PLH}	2	—	270	—	—	—	340	—	—	—	405	—	—	ns
	t_{PHL}	4.5	—	54	—	54	—	68	—	68	—	81	—	81	
		6	—	46	—	—	—	58	—	—	—	69	—	—	
$\overline{BI}$ to Output	t_{PLH}	2	—	220	—	—	—	275	—	—	—	330	—	—	ns
	t_{PHL}	4.5	—	44	—	44	—	55	—	55	—	66	—	66	
		6		37	—	—	—	47	—	—	—	56	—	—	
$\overline{LT}$ to Output	t_{PLH}	2	—	160	—	—	—	200	—	—	—	240	—	—	ns
	t_{PHL}	4.5	—	32	—	33	—	40	—	41	—	48	—	50	
		6	—	27	—	—	—	34	—	—	—	41	—	—	
Transition Time	t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



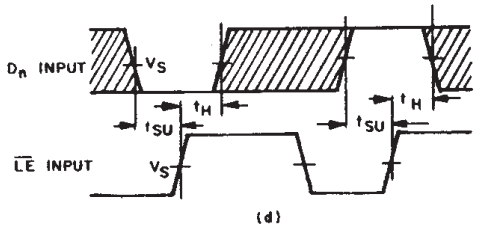
Input (Dn, $\overline{LT}$) to output propagation delays and output transition times



Input ($\overline{LE}$) to output propagation delays and latch enable pulse width



Input ($\overline{BI}$) to output propagation delays.



Note

The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveforms showing the data set-up and hold times for Dn input to $\overline{LE}$ input.

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

92CM-39899

Fig. 2 - AC waveforms.

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CD74HC4511, High Speed CMOS Logic BCD-to-7 Segment Latch/Decoder/Driver

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	CD54HC4511
Voltage Nodes (V)	6, 5, 2

FEATURES

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- High-output sourcing capability - 7.5 Ma @ 4.5 v, 10 mA @6 v (HC4511)
- Input latches for BCD code storage
- Lamp test and blanking capability
- Fanout (over temperature range):
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
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  CD74HC/HCT: -40 to +85°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- Alternate source is Philips/Signetics
- CD54HC/CD74HC types:
  2 TO 6 V operation
  High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- CD54HCT/CD74HCT types:
  4.5 TO 5.5 V operation
  Direct LSTTL input logic compatibility - V_{IL} = 0.8 V max,. V_{IH}=2 V min.
  CMOS input compatibility - $I_I \leq 1$ uA @ V_{OL}, V_{OH}

DESCRIPTION

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The RCA CD54/74HC4511 and CD54/74HCT4511 are BCD-to-7 segment latch/decoder/drivers having four address inputs (D_0-D_3), active "Low" blanking and lamp test inputs, and a latch enable input which, when "High", enables the latches to store the BCD inputs. When Latch Enable is "Low", the latches are disabled, making the outputs transparent to the BCD inputs.

These devices have standard-size output transistors but are capable of sourcing (at standard V_{OH} levels) up to 7.5 mA at 4.5 V. The HC types can supply up to 10 mA at 6 V.

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TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: cd74hc4511.pdf (183 KB) (Updated: 12/02/1998)

APPLICATION NOTES

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View Application Notes for Digital Logic

- CMOS Power Consumption and CPD Calculation (Rev. B) (SCAA035B - Updated: 06/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C - Updated: 02/01/1998)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- SN54/74HCT CMOS Logic Family Applications and Restrictions (SCLA011 - Updated: 05/01/1996)
- Selecting the Right Texas Instruments Signal Switch (SZZA030 - Updated: 09/07/2001)
- Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc (SCLA008 - Updated: 04/01/1996)

RELATED DOCUMENTS

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View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

SAMPLES

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ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
CD74HC4511M	SOP (D)	16	-55 TO 125	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE|PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY|DATE	LEAD TIME	DISTRIBUTOR COMPANY|REGION	IN STOCK	PURCHASE
CD74HC4511E	ACTIVE	PDIP (N) | 16	-55 TO 125	View Contents	1KU | 0.41	25	N/A*	>10k | 19 Sep	2 WKS			
								31 | 25 Sep				
								4000 | 03 Oct				
								>10k | 07 Oct				
								>10k | 14 Oct				
CD74HC4511M	ACTIVE	SOP (D) | 16	-55 TO 125	View Contents	1KU | 0.41	40	N/A*	80 | 19 Sep	2 WKS	Avnet | AMERICA	230	BUY NOW
								2922 | 30 Sep				
								440 | 03 Oct				
								>10k | 08 Oct				
CD74HC4511M96	ACTIVE	SOP (D) | 16	-55 TO 125	View Contents	1KU | 0.41	2500	N/A*	>10k | 14 Oct	3 WKS			

CD74HC4511PWR	ACTIVE	TSSOP (PW) | 16	-55 TO 125	View Contents	1KU | 0.41	2000	N/A*	>10k | 03 Oct	2 WKS			
								>10k | 10 Oct				

Table Data Updated on: 9/26/2002