4 DIMM Desktop System Clock

Features

- Generates system clocks for 2.5/3.3V based designs:
  - 5 CPU Clocks with 2.5V output swing
  - 16 SDRAM clocks; supports up to four 168 pin DIMM modules
  - 7 PCI clocks
  - 2 IOAPIC clocks; supports dual processor applications
  - 2 REF clocks
  - 1 48MHz clock
  - 1 24MHz clock
- Serial control interface (SDATA, SCLOCK inputs) provides additional CPU/CPI clock frequency selections, individual output clock disabling and other functions
- Separate supply pins for CPU and IOAPIC output buffers:
  - VDDQ2 = 2.5V+/-5%
  - VDD and VDDQ3 = 3.3V+/-5%
- No power supply sequence requirements
- Uses external 14.318MHz crystal
- Low frequency test mode
- Available in 56-pin SSOP (300 mils)

Figure 1 Block Diagram

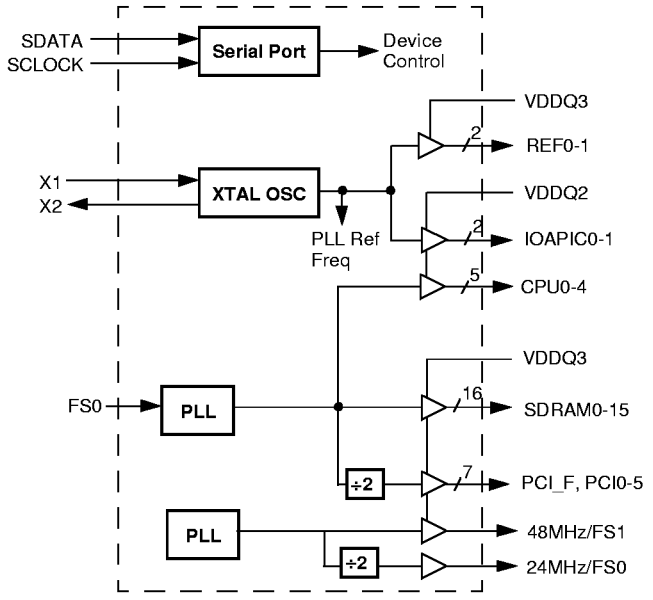


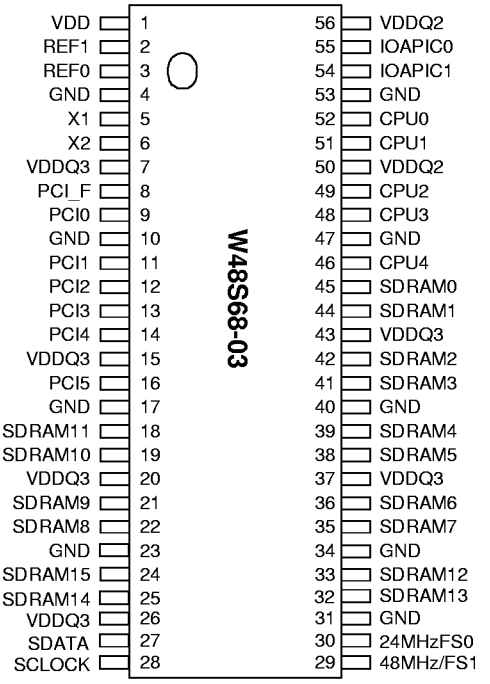
Table 1 Order Information

Part Number	Freq. Mask Code	Package
W48S68	03	H = SSOP (300 mils)

Table 2 Pin Selectable Frequency

Input Address		CPU, SDRAM Clocks (MHz)	PCI Clocks (MHz)
FS1	FS0		
0	0	83.3	41.7
0	1	75.0	37.5
1	0	60	30
1	1	66.8	33.4

Figure 2 Pin Diagram



Overview

The W48S68-03, a motherboard clock synthesizer, can provide either a 2.5V or 3.3V CPU clock swing making it suitable for a variety of CPU options. Sixteen SDRAM clocks are provided in phase with the CPU clock outputs. This provides clock support for up to four SDRAM DIMMs. A fixed 48MHz clock is provided for other system functions.

Functional Description

I/O Pin Operation

Pin 29 is a dual purpose I/O pin. Upon power up this pin acts as a logic input, allowing the determination of assigned device functions. A short time after power up, the logic state of the pin is latched and the pin then becomes a clock output. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10 kohm "strapping" resistor is connected between each I/O pin and ground or VDDQ3. Connection to ground sets a "0" bit, connection to VDDQ3 sets a "1" bit. Figure 3 and Figure 4 show two suggested methods for strapping resistor connection.

Upon W48S68-03 power up, the first 2ms of operation is used for input logic selection. During this period, the 48MHz clock output buffer is tristated, allowing the output strapping resistor on each I/O pin to pull the pin and its associated capacitive clock load to either a logic high or low state. At the end of the 2ms period, the established logic 0 or 1 condition of each I/O pin is then latched. Next the output buffer is enabled which converts the I/O pin into operating clock output. The 2ms timer is started when VDD reaches 2.0V. The input bits can only be re-set by turning VDD off and then back on again.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of both clock outputs is 40 ohms (nominal) which is minimally affected by the 10 kohm strap to ground or VDD. As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or VDD should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

When the clock outputs are enabled following the 2ms input period, target (normal) output frequency is delivered assuming that VDD has stabilized. If VDD has not yet reached full value, output frequency initially may be below target but will increase to target once VDD voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.

Figure 3 Input Logic Selection Through Resistor Load Option

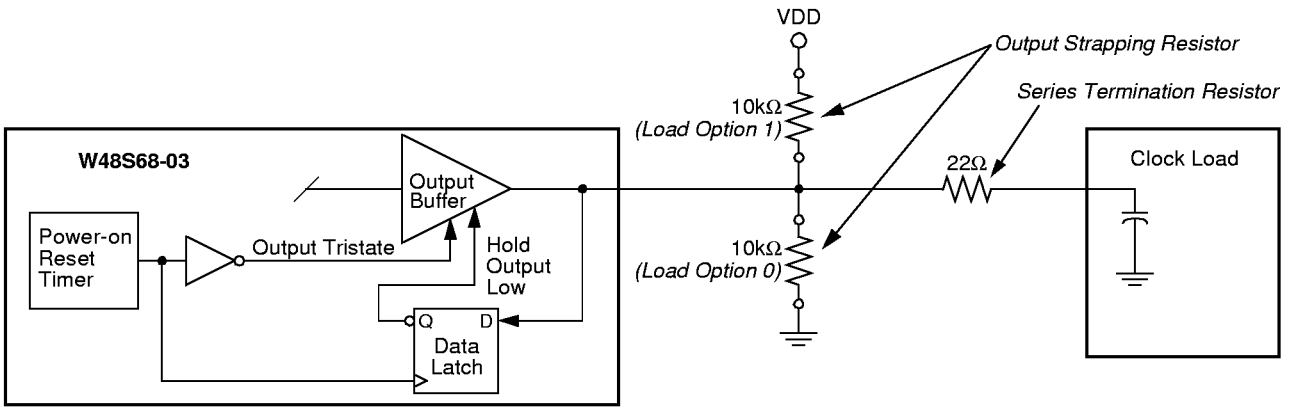
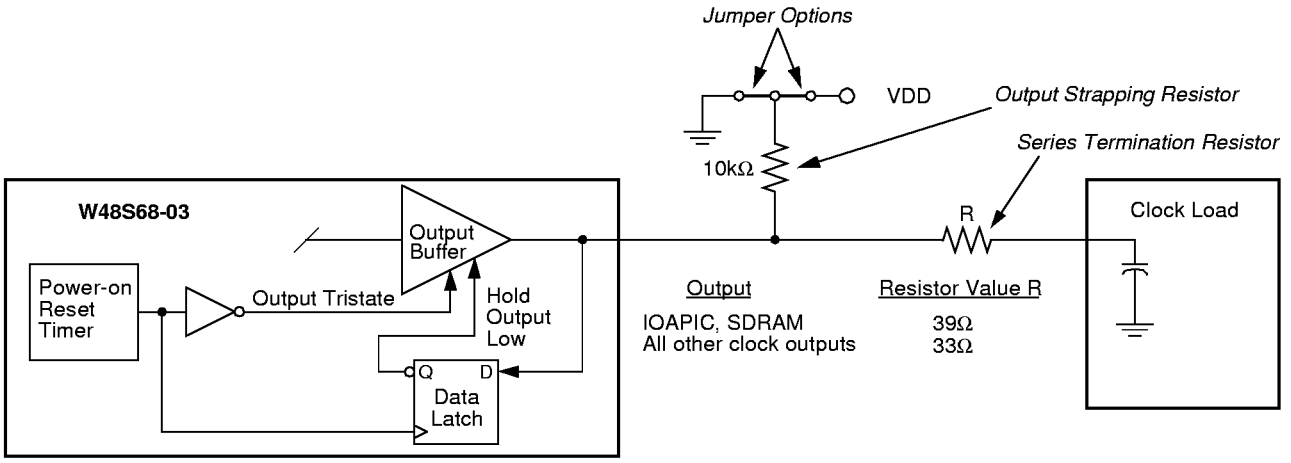


Figure 4 Input Logic Selection Through Jumper Option



CPU/PCI Frequency Selection

CPU frequency is selected with I/O pin 29 and pin 30(48/FS1). Refer to Table 2 for CPU/PCI frequency programming information. Additional frequency selections are available through the serial data interface. Refer to Table 6, "Additional Frequency Selections through Serial Data Interface Data Bytes" on page 8.

Output Buffer Configuration

Clock Outputs

All clock outputs are designed to drive serial terminated clock lines. The W48S68-03 outputs are CMOS-type which provide rail-to-rail output swing. To accommodate the limited voltage swing required by some processors, the output buffers of CPU0:4 use a special VDDQ2 power supply pin that can be tied to 2.5V nominal.

Crystal Oscillator

The W48S68-03 requires one input reference clock to synthesize all output frequencies. The reference clock can be either an externally generated clock signal or the clock generated by the internal crystal oscillator. When using an external clock signal, pin X1 is used as the clock input and pin X2 is left open. The input threshold voltage of pin X1 is VDD/2.

The internal crystal oscillator is used in conjunction with a quartz crystal connected to device pins X1 and X2. This forms a parallel resonant crystal oscillator circuit. The W48S68-03 incorporates the necessary feedback resistor and crystal load capacitors. Including typical stray circuit capacitance, the total load presented to the crystal is approximately 14pF. For optimum frequency accuracy without the addition of external capacitors, a parallel-resonant mode crystal specifying a load of 14pF should be used. This will typically yield reference frequency accuracies within ±100 ppm. To achieve similar accuracies with a crystal calling for a greater load, external capacitors must be added such that the total load (internal, external, and parasitic capacitors) equals that called for by the crystal. For example, the use of a crystal calling for a 20pF load capacitance would require the addition of a 14pF capacitor at both pins X1 and X2, each terminated to ground (viewed by the crystal, these external load capacitors are connected in series through the common ground). Failure to match capacitance or the use of a serial resonant crystal could result in an oscillator frequency error as high as 500 ppm.

Dual Supply Voltage Operation

The W48S68-03 is designed for dual power supply operation. Supply pin VDDQ3 is connected to a 3.3V supply and supply power to the internal core circuit and to the clock output buffers, except for outputs CPU0:4 and IOAPIC. Supply pin VDDQ2 should be connected to a 2.5V supply.

Serial Data Interface

The W48S68-03 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the W48S68-03 initializes with default register settings, therefore the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLOCK. In motherboard applications, SDATA and SCLOCK are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface an also be used during system operation for power management functions. Table 3 summarizes the control functions of the serial data interface.

Table 3 Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held low.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused SDRAM DIMM socket or PCI slot.
48MHZ Clock Output Frequency Selection	48MHZ clock outputs can be set to 48MHz.	Provides flexibility in Super I/O and USB device selection.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections beyond the 50 and 66.6MHz selections that are provided by the FS0:2 power-on default selection. Frequency is changed in a smooth and controlled fashion.	For alternate CPU devices, and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Output Tristate	Puts all clock outputs into a high impedance state.	Production PCB testing.
Test Mode	All clock outputs toggle in relation with X1 input, internal PLL is bypassed. Refer to Table 5.	Production PCB testing.
(Reserved)	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

Operation

Data is written to the W48S68-03 in ten bytes of eight bits each. Bytes are written in the order shown in Table 4.

Table 4 Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the W48S68-03 to accept the bits in Data Bytes 0-6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the W48S68-03 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Dont' Care	Unused by the W48S68-03, therefore bit values are ignored (dont' care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Dont' Care	Unused by the W48S68-03, therefore bit values are ignored (dont' care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to Table 5	The data bits in these bytes set internal W48S68-03 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to Table 5, Data Byte Serial Configuration Map.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3		
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

Writing Data Bytes

Each bit in the data bytes control a particular device function except for the "reserved" bits which must be writing as a logic 0. Bits are written MSB (most significant bit) first, which is bit 7. Table 5 gives the bit formats for registers located in Data Bytes 0-6.

Table 6 details additional frequency selections that are available through the serial data interface.

Table 7 details the select functions for Byte 0, bits 1 and 0.

Table 5 Data Bytes 0-6 Serial Configuration Map

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 0						
7	--	--	(Reserved)	--	--	0
6	--	--	SEL_2	Refer to Table 6		0
5	--	--	SEL_1	Refer to Table 6		0
4	--	--	SEL_0	Refer to Table 6		0
3			BYT0 _FS#	Frequency Controlled by FS (1:0)	Frequency Controlled by BYT0_SEL (2:0)	0
2			(Reserved)			0
1-0	--	--	Bit 1 Bit 0 Function (See Table 7 for function details) 0 0 Normal Operation 1 0 (Reserved) 0 1 Test Mode 1 1 All Outputs Tristated			00
Data Byte 1						
7			(Reserved)			
6	--	--	--	--	--	--
5	--	--	(Reserved)	--	--	0
4	46	CPU4	Clock Output Disable	Low	Active	1
3	48	CPU3	Clock Output Disable	Low	Active	1
2	49	CPU2	Clock Output Disable	Low	Active	1
1	51	CPU1	Clock Output Disable	Low	Active	1
0	52	CPU0	Clock Output Disable	Low	Active	1
Data Byte 2						
7	--	--	(Reserved)	--	--	0
6	8	PCI_F	Clock Output Disable	Low	Active	1
5	16	PCI5	Clock Output Disable	Low	Active	1
4	14	PCI4	Clock Output Disable	Low	Active	1
3	13	PCI3	Clock Output Disable	Low	Active	1
2	12	PCI2	Clock Output Disable	Low	Active	1
1	11	PCI1	Clock Output Disable	Low	Active	1
0	9	PCI0	Clock Output Disable	Low	Active	1
Data Byte 3						
7	28	SDRAM7	Clock Output Disable	Low	Active	1
6	36	SDRAM6	Clock Output Disable	Low	Active	1
5	38	SDRAM5	Clock Output Disable	Low	Active	1

Table 5 Data Bytes 0-6 Serial Configuration Map (cont.)

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
4	39	SDRAM4	Clock Output Disable	Low	Active	1
3	41	SDRAM3	Clock Output Disable	Low	Active	1
2	42	SDRAM2	Clock Output Disable	Low	Active	1
1	44	SDRAM1	Clock Output Disable	Low	Active	1
0	45	SDRAM0	Clock Output Disable	Low	Active	1
Data Byte 4						
7	24	SDRAM15	Clock Output Disable	Low	Active	1
6	25	SDRAM14	Clock Output Disable	Low	Active	1
5	32	SDRAM13	Clock Output Disable	Low	Active	1
4	33	SDRAM12	Clock Output Disable	Low	Active	1
3	18	SDRAM11	Clock Output Disable	Low	Active	1
2	19	SDRAM10	Clock Output Disable	Low	Active	1
1	21	SDRAM9	Clock Output Disable	Low	Active	1
0	22	SDRAM8	Clock Output Disable	Low	Active	1
Data Byte 5						
7	--	--	(Reserved)	--	--	0
6	2	REF1	Clock Output Disable	Low	Active	1
5	54	IOAPIC1	Clock Output Disable	Low	Active	1
4	55	IOAPIC0	Clock Output Disable	Low	Active	1
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	--	--	(Reserved)	--	--	--
0	3	REF0	Clock Output Disable	Low	Active	1
Data Byte 6						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	--	--	(Reserved)	--	--	0
0	--	--	(Reserved)	--	--	0

Table 6 Additional Frequency Selections through Serial Data Interface Data Bytes

Input Conditions			Output Frequency	
Data Byte 0, Bit 3 = 1				
Bit 6 SEL_2	Bit 5 SEL_1	Bit 4 SEL_0	CPU, SDRAM Clocks (MHz)	PCI Clocks (MHz)
0	0	0	68.5	34.3
0	0	1	75.0	32
0	1	0	75.0	30
0	1	1	83.3	33.3
1	0	0	83.3	41.7
1	0	1	75.0	37.5
1	1	0	60.0	30.0
1	1	1	66.8	33.4

Table 7 Select Function for Data Byte 0, Bits 0:1

Function	Input Conditions		Output Conditions				
	Data Byte 0		CPU0:3, SDRAM0:11	PCI_F, PCI0:5	REF0:1, IOAPIC	48MHz	24MHz
	Bit 1	Bit 0					
Normal Operation	0	0	Note 1	Note 1	14.318MHz	48MHz	24
Test Mode	0	1	X1/2	X1/4	X1	X1/2	X1/4
Tristate	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Notes: 1. CPU, SDRAM and PCI frequency selections are listed in Table 2 and Table 6.

How To Use the Serial Data Interface

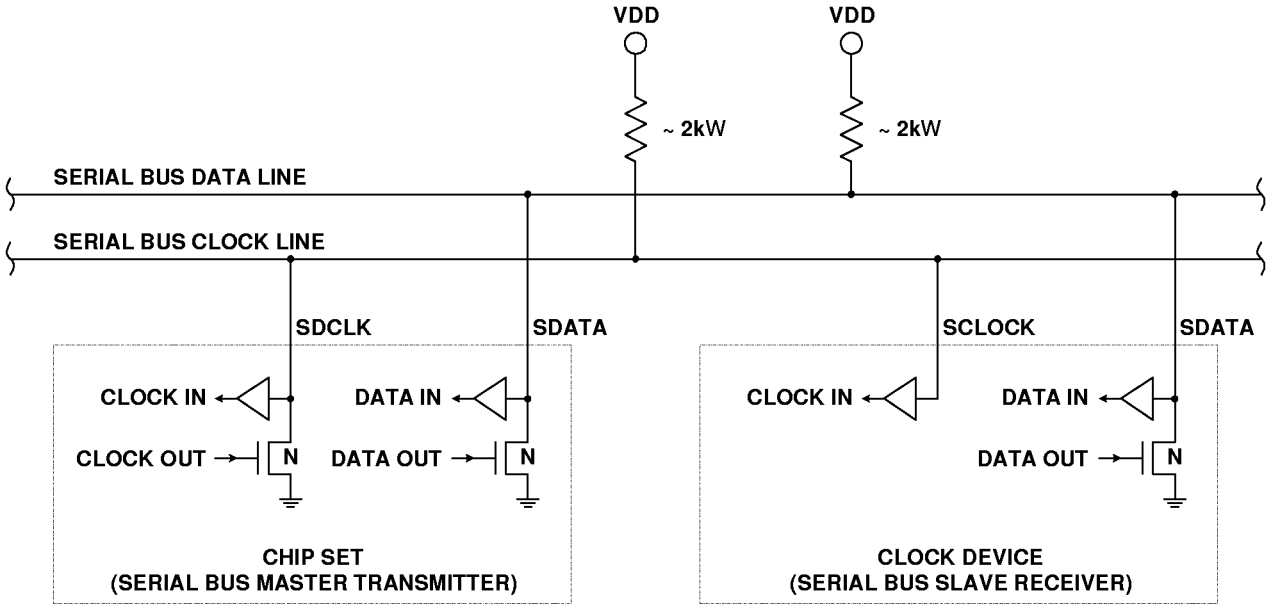
Electrical Requirements

Figure 5 illustrates electrical characteristics for the serial interface bus used with the W48S68-03. Devices send data over the bus with an open collector logic output that can (a) pull the bus line low, or (b) let the bus default to logic 1. The pull-up resistor on the bus (both clock and data lines) establish a default logic 1. All bus devices generally have logic inputs to receive data.

Although the W48S68-03 is a receive-only device (no data write-back capability), it does transmit an "acknowledge" data pulse after each byte is received. Thus, the SDATA line can both transmit and receive data.

The open collector output and pull-up resistor should be sized to meet the rise and fall times specified in AC parameters, taking into consideration total bus line capacitance.

Figure 5 Serial Interface Bus Electrical Characteristics



Signaling Requirements

As shown in Figure 6, valid data bits are defined as stable logic 0 or 1 condition on the data line during a clock high (logic 1) pulse. A transitioning data line during a clock high pulse may be interpreted as a start or stop pulse (it will be interpreted as a start or stop pulse if the start/stop timing parameters are met).

A write sequence is initiated by a "start bit" as shown in Figure 7. A "stop bit" signifies that a transmission has ended.

As stated previously, the W48S68-03 sends an "acknowledge" pulse after receiving eight data bits in each byte as shown in Figure 8.

Figure 6 Serial Data Bus Valid Data Bit

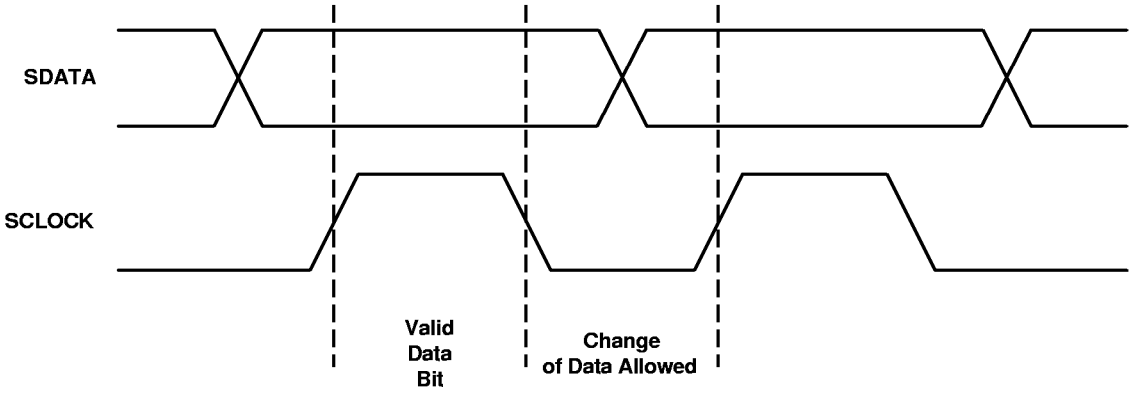


Figure 7 Serial Data Bus Start and Stop Bit

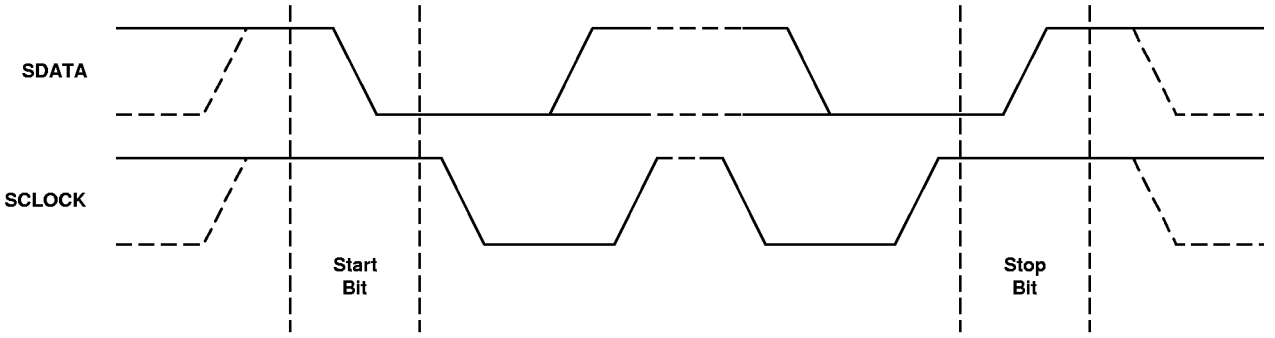


Figure 8 Serial Data Bus Write Sequence

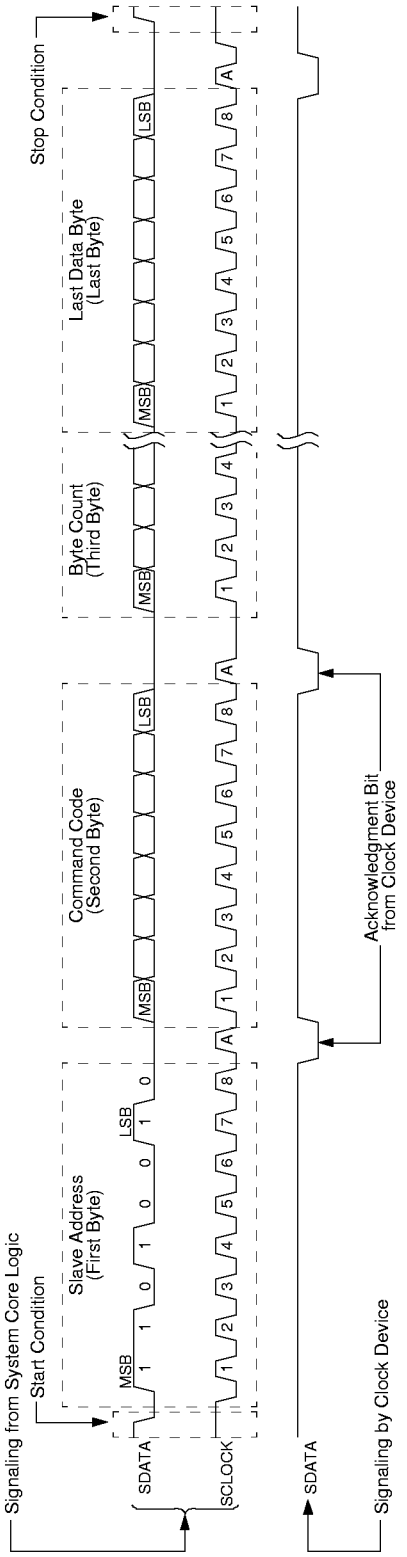
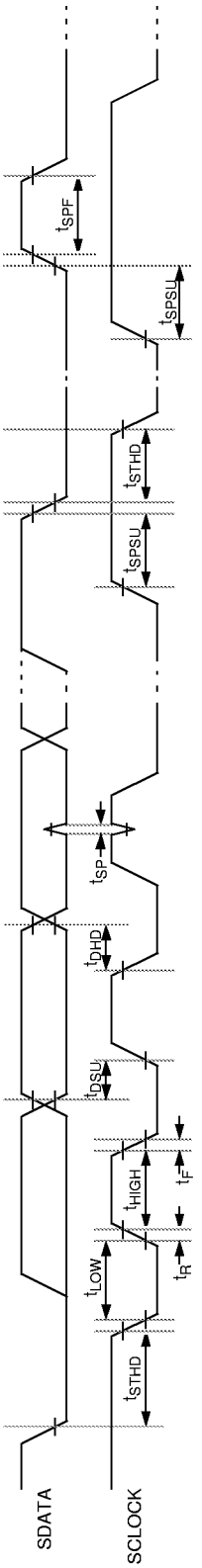


Figure 9 Serial Data Bus Timing Diagram



Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:4	52, 51, 49, 48, 46	O	***CPU Clock Outputs 0 through 4:*** Five CPU. Output voltage swing is controlled by voltage applied to VDDQ2.
PCI_F	8	O	***Fixed PCI Clock Output:*** As an output, this pin works in conjunction with PCI0:5. Output voltage swing is controlled by voltage applied to VDDQ3.
PCI1:5	9, 11, 12, 13, 14, 16	O	***PCI Bus Clock Outputs 1 through 5:*** Output voltage swing is controlled by voltage applied to VDDQ3.
SDRAM0:15	45, 44, 42, 41, 39, 38, 36, 35, 33, 32, 25, 24, 22, 21, 19, 18	O	***SDRAM Clock Outputs 0 through 15:*** These sixteen SDRAM clock outputs run synchronous to the CPU clock outputs. Output voltage swing is controlled by voltage applied to VDDQ3.
IOAPIC0:2	2, 55, 54	O	***I/O APIC Clock Outputs:*** Provides 14.318MHz fixed frequency. The output voltage swing is controlled by VDDQ2.
48MHZ/FS1	29	I/O	***48MHz Output and Frequency Selection Bit 1:*** Fixed clock output that defaults to 48MHz following device power-up. Output voltage swing is controlled by voltage applied to VDDQ3. As an input, this pin functions as part of the frequency selection address. The value of FS0:1 determines the power-up default frequency of device output clocks as per the Table 2, "Pin Selectable Frequency" on page 1.
24MHz/FS0	30	I/O	***24MHz Output and Frequency Selection Bit 0:*** Fixed clock output that defaults to 24MHz following device power-up.
REF0	3	I/O	***Fixed 14.318MHz Output:*** As an output, this pin is used for various system applications. Output voltage swing is controlled by voltage applied to VDDQ3.
X1	5	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It can be used as an external 14.318MHz crystal connection or as an external reference frequency input.
X2	6	I	***Crystal Connection:*** An input connection for an external 14.318MHz crystal. If using an external reference, this pin must be left unconnected.
SDATA	23	I	***Serial Data Input:*** Data input for Serial Data Interface. Refer to Serial Data Interface section that follows.
SCLOCK	24	I	***Serial Clock Input:*** Clock input for Serial Data Interface. Refer to Serial Data Interface section that follows.
VDD	1	P	***Power Connection:*** Power supply for crystal oscillator and REF0 output buffers. Connected to 3.3V supply.
VDDQ2	56,50	P	***Power Connection:*** Power supply for IOAPIC output buffer, core logic and PLL circuitry. Connected to 2.5V.
VDDQ3	43, 37, 26, 20, 15, 7	P	***Power Connection:*** Power supply for SDRAM and PCI clock output buffers. Connected to 3.3V supply.
GND	4, 10, 17, 23, 31, 34, 40, 47, 53	G	***Ground Connection:*** Connect all ground pins to the common system ground plane.

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C
ESD_{PROT}	Input ESD Protection	2 (min)	kV

3.3V DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = VDD = 3.3V±5% (3.135-3.456V), VDD_{IOAPIC} = VDD_{CPU} = 2.5V±5% (2.375-2.625V)

Symbol	Parameter		Min	Typ	Max	Unit	Test Condition
Supply Current							
$I_{DD-3.3V}$	Combined 3.3V Supply Current			150	235	mA	CPUCLK = 66.4MHz Outputs Loaded (Note 1)
$I_{DD-2.5}$	Combined 2.5V Supply Current			30	50	mA	CPUCLK = 66.4MHz Outputs Loaded (Note 1)
Logic Inputs							
V_{IL}	Input Low Voltage				0.8	V	
V_{IH}	Input High Voltage		2.0			V	
I_{IL}	Input Low Current (Note 2)				10	µA	
I_{IH}	Input High Current (Note 2)				10	µA	
Clock Outputs							
V_{OL}	Output Low Voltage				50	mV	I_{OL} = 1mA
V_{OH}	Output High Voltage		3.1			V	I_{OH} = –1mA
I_{OL}	Output Low Current:	CPU0:4	45	70	105	mA	V_{OL} = 1.25V
		SDRAM0:15	80	110	155		V_{OL} = 1.5V
		PCI_F, PCI0:5	55	75	105		V_{OL} = 1.5V
		IOAPIC	55	85	130		V_{OL} = 1.25V
		REF0	60	75	105		V_{OL} = 1.5V
		48MHZ	55	75	105		V_{OL} = 1.5V

3.3V DC Electrical Characteristics (cont)

Symbol	Parameter		Min	Typ	Max	Unit	Test Condition
I_{OH} Output High Current:		CPU0:4	40	65	95	mA	V_{OH} = 1.25V
		SDRAM0:15	80	120	175		V_{OH} = 1.5V
		PCI_F, PCI0:5	55	85	125		V_{OH} = 1.5V
		IOAPIC	50	80	120		V_{OH} = 1.25V
		REF0	60	85	110		V_{OH} = 1.5V
		48MHZ	55	85	125		V_{OH} = 1.5V
Crystal Oscillator							
V_{TH}	X1 Input threshold Voltage (Note 3)			1.25	1.7	V	
C_{LOAD}	Load Capacitance, Imposed on External Crystal (Note 4)			14	20	pF	
$C_{IN,X1}$	X1 Input Capacitance (Note 5)			30	40	pF	Pin X2 unconnected
Pin Capacitance/Inductance							
C_{IN}	Input Pin Capacitance				5	kΩ	Except X1 and X2
C_{OUT}	Output Pin Capacitance				6	pF	
L_{IN}	Input Pin Inductance				7	nH	
Serial Input Port							
V_{IL}	Input Low Voltage				$0.3V_{DD}$	V	V_{DD} = 2.5V
V_{IH}	Input High Voltage		$0.7V_{DD}$			V	V_{DD} = 2.5V
I_{IL}	Input Low Current				10	µA	No internal pull-up/down on SDATA or SCLOCK
I_{IH}	Input High Current				10	µA	No internal pull-up/down on SDATA or SCLOCK
I_{OL}	Sink Current into SDATA or SCLOCK, Open Drain N-Channel Device On		6			mA	$I_{OL} = 0.3V_{DD}$
C_{IN}	Input Capacitance of SDATA and SCLOCK				10	pF	
C_{SDATA}	Total Capacitance of SDATA Bus				400	pF	
C_{SCLOCK}	Total Capacitance of SCLOCK Bus				400	pF	

2.5V AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = VDD = 3.3V±5% (3.135-3.465V), VDD_{IOAPIC} = VDD_{CPU} = 2.5V±5% (2.375-2.625V), f_{XTL} = 14.31818MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.

CPU Clock Outputs, CPU0:4 (Lump Capacitance Test Load = 20pF)

Symbol	Parameter	CPU = 66.6MHz			CPU = 60MHz			Unit	Test Condition/Comments
		Min	Typ	Max	Min	Typ	Max		
t_P	Period	15			16.7			ns	Measured on rising edge at 1.25V.
f	Frequency, Actual		66.8			59.876		MHz	Determined by PLL divider ratio.
t_H	High Time	5.2			6			ns	Duration of clock cycle above 2.0V.
t_L	Low Time	5			5.8			ns	Duration of clock cycle below 0.4V.
t_R	Output Rise Edge Rate	0.8		3	0.8		3	V/ns	Measured from 0.4V to 2.0V.
t_F	Output Fall Edge Rate	0.8		3	0.8		3	V/ns	Measured from 2.0V to 0.4V.
t_D	Duty Cycle	45		55	45		55	%	Measured on rising and falling edge at 1.25V.
t_{JC}	Jitter, Cycle-to-Cycle			250			250	ps	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.
t_{SK}	Output Skew			250			250	ps	Measured on rising edge at 1.25V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3			3	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance	12	20	30	12	20	30	ohm	Average value during switching transition. Used for determining series termination value.

SDRAM Clock Outputs, SDRAM0:15 (Lump Capacitance Test Load = 30pF)

Symbol	Parameter	CPU = 66.6MHz			CPU = 60MHz			Unit	Test Condition/Comments
		Min	Typ	Max	Min	Typ	Max		
t_P	Period	15			16.7			ns	Measured on rising edge at 1.5V.
f	Frequency, Actual		66.8			59.876		MHz	Determined by PLL divider ratio.
t_R	Output Rise Edge Rate	1		4	1		4	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	1		4	1		4	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45		55	45		55	%	Measured on rising and falling edge at 1.5V.
t_{JC}	Jitter, Cycle-to-Cycle			250			250	ps	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.
t_{SK}	Output Skew		100			100		ps	Measured on rising edge at 1.5V.
t_{SK}	CPU to SDRAM Clock Skew			500			500	ps	Covers all CPU/SDRAM outputs. Measured on rising edge at 1.5V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3			3	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance	10	15	20	10	15	20	ohm	Average value during switching transition. Used for determining series termination value.

2.5V AC Electrical Characteristics (cont)

PCI Clock Outputs, PCI_F and PCI0:5 (Lump Capacitance Test Load = 30pF)

Symbol	Parameter	CPU = 66.6MHz			CPU = 60MHz			Unit	Test Condition/Comments
		Min	Typ	Max	Min	Typ	Max		
t_P	Period	30			33.3			ns	Measured on rising edge at 1.5V.
f	Frequency, Actual		33.4			29.938		MHz	Determined by PLL divider ratio.
t_H	High Time	12			13.3			ns	Duration of clock cycle above 2.4V.
t_L	Low Time	12			13.3			ns	Duration of clock cycle below 0.4V.
t_R	Output Rise Edge Rate	1		4	1		4	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	1		4	1		4	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45		55	45		55	%	Measured on rising and falling edge at 1.5V.
t_{JC}	Jitter, Cycle-to-Cycle			250			250	ps	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.
t_{SK}	Output Skew			250			250	ps	Measured on rising edge at 1.5V.
t_O	CPU to PCI Clock Offset	1		4	1		4	ns	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3			3	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance	15	20	30	15	20	30	ohm	Average value during switching transition. Used for determining series termination value.

IOAPIC Clock Output (Lump Capacitance Test Load = 20pF)

Symbol	Parameter	CPU = 60/66.6MHz			Unit	Test Condition/Comments
		Min	Typ	Max		
f	Frequency, Actual		14.31818		MHz	Frequency generated by crystal oscillator.
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.0V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.0V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.25V.
t_A	Jitter, Absolute				ps	Measured on rising edge at 1.25V. Maximum deviation of clock period.
f_{ST}	Frequency Stabilization from Power-up (cold start)			1.5	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance	10	15	25	ohm	Average value during switching transition. Used for determining series termination value.

REF0 Clock Output (Lump Capacitance Test Load = 45pF)

Symbol	Parameter	CPU = 60/66.6MHz			Unit	Test Condition/Comments
		Min	Typ	Max		
f	Frequency, Actual		14.31818		MHz	Frequency generated by crystal oscillator.
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	40		60	%	Measured on rising and falling edge at 1.5V.
t_A	Jitter, Absolute				ps	Measured on rising edge at 1.5V. Maximum deviation of clock period.
f_{ST}	Frequency Stabilization from Power-up (cold start)			1.5	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance	17	20	25	ohm	Average value during switching transition. Used for determining series termination value.

2.5V AC Electrical Characteristics (cont)

48MHZ/24MHz Clock Outputs (Lump Capacitance Test Load = 20pF)

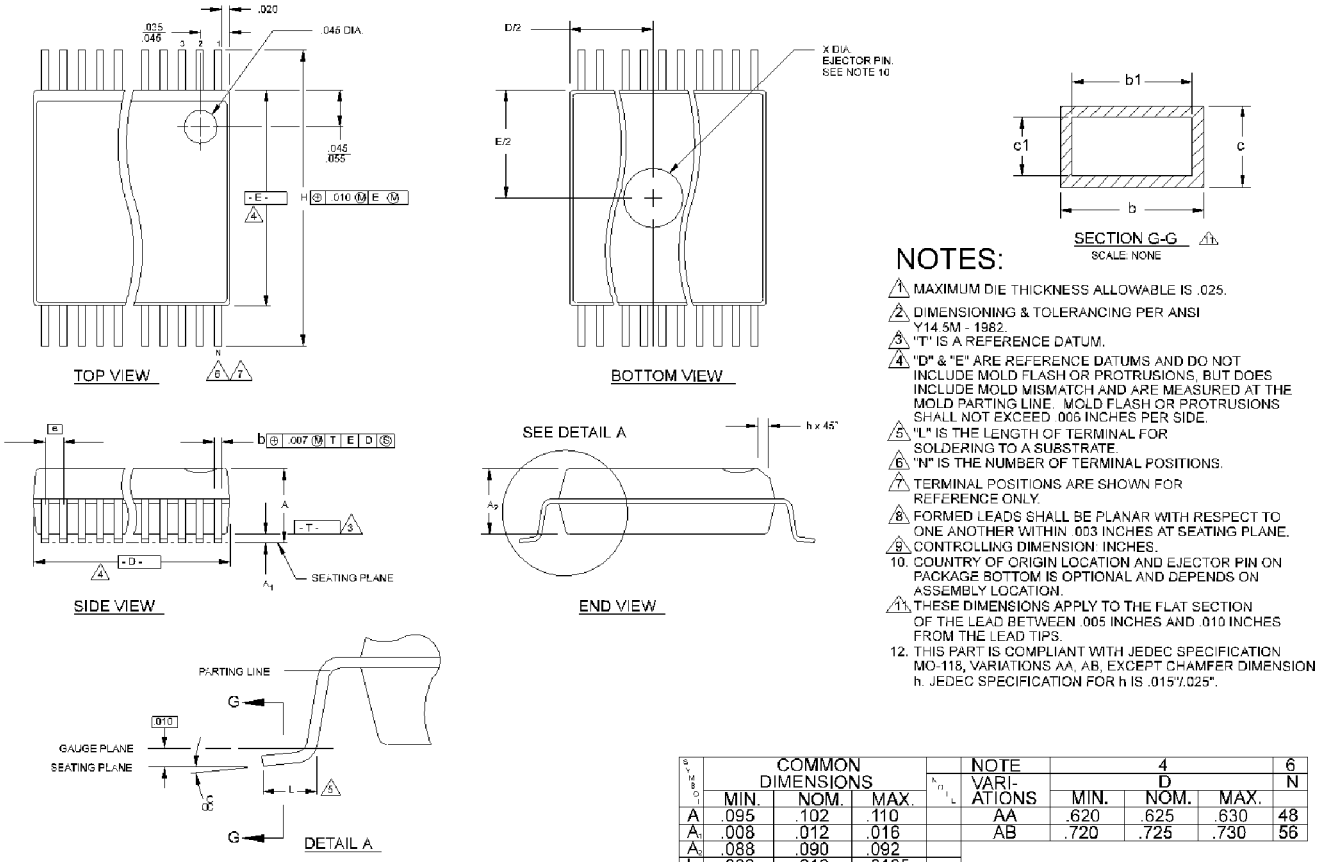
Symbol	Parameter	CPU = 60/66.6MHz			Unit	Test Condition/Comments
		Min	Typ	Max		
f	Frequency, Actual		48.008/24.004		MHz	Determined by PLL divider ratio (see n/m below).
f_D	Deviation from 48MHz		+167		ppm	(48.008 – 48)/48
n/m	PLL Ratio		57/17, 114/17			(14.31818MHz x 57/17 = 48.008MHz)
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	40		55	%	Measured on rising and falling edge at 1.5V.
t_{JC}	Jitter, Cycle-to-Cycle			500	ps	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance	15	20	30	ohm	Average value during switching transition. Used for determining series termination value.

Serial Input Port

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
f_{SCLOCK}	SCLOCK Frequency	0		400	kHz	
t_{STHD}	Start Hold Time	4.0			µs	
t_{LOW}	SCLOCK Low Time	4.7			µs	
t_{HIGH}	SCLOCK High Time	4.0			µs	
t_{DSU}	Data Setup Time	250			ns	
t_{DHD}	Data Hold Time	0			ns	(Transmitter should provide a 300ns hold time to ensure proper timing at the receiver.)
t_R	Rise Time, SDATA and SCLOCK			1000	ns	From $0.3V_{DD}$ to $0.7V_{DD}$
t_F	Fall Time, SDATA and SCLOCK			300	ns	From $0.7V_{DD}$ to $0.3V_{DD}$
t_{STSU}	Stop Setup Time	4.0			µs	
t_{SPF}	Bus Free Time between Stop and Start Condition	4.7			µs	
t_{SP}	Allowable Noise Spike Pulse Width			50	µs	

Mechanical Package Outline

Figure 10 56-Pin Small Shrink Outline Package (SSOP, 300 mils)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .005 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. CONTROLLING DIMENSION: INCHES.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .010 INCHES FROM THE LEAD TIPS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION h. JEDEC SPECIFICATION FOR h IS .015"/.025".

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	.095	.102	.110	
A_1	.008	.012	.016	
A_2	.088	.090	.092	
b	.008	.010	.0135	
b_1	.008	.010	.012	
c	.005	-	.010	
c_1	.005	.006	.0085	
D	SEE VARIATIONS			4
E	.292	.296	.299	
e	.025 BSC			
H	.400	.406	.410	
h	.010	.013	.016	
L	.024	.032	.040	
N	SEE VARIATIONS			6
X	.085	.093	.100	10
α	0°	5°	8°	

NOTE	4			6
VARIATIONS	D			N
	MIN.	NOM.	MAX.	
AA	.620	.625	.630	48
AB	.720	.725	.730	56

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	2.41	2.59	2.79	
A_1	0.20	0.31	0.41	
A_2	2.24	2.29	2.34	
b	0.203	0.254	0.343	
b_1	0.203	0.254	0.305	
c	0.127	-	0.254	
c_1	0.127	0.152	0.216	
D	SEE VARIATIONS			4
E	7.42	7.52	7.59	
e	0.635 BSC			
H	10.16	10.31	10.41	
h	0.25	0.33	0.41	
L	0.61	0.81	1.02	
N	SEE VARIATIONS			6
X	2.16	2.36	2.54	10
α	0°	5°	8°	

NOTE	4			6
VARIATIONS	D			N
	MIN.	NOM.	MAX.	
AA	15.75	15.88	16.00	48
AB	18.29	18.42	18.54	56

THIS TABLE IN MILLIMETERS

Summary of nominal dimensions in inches:

Body Width: .296
Lead Pitch: .025
Body Length: .726
Body Height: .102

IC WORKS

Sales Information

Corporate Headquarters

IC WORKS, Inc.
3725 North First Street
San Jose, CA 95134-1700
Tel: 408-922-0202
Fax: 408-922-0833

U.S. Sales Representatives

Alabama
Rep One Associates
Huntsville, AL
Tel: 205-539-7371
Fax: 205-533-4509

Arizona
Reptronix, Ltd.
Phoenix, AZ
Tel: 602-230-2630
Fax: 602-230-7730

California
Exis
San Jose, CA
Tel: 408-944-4600
Fax: 408-433-0450

Mission Technology
San Diego, CA
Tel: 619-674-6191
Fax: 619-674-6196

Mission Technology
Santa Ana, CA
Tel: 714-951-3696
Fax: 714-951-3874

Colorado
Bager Electronics
Denver, CO
Tel: 303-321-1340
Fax: 303-322-8229

Illinois
TEQ Sales
Elgin, IL
Tel: 847-742-37677
Fax: 847-742-3947

Indiana
Electronic Components of Indiana
New Albany, IN
Tel/Fax: 812-945-3187

Florida
Marathon Technical Assoc.
St Petersburg, FL
Tel: 813-894-3603
Fax: 813-894-3804

Marathon Technical Assoc.
Orlando, FL
Tel: 407-872-5775
Fax: 407-872-0535

Marathon Technical Assoc.
Pompano Beach, FL
Tel: 954-785-0072
Fax: 954-782-7090

Maryland
Robert Electronic Sales
Columbia, MD
Tel: 410-995-1900 (MD)
Tel: 301-982-1177 (DC)

Massachusetts
Hi-Peak Technical Sales
Chelmsford, MA
Tel: 978-251-8200
Fax: 978-251-0200

Future Global
Bolton, MA
Tel: 978-779-6900
Fax: 978-779-5141

Michigan
MicroTech Sales
Plymouth, MI
Tel: 313-459-0200
Fax: 313-459-0232

Minnesota
Gleason Associates
Prior Lake, MN
Tel/Fax: 612-447-7020

Minnesota
Gleason Associates
Prior Lake, MN
Tel/Fax: 612-447-7020

New Jersey
Harwood Associates
Maplewood, NJ
Tel: 973-763-0706
Fax: 973-763-2432

New York (Upstate)
ICS-LAMTEC
East Syracuse, NY
Tel: 315-432-8236
Fax: 315-432-8327

North Carolina
Rep One Associates
Raleigh, NC
Tel: 919-845-9900
Fax: 919-845-9700

Future Global
Raleigh, NC
Tel: 919-877-9625
Fax: 919-877-9538

Oregon
Phase II
Portland, OR
Tel: 503-292-7922
Fax: 503-292-7903

Phase II
Kirkland, WA
Tel: 425-821-8313
Fax: 425-823-4089

Pennsylvania
Harwood Associates
Huntington, NY
Tel: 516-673-1900
Fax: 516-673-2848

Texas
Millennium Sales, Inc.
Austin, TX
Tel: 512-335-2375
Fax: 512-335- 2376

Utah
Bager Electronic
Salt Lake City Utah
Tel: 801-582-0501
Fax: 801-582-1850

Wisconsin
TEQ Sales
Waukesha, WI
Tel: 414-780-0340
Fax: 414-780-0342

Puerto Rico
Marathon Technical Assoc.
Mayaguez, PR
Tel: 809-831-4050
Fax: 809-831-4250

International Sales Representatives

Australia
ICD Australia
Bayswater, Victoria
Tel: 613-761-3455
Fax: 613-761-3415

Canada
Electro Source, Inc.
Rexdale, Ontario
Tel: 416-675-4490
Fax: 416-675-6871

Electro Source, Inc.
Pointe Claire, Quebec
Tel: 514-630-7486
Fax: 514-630-7421

Electro Source, Inc.
Kanata, Ontario
Tel: 613-592-3214
Fax: 613-592-4256

Electro Source, Inc.
Burnaby, B.C.
Tel: 604-435-2533
Fax: 604-435-2538

France
Tech Inter
Trappes, France
Tel: 33-1-30-51-6699
Fax: 33-1-30-62-2019

Germany
Ineltek Gmbh
Heidenheim, Germany
Tel: 49-40-839-604
Fax: 49-40-839-60433

Ineltek Gmbh
Vienna, Austria
Tel: 43-1-204-9838
Fax: 43-1-204-9038

Hong Kong
Semicon Product & Systems Co. Ltd.
Kowloon, Hong Kong
Tel: 852-763-7788
Fax: 852-763-6155

Italy
Consystem SRL
Milan, Italy
Tel: 39-26-640-0153
Fax: 39-26-640-0339

Japan
Macnica, Inc.
Yokohama City, Japan
Tel: 81-045-939-6106
Fax: 81-045-939-6107

Korea
FM Com Corporation
Seoul, Korea
Tel: 822-596-3880
Fax: 822-596-3881

Netherlands
Tekelec Airtronic B.V.
Zoetermeer, Netherlands
Tel: 317-934-61430
Fax: 317-934-17504

Singapore, Thailand, Malaysia
Transdata Tech Private, Ltd.
Singapore
Tel: 65-741-0161
Fax: 65-741-2016

Taiwan
Weikeng Industrial Co., Ltd.
Taipei, Taiwan, ROC
Tel: 886-22-659-0202
Fax: 886-22-658-0959

United Kingdom
K-9 Technology Limited
Marlborough, UK
Tel: 44-1672-515199
Fax: 44-1672-515399

North American Distributors

Bell Microproducts/ Vantage
San Jose, CA
Tel: 408-451-9400
Fax: 408-451-1600

Irvine, CA..... 714-470-2900

Westlake Village, CA 805-496-2606

Redmond, WA.. 206-861-5710

Clifton, NJ..... 201-777-4100

Billerica, MA..... 508-667-2400

Smithtown, NY. 516-543-2000

Columbia, MD... 410-720-5100

Herndon, VA..... 703-803-1020

Amber, PA..... 215-540-4148

Altamonte Springs, FL 407-682-1199

Deerfield Beach, FL 305-429-1001
Edina, MN..... 612-933-3236
Austin, TX..... 517-208-0725
Richardson,TX 214-783-4191

Dove Electronic Components, Inc.
East Setauket, NY
Tel: 516-689-7733
Fax: 516-689-7362
Mathews, NC.... 704-847-8695
Vienna, VA 703-893-1821
Dania, FL..... 305-920-4101
Mtn View, CA.... 415-254-8944
Melbourne, FL.. 407-242-6916
Alpharetta, CA.. 404-993-6336

Richardson Electronics, Ltd.
La Fox, IL
Tel: 708-208-2200
Fax: 708-208-2553
E. Rochester, NY
Tel: 716-264-1100
Fax: 716-264-1150

Lawrenceville, GA
Tel: 800-471-2016
Fax: 770-979-6684

Anna, TX
Tel: 214-924-2308
Fax: 214-924-2845

San Jose, CA
Tel: 800-348-5580
Fax: 408-441-8588

Scottsdale, AZ
Tel: 602-922-7172
Fax:602-922-4715

The Netherlands
European Headquarters
Tel: 31-020-691-91-48
Fax: 31-020-691-93-78

Valtrie Marketing, Inc.
Rexdale, Ontario, Canada
Tel: 416-798-2555
Fax: 416-798-2560

(2/98)