

# 54F/74F412

## Multi-Mode Buffered Latch With 3-State Outputs

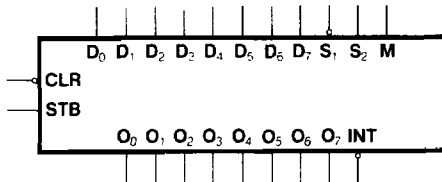
### Description

The 'F412 is an 8-bit latch with 3-state output buffers. Also included is a status flip-flop for providing device-busy or request-interrupt commands. Separate Mode and Select inputs allow data to be stored with the outputs enabled or disabled. The device can also operate in a fully transparent mode. The 'F412 is the functional equivalent of the Intel 8212.

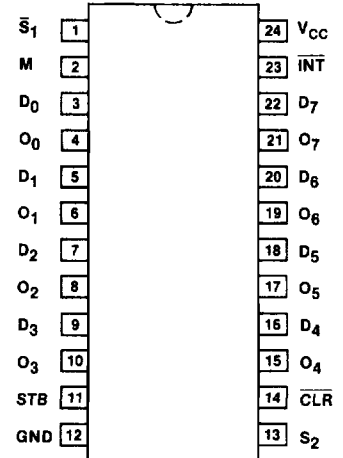
- 3-State Outputs
- Status Flip-flop for Interrupt Commands
- Asynchronous or Latched Receiver Modes
- 300 mil 24-Pin Slim Package

Ordering Code: See Section 5

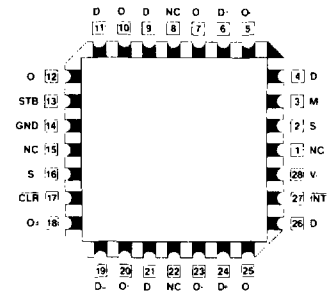
### Logic Symbol



### Connection Diagrams



### Pin Assignment for DIP and SOIC



### Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
O <sub>0</sub> -O <sub>7</sub>	Latch Outputs	75/15 (12.5)
D <sub>0</sub> -D <sub>7</sub>	Data Inputs	0.5/0.375
CLR	Clear	0.5/0.375
STB	Strobe	0.5/0.375
INT	Interrupt	25/12.5
M	Mode Control Input	0.5/0.375
S <sub>1</sub> , S <sub>2</sub>	Select Inputs	0.5/0.375

### Functional Description

This high-performance eight-bit parallel expandable buffer register incorporates package and mode selection inputs and an edge-triggered status flip-flop designed specifically for implementing bus-organized input/output ports. The 3-state data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides busy or request interrupt commands.

The eight data latches are fully transparent when the internal gate enable, G, input is HIGH and the outputs are enabled. Latch transparency is selected by the mode control (M), select ( $\bar{S}_1$  and  $S_2$ ), and the strobe (STB) inputs and during transparency each data output ( $O_n$ ) follows its respective data input ( $D_n$ ). This mode of operation can be terminated by clearing, de-selecting, or holding the data latches.

An input mode or an output mode is selectable from the M input. In the input mode, M = L, the eight data latch inputs are enabled when the strobe is HIGH regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken LOW, the latches will store the most-recently setup data.

In the output mode, M = H, the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the select ( $\bar{S}_1$  and  $S_2$ ) inputs.

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#### Data Latches Function Table

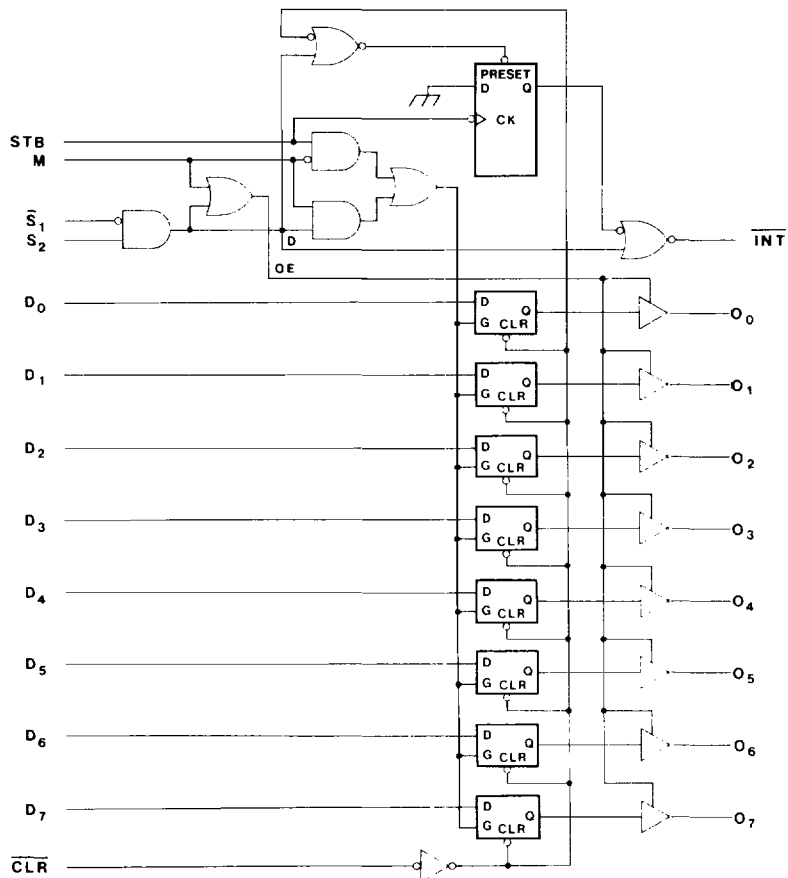
Function	$\bar{CLR}$	M	$\bar{S}_1$	$S_2$	STB	Data In	Data Out
Clear	L	H	H	X	X	X	L
	L	L	L	H	L	X	L
De-select	X	L	X	L	X	X	Z
	X	L	H	X	X	X	Z
Hold	H	H	H	L	X	X	$Q_0$
	H	L	L	H	L	X	$Q_0$
Data Bus	H	H	L	H	X	L	L
	H	H	L	H	X	H	H
Data Bus	H	L	L	H	H	L	L
	H	L	L	H	H	H	H

#### Status Flip-flop Function Table

$\bar{CLR}$	$\bar{S}_1$	$S_2$	STB	INT
L	H	X	X	H
L	X	L	X	H
H	X	X	J	L
H	L	H	X	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

### DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
$I_{CCH}$ $I_{CCL}$ $I_{CCZ}$	Power Supply Current		33 40 40	50 60 60	mA	$V_{CC} = \text{Max}$

## AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} =$ Mil $C_L = 50\text{ pF}$		$T_A, V_{CC} =$ Com $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to $O_n$	3.5	6.5	8.5	3.0	11.5	3.0	9.5	ns	3-1 3-4
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{S}_1, S_2$ or STB to $O_n$	8.5	14.5	18.5	6.5	23.0	7.5	20.5	ns	3-1 3-7
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{S}_1$ or $S_2$ to $\bar{INT}$	4.5	7.5	9.5	3.5	12.0	4.0	10.5	ns	3-1 3-10
$t_{PHL}$	Propagation Delay $\bar{CLR}$ to $O_n$	7.5	12.5	16.0	5.5	18.5	6.5	17.5	ns	3-1 3-9
$t_{PHL}$	Propagation Delay STB to $\bar{INT}$	6.5	11.0	14.0	5.5	17.5	5.5	15.0	ns	3-1 3-10
$t_{PZH}$ $t_{PZL}$	Access Time, HIGH or LOW $\bar{S}_1$ to $O_n$	8.0	12.5	18.0	6.5	20.0	7.0	19.0	ns	3-1 3-12 3-13
$t_{PHZ}$ $t_{PLZ}$	Disable Time, HIGH or LOW $\bar{S}_1$ to $O_n$	4.5	8.0	10.5	4.0	14.5	4.0	11.5		
$t_{PZH}$ $t_{PZL}$	Access Time, HIGH or LOW $S_2$ to $O_n$	7.5	12.5	16.0	6.5	18.5	6.5	17.5	ns	3-1 3-12 3-13
$t_{PHZ}$ $t_{PLZ}$	Disable Time, HIGH or LOW $S_2$ to $O_n$	4.5	7.5	9.5	3.5	12.5	4.0	10.5		
$t_{PZH}$ $t_{PZL}$	Access Time, HIGH or LOW M to $O_n$	5.0	8.5	11.0	4.5	16.0	4.5	12.0	ns	3-1 3-12 3-13
$t_{PHZ}$ $t_{PLZ}$	Disable Time, HIGH or LOW M to $O_n$	4.0	7.0	9.0	3.5	11.5	3.5	10.0		
		5.0	8.5	11.0	4.5	14.0	4.5	12.0		

## AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$	$T_A, V_{CC} =$ MII	$T_A, V_{CC} =$ Com		
		Min Typ Max	Min Max	Min Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $D_n$ to $\bar{S}_1, S_2$ or STB	0 0	2.0 2.0	1.0 1.0	ns	3-15
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time $D_n$ to $\bar{S}_1, S_2$ or STB	8.0 8.0	10.0 10.0	9.0 9.0		
$t_w(\text{H})$ $t_w(\text{L})$	$\bar{S}_1, S_2$ or STB Pulse Width, HIGH or LOW	8.0 8.0	11.0 11.0	9.0 9.0	ns	3-9
$t_w(\text{L})$	$\overline{\text{CLR}}$ Pulse Width, LOW	8.0	11.5	9.0	ns	3-9