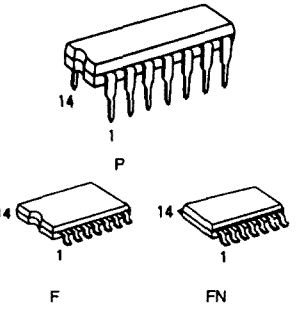
Quad 2-Input NAND Gate (Open Drain)

The TC74HC03A is a high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

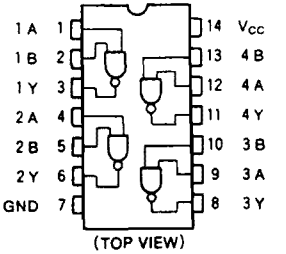
Pin configuration and function are the same as the TC74HC00A. But the TC74HC03A has, as its outputs, high performance MOS N-channel transistors. (OPEN-DRAIN outputs) This device can, therefore, with a suitable pull-up resistors, be used in wired-AND, LED driver and other application.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

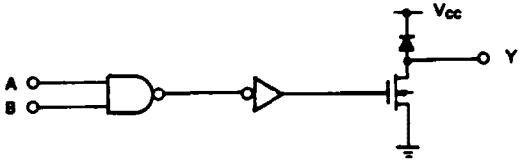


Features

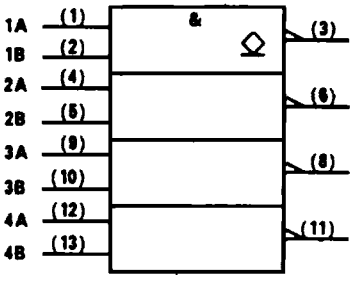
- High Speed: t_{pZ} = 5ns(Typ.) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 1μA(Max.) at Ta = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability: 10 LSTTL Loads
- Wide Operating Voltage Range: V_{CC}(opr) = 2V ~ 6V
- Open Drain Structure
- Pin and Function Compatible with 74LS03



Pin Assignment



Logic Diagram (per gate)



IEC Logic Symbol

Truth Table

A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

Z: High Impedance

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of Ta = -40°C ~ 65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC} = 2.0V) 0 ~ 500(V_{CC} = 4.5V) 0 ~ 400(V_{CC} = 6.0V)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition		V_{CC}	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max.	Ta = -40 ~ 85°C Min.	Ta = -40 ~ 85°C Max.	Unit
High-Level Input Voltage	V_{IH}	–		2.0 4.5 6.0	1.5 3.15 4.2	– – –	– – –	1.5 3.15 4.2	– – –	V
Low-Level Input Voltage	V_{IL}	–		2.0 4.5 6.0	– – –	– – –	0.5 1.35 1.8	– – –	0.5 1.35 1.8	V
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	– – –	0.0 0.0 0.0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V
			I_{OL} = 4 mA I_{OL} = 5.2mA	4.5 6.0	– –	0.17 0.18	0.26 0.26	– –	0.33 0.33	
Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC}		6.0	–	–	±0.5	–	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	–	±0.1	–	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	–	–	1.0	–	10.0	

AC Electrical Characteristics (C_L = 15pF, V_{CC} = 5V, Ta = 25°C)

Parameter	Symbol	Test Conditon	Min.	Typ.	Max.	Unit
Output Transition Time	t_{TLH} t_{THL}	–	–	4	8	ns
Propagation Delay Time	t_{pLZ}	R_L = 1kΩ	–	5	12	
Propagation Delay Time	t_{pZL}	R_L = 1kΩ	–	5	12	

AC Electrical Characteristics (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Parameter	Symbol	Test Condition		Ta = 25°C			Ta = -40 ~ 85°C		Unit
			V_{CC}	Min	Typ.	Max.	Min.	Max.	
Output Transition Time	t_{TLH} t_{THL}	–	2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLZ}	R_L = 1kΩ	2.0	–	20	75	–	95	
			4.5	–	10	15	–	19	
			6.0	–	9	13	–	16	
Propagation Delay Time	t_{pZL}	R_L = 1kΩ	2.0	–	24	75	–	95	
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Input Capacitance	C_{IN}	–		–	5	10	–	10	pF
Output Capacitance	C_{OUT}	–		–	10	–	–	–	
Power Dissipation Capacitance	C_{PD}(1)	–		–	5	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$(per Gate)

Notes