STK11C68

64 Kbit (8K x 8) SoftStore nvSRAM

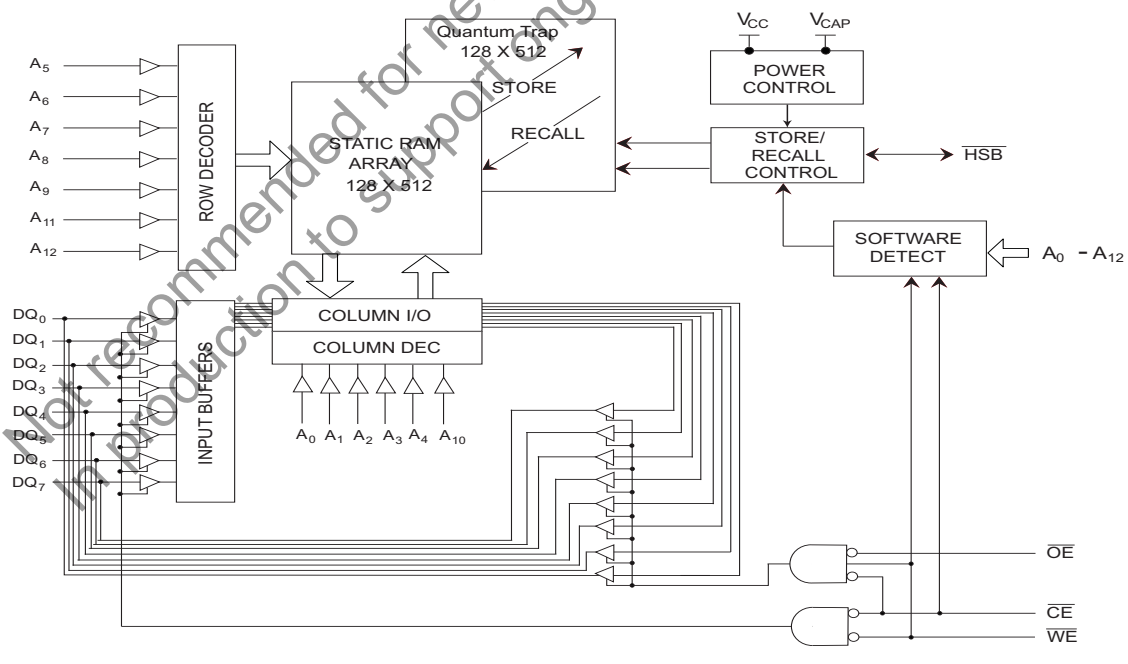
Features

- 25 ns, 35 ns, and 45 ns access times
- Pin compatible with industry standard SRAMs
- Software initiated nonvolatile STORE
- Unlimited Read and Write endurance
- Automatic RECALL to SRAM on power up
- Unlimited RECALL cycles
- 1,000,000 STORE cycles
- 100 year data retention
- Single 5V±10% operation
- Commercial and industrial temperature
- 28-pin (330 mil) SOIC package
- 28-pin (300 mil) CDIP and 28-pad (350 mil) LCC packages
- RoHS compliance

Functional Description

The Cypress STK11C68 is a 64Kb fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers under software control from SRAM to the nonvolatile elements (the STORE operation). On power up, data is automatically restored to the SRAM (the RECALL operation) from the nonvolatile memory. RECALL operations are also available under software control.

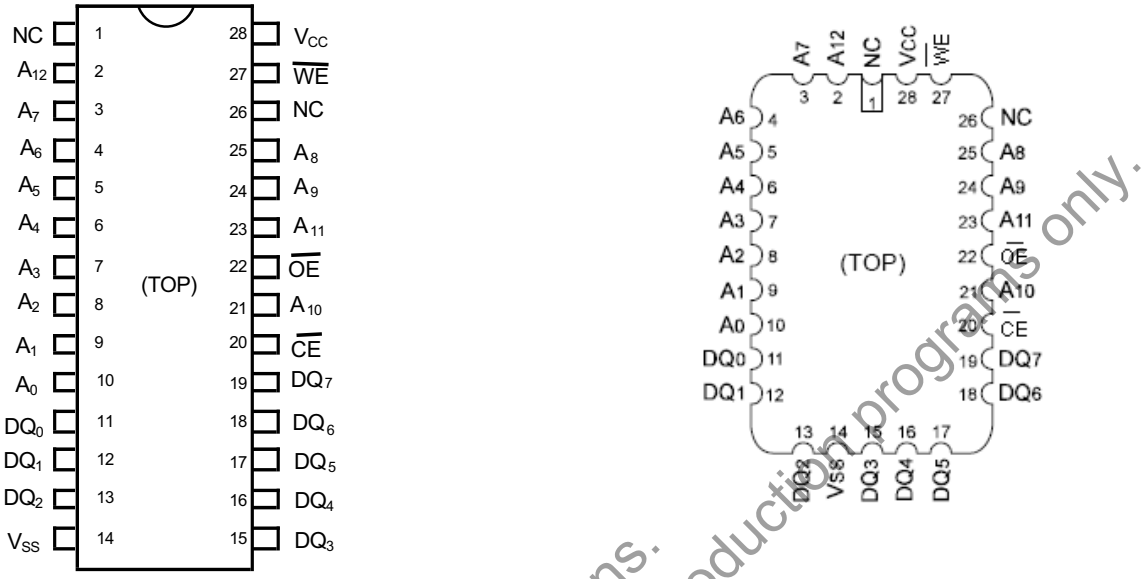
Logic Block Diagram



Contents

Pin Configurations

Figure 1. Pin Diagram - 28-Pin SOIC/DIP and 28-Pin LLC



Pin Definitions

Pin Name	Alt	I/O Type	Description
A_0–A_{12}		Input	**Address Inputs.** Used to select one of the 8,192 bytes of the nvSRAM.
DQ_0-DQ_7		Input or Output	**Bidirectional Data I/O Lines**. Used as input or output lines depending on operation.
$\overline{WE}$	$\overline{W}$	Input	**Write Enable Input, Active LOW**. When the chip is enabled and $\overline{WE}$ is LOW, data on the I/O pins is written to the specific address location.
$\overline{CE}$	$\overline{E}$	Input	**Chip Enable Input, Active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	$\overline{G}$	Input	**Output Enable, Active LOW**. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the I/O pins to tristate.
V_{SS}		Ground	**Ground for the Device**. The device is connected to ground of the system.
V_{CC}		Power Supply	**Power Supply Inputs to the Device**.

Device Operation

The STK11C68 is a versatile memory chip that provides several modes of operation. The STK16C88 can operate as a standard 8K x 8 SRAM. A 8K x 8 array of nonvolatile storage elements shadow the SRAM. SRAM data can be copied nonvolatile memory or nonvolatile data can be recalled to the SRAM.

SRAM Read

The STK11C68 performs a Read cycle whenever $\overline{CE}$ and $\overline{OE}$ are LOW while $\overline{WE}$ is HIGH. The address specified on pins $A_{0–12}$ determines the 8,192 data bytes accessed. When the Read is initiated by an address transition, the outputs are valid after a delay of t_{AA} (Read cycle 1). If the Read is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at t_{ACE} or at t_{DOE}, whichever is later (Read cycle 2). The data outputs repeatedly respond to address changes within the t_{AA} access time without the need for transitions on any control input pins, and remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ brought LOW.

SRAM Write

A Write cycle is performed whenever $\overline{CE}$ and $\overline{WE}$ are LOW. The address inputs must be stable prior to entering the Write cycle and must remain stable until either $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common I/O pins $DQ_{0–7}$ are written into the memory if it has valid t_{SD}, before the end of a $\overline{WE}$ controlled Write or before the end of an $\overline{CE}$ controlled Write. Keep $\overline{OE}$ HIGH during the entire Write cycle to avoid data bus contention on common I/O lines. If $\overline{OE}$ is left LOW, internal circuitry turns off the output buffers t_{HZWE} after $\overline{WE}$ goes LOW.

Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. The STK11C68 software STORE cycle is initiated by executing sequential $\overline{CE}$ controlled Read cycles from six specific address locations in exact order. During the STORE cycle, an erase of the previous nonvolatile data is first performed followed by a program of the nonvolatile elements. When a STORE cycle is initiated, input and output are disabled until the cycle is completed.

Because a sequence of Reads from specific addresses is used for STORE initiation, it is important that no other Read or Write accesses intervene in the sequence. If they intervene, the sequence is aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following Read sequence is performed:

1. Read address 0x0000, Valid READ
2. Read address 0x1555, Valid READ
3. Read address 0x0AAA, Valid READ
4. Read address 0x1FFF, Valid READ
5. Read address 0x10F0, Valid READ
6. Read address 0x0F0F, Initiate STORE cycle

The software sequence is clocked with $\overline{CE}$ controlled Reads. When the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. It is important that Read cycles and not Write cycles are used in the sequence. It is not necessary that $\overline{OE}$ is LOW for a valid sequence. After the t_{STORE} cycle time is fulfilled, the SRAM is again activated for Read and Write operation.

Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of Read operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of $\overline{CE}$ controlled Read operations is performed:

1. Read address 0x0000, Valid READ
2. Read address 0x1555, Valid READ
3. Read address 0x0AAA, Valid READ
4. Read address 0x1FFF, Valid READ
5. Read address 0x10F0, Valid READ
6. Read address 0x0F0E, Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared; then, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is again ready for Read and Write operations. The RECALL operation does not alter the data in the nonvolatile elements. The nonvolatile data can be recalled an unlimited number of times.

Hardware RECALL (Power Up)

During power up or after any low power condition (V_{CC} < V_{RESET}), an internal RECALL request is latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete.

If the STK11C68 is in a Write state at the end of power up RECALL, the SRAM data is corrupted. To help avoid this situation, a 10 Kohm resistor is connected either between $\overline{WE}$ and system V_{CC} or between $\overline{CE}$ and system V_{CC}.

Hardware Protect

The STK11C68 offers hardware protection against inadvertent STORE operation and SRAM Writes during low voltage conditions. When V_{CAP}<V_{SWITCH}, all externally initiated STORE operations and SRAM Writes are inhibited.

Noise Considerations

The STK11C68 is a high speed memory. It must have a high frequency bypass capacitor of approximately 0.1 µF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high speed CMOS ICs, careful routing of power, ground, and signals reduce circuit noise.

Low Average Active Power

CMOS technology provides the STK11C68 the benefit of drawing significantly less current when it is cycled at times longer than 50 ns. Figure 2 shows the relationship between I_{CC} and Read or Write cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, VCC = 5.5V, 100% duty cycle on chip enable). Only standby current is drawn when the chip is disabled.

The overall average current drawn by the STK11C68 depends on the following items:

- The duty cycle of chip enable
- The overall cycle rate for accesses
- The ratio of Reads to Writes
- CMOS versus TTL input levels
- The operating temperature
- The V_{CC} level
- I/O loading

Figure 2. Current Versus Cycle Time (Read)

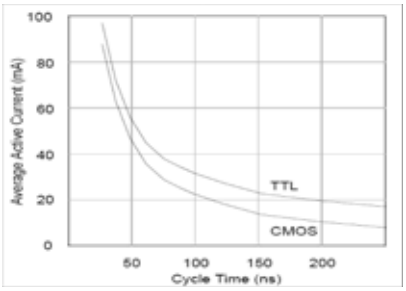
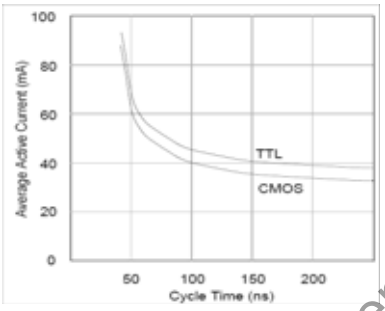


Figure 3. Current Versus Cycle Time (Write)



Best Practices

nvSRAM products have been used effectively for over 15 years. While ease of use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The nonvolatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprograms these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. The end product's firmware should not assume that an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration,
- cold or warm boot status, and so on must always program a unique NV pattern (for example, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power up boot firmware routines should rewrite the nvSRAM into the desired state. While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently (program bugs, incoming inspection routines, and so on).

Table 1. Hardware Mode Selection

$\overline{CE}$	$\overline{WE}$	A12–A0	Mode	I/O	Notes
L	H	0x0000 0x1555 0x0AAA 0x1FFF 0x10F0 0x0F0F	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output Data Output Data Output Data Output Data Output Data Output High Z	[1]
L	H	0x0000 0x1555 0x0AAA 0x1FFF 0x10F0 0x0F0E	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output Data Output Data Output Data Output Data Output Data Output High Z	[1]

Note
1. The six consecutive addresses must be in the order listed. $\overline{WE}$ must be high during all six consecutive $\overline{CE}$ controlled cycles to enable a nonvolatile cycle.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Temperature under bias..... –55°C to +125°C

Supply Voltage on V_{CC} Relative to GND .....–0.5V to 7.0V

Voltage on Input Relative to Vss..... –0.6V to V_{CC} + 0.5V

Voltage on DQ_{0-7} .....–0.5V to Vcc + 0.5V

Power Dissipation 1.0W

DC Output Current (1 output at a time, 1s duration).... 15 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	4.5V to 5.5V
Industrial	-40°C to +85°C	4.5V to 5.5V

DC Electrical Characteristics

Over the operating range (V_{CC} = 4.5V to 5.5V)

Parameter	Description	Test Conditions		Min	Max	Unit
I_{CC1}	Average V_{CC} Current	t_{RC} = 25 ns t_{RC} = 35 ns t_{RC} = 45 ns Dependent on output loading and cycle rate. Values obtained without output loads. I_{OUT} = 0 mA.	Commercial		90 75 65	mA mA mA
			Industrial		90 75 65	mA mA mA
I_{CC2}	Average V_{CC} Current during STORE	All Inputs Do Not Care, V_{CC} = Max Average current for duration t_{STORE}			3	mA
I_{CC3}	Average V_{CC} Current at t_{RC}= 200 ns, 5V, 25°C Typical	$\overline{WE} \geq (V_{CC} - 0.2V)$. All other inputs cycling. Dependent on output loading and cycle rate. Values obtained without output loads.			10	mA
I_{SB1} [2]	V_{CC} Standby Current (Standby, Cycling TTL Input Levels)	t_{RC} = 25 ns, $\overline{CE} \geq V_{IH}$ t_{RC} = 35 ns, $\overline{CE} \geq V_{IH}$ t_{RC} = 45 ns, $\overline{CE} \geq V_{IH}$	Commercial		27 23 20	mA mA mA
			Industrial		28 24 21	mA mA mA
I_{SB2} [2]	V_{CC} Standby Current	$\overline{CE} \geq (V_{CC} - 0.2V)$. All others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$. Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.	Commercial		750	µA
			Industrial		1500	µA
I_{IX}	Input Leakage Current	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$		-1	+1	µA
I_{OZ}	Off State Output Leakage Current	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$, $\overline{CE}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$		-5	+5	µA
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			V_{SS} – 0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OUT} = –4 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OUT} = 8 mA			0.4	V

Data Retention and Endurance

Parameter	Description	Min	Unit
$DATA_R$	Data Retention	100	Years
NV_C	Nonvolatile STORE Operations	1,000	K

Note

2. $\overline{CE} \geq V_{IH}$ does not produce standby current levels until any nonvolatile cycle in progress has timed out.

Capacitance

In the following table, the capacitance parameters are listed.[3]

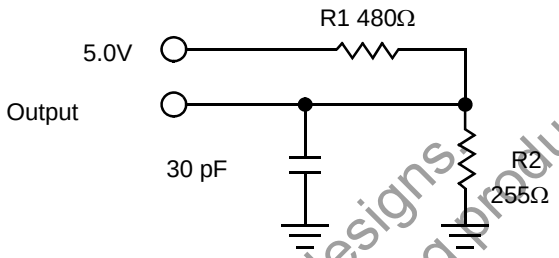
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 0 to 3.0V	8	pF
C_{OUT}	Output Capacitance		7	pF

Thermal Resistance

In the following table, the thermal resistance parameters are listed.[3]

Parameter	Description	Test Conditions	28-SOIC	28-CDIP	28-LCC	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	TBD	TBD	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		TBD	TBD	TBD	°C/W

Figure 4. AC Test Loads



AC Test Conditions

Input Pulse Levels ..... 0V to 3V
Input Rise and Fall Times (10% to 90%) ..... ≤5 ns
Input and Output Timing Reference Levels 1.5V

Note
3. These parameters are guaranteed by design and are not tested.

AC Switching Characteristics

SRAM Read Cycle

Parameter		Description	25 ns		35 ns		45 ns		Unit
Cypress Parameter	Alt		Min	Max	Min	Max	Min	Max	
t_{ACE}	t_{ELQV}	Chip Enable Access Time		25		35		45	ns
t_{RC} [4]	t_{AVAV}, t_{ELEH}	Read Cycle Time	25		35		45		ns
t_{AA} [5]	t_{AVQV}	Address Access Time		25		35		45	ns
t_{DOE}	t_{GLQV}	Output Enable to Data Valid		10		15		20	ns
t_{OHA} [5]	t_{AXQX}	Output Hold After Address Change	5		5		5		ns
t_{LZCE} [6]	t_{ELQX}	Chip Enable to Output Active	5		5		5		ns
t_{HZCE} [6]	t_{EHQZ}	Chip Disable to Output Inactive		10		13		15	ns
t_{LZOE} [6]	t_{GLQX}	Output Enable to Output Active	0		0		0		ns
t_{HZOE} [6]	t_{GHQZ}	Output Disable to Output Inactive		10		13		15	ns
t_{PU} [3]	t_{ELICCH}	Chip Enable to Power Active	0		0		0		ns
t_{PD} [3]	t_{EHICCL}	Chip Disable to Power Standby		25		35		45	ns

Switching Waveforms

Figure 5. SRAM Read Cycle 1: Address Controlled [4, 5]

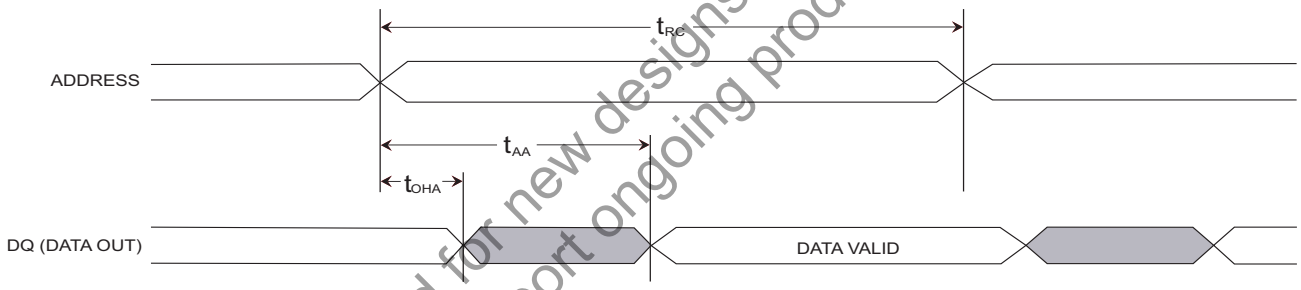
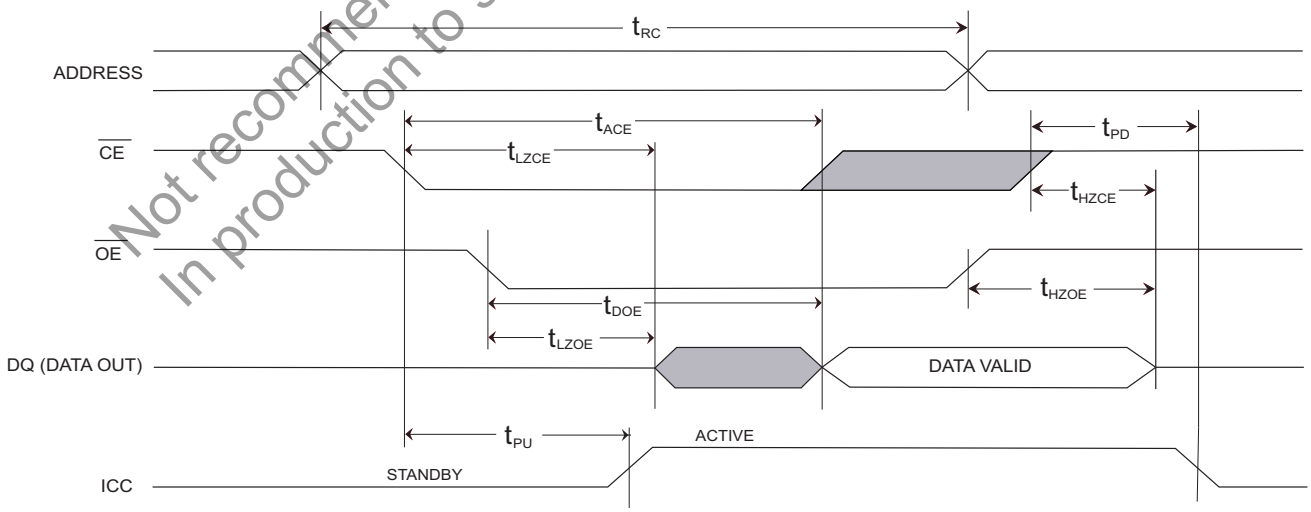


Figure 6. SRAM Read Cycle 2: $\overline{CE}$ and $\overline{OE}$ Controlled [4]



Notes
4. $\overline{WE}$ must be High during SRAM Read cycles.
5. I/O state assumes $\overline{CE}$ and $\overline{OE} \leq V_{IL}$ and $\overline{WE} \geq V_{IH}$; device is continuously selected.
6. Measured ±200 mV from steady state output voltage.

SRAM Write Cycle

Parameter		Description	25 ns		35 ns		45 ns		Unit
Cypress Parameter	Alt		Min	Max	Min	Max	Min	Max	
t_{WC}	t_{AVAV}	Write Cycle Time	25		35		45		ns
t_{PWE}	t_{WLWH}, t_{WLEH}	Write Pulse Width	20		25		30		ns
t_{SCE}	t_{ELWH}, t_{ELEH}	Chip Enable To End of Write	20		25		30		ns
t_{SD}	t_{DVWH}, t_{DVEH}	Data Setup to End of Write	10		12		15		ns
t_{HD}	t_{WHDX}, t_{EHDX}	Data Hold After End of Write	0		0		0		ns
t_{AW}	t_{AVWH}, t_{AVEH}	Address Setup to End of Write	20		25		30		ns
t_{SA}	t_{AVWL}, t_{AVEL}	Address Setup to Start of Write	0		0		0		ns
t_{HA}	t_{WHAX}, t_{EHAX}	Address Hold After End of Write	0		0		0		ns
t_{HZWE} [6,7]	t_{WLQZ}	Write Enable to Output Disable		10		13		15	ns
t_{LZWE} [6]	t_{WHQX}	Output Active After End of Write	5		5		5		ns

Switching Waveforms

Figure 7. SRAM Write Cycle 1: $\overline{WE}$ Controlled [7, 8]

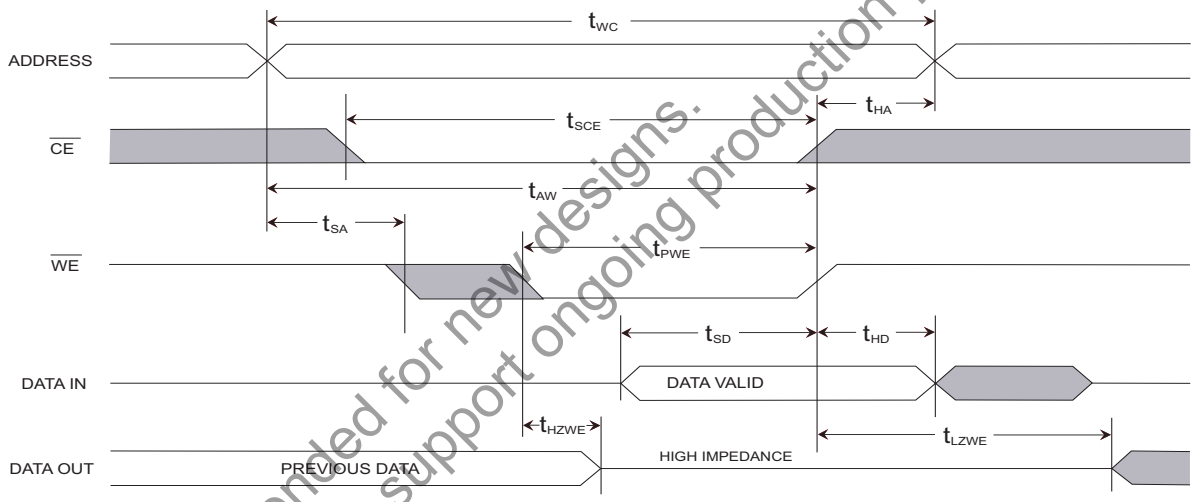
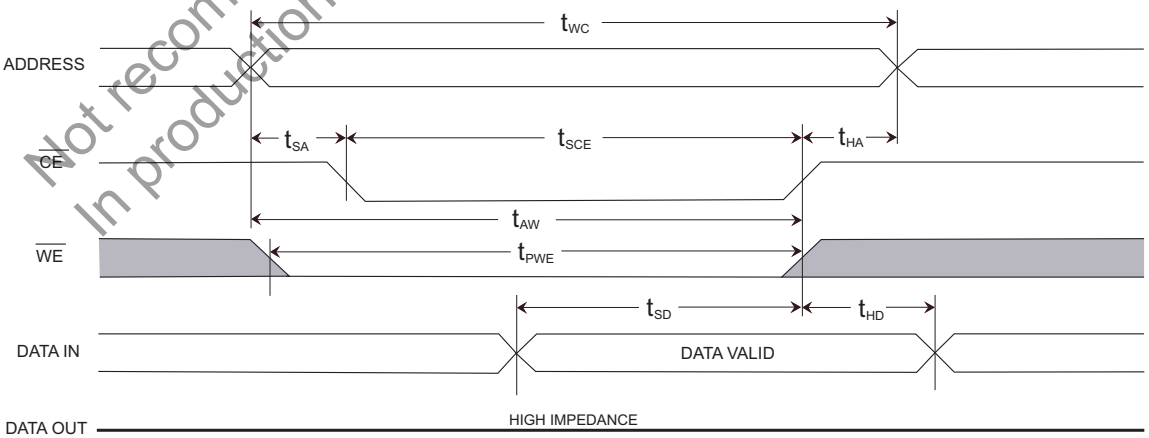


Figure 8. SRAM Write Cycle 2: $\overline{CE}$ and $\overline{OE}$ Controlled [7, 8]



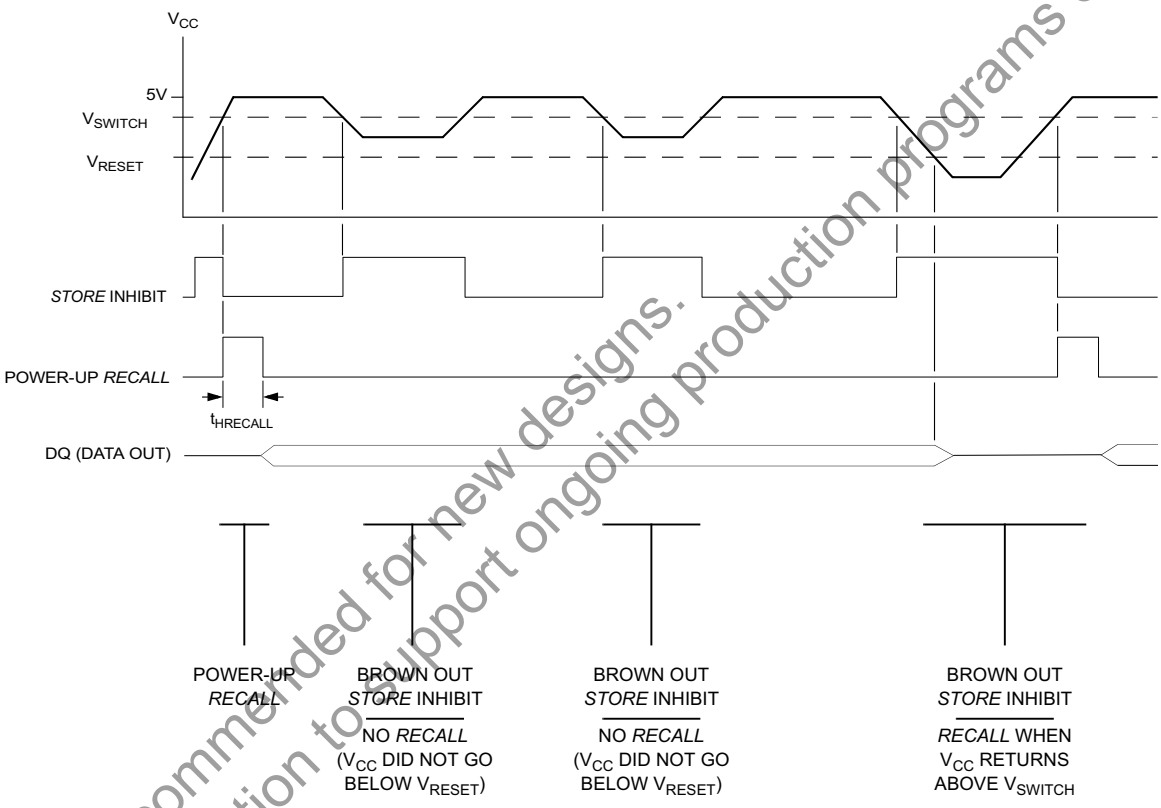
Notes
7. If $\overline{WE}$ is Low when $\overline{CE}$ goes Low, the outputs remain in the high impedance state.
8. $\overline{CE}$ or $\overline{WE}$ must be greater than V_{IH} during address transitions.

AutoStore INHIBIT or Power Up RECALL

Parameter	Alt	Description	STK11C68		Unit
			Min	Max	
$t_{HRECALL}$ [9]	$t_{RESTORE}$	Power up RECALL Duration		550	µs
t_{STORE}	t_{HLHZ}	STORE Cycle Duration		10	ms
V_{SWITCH}		Low Voltage Trigger Level	4.0	4.5	V
V_{RESET}		Low Voltage Reset Level		3.6	V

Switching Waveform

Figure 9. AutoStore INHIBIT/Power Up RECALL



Note

9. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.

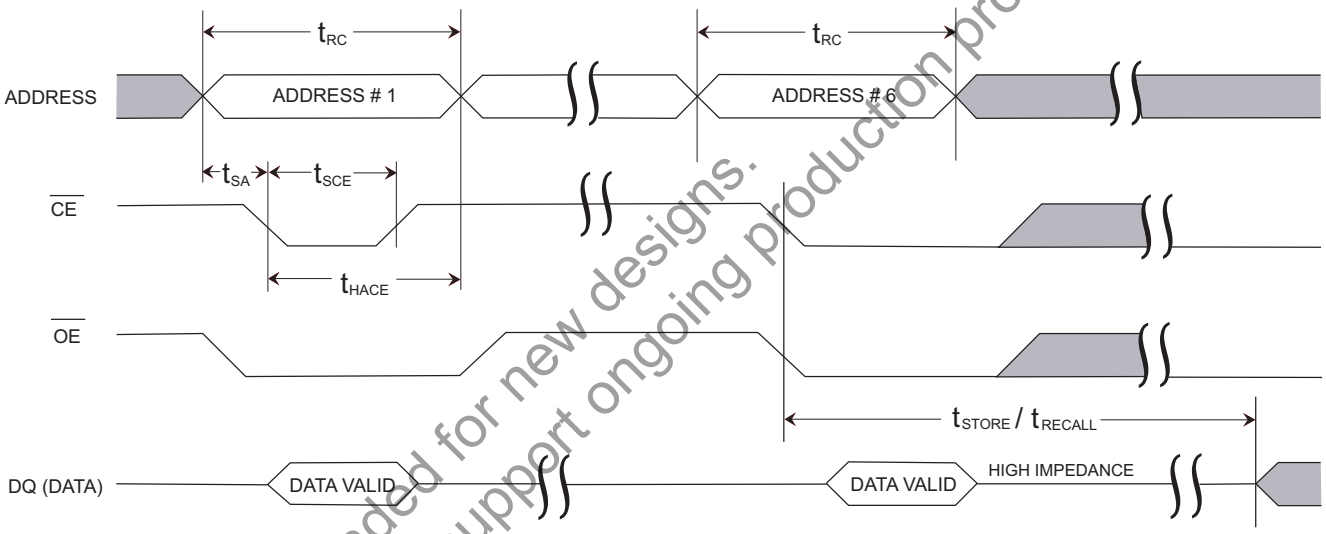
Software Controlled STORE/RECALL Cycle

The software controlled STORE/RECALL cycle follows. [10, 11]

Parameter	Alt	Description	25 ns		35 ns		45 ns		Unit
			Min	Max	Min	Max	Min	Max	
t_{RC}	t_{AVAV}	STORE/RECALL Initiation Cycle Time	25		35		45		ns
t_{SA}[10]	t_{AVEL}	Address Setup Time	0		0		0		ns
t_{CW}[10]	t_{ELEH}	Clock Pulse Width	20		25		30		ns
t_{HACE}[10]	t_{ELAX}	Address Hold Time	20		20		20		ns
t_{RECALL}[10]		RECALL Duration		20		20		20	µs

Switching Waveform

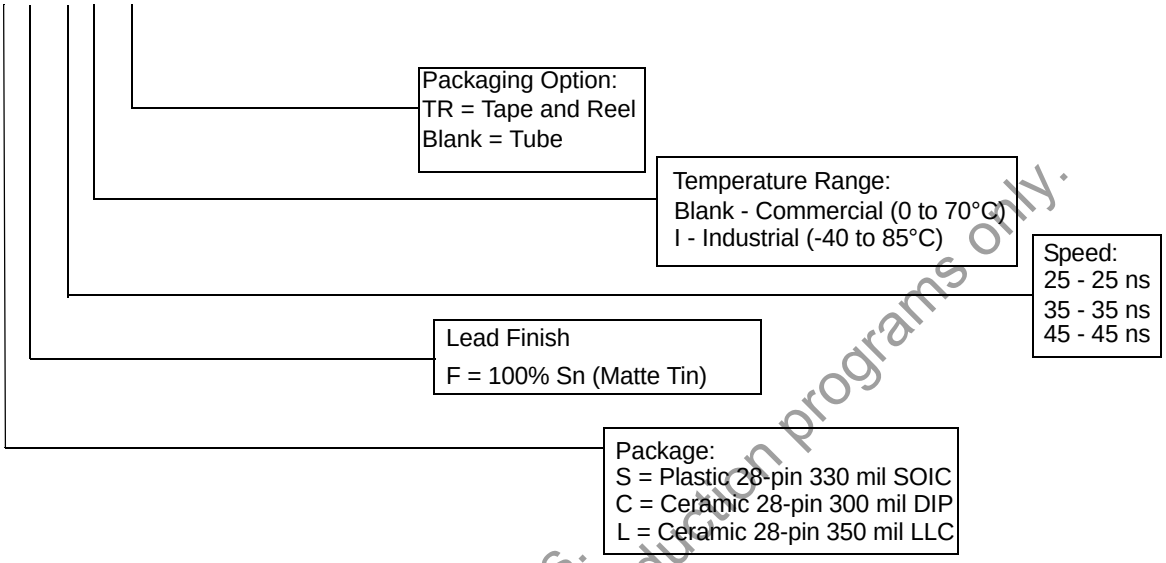
Figure 10. $\overline{CE}$ Controlled Software STORE/RECALL Cycle [11]



Notes
10. The software sequence is clocked on the falling edge of $\overline{CE}$ without involving $\overline{OE}$ (double clocking aborts the sequence).
11. The six consecutive addresses must be read in the order listed in Table 1 on page 5. $\overline{WE}$ must be HIGH during all six consecutive cycles.

Part Numbering Nomenclature

STK11C68 - S F 45 I TR



Ordering Information

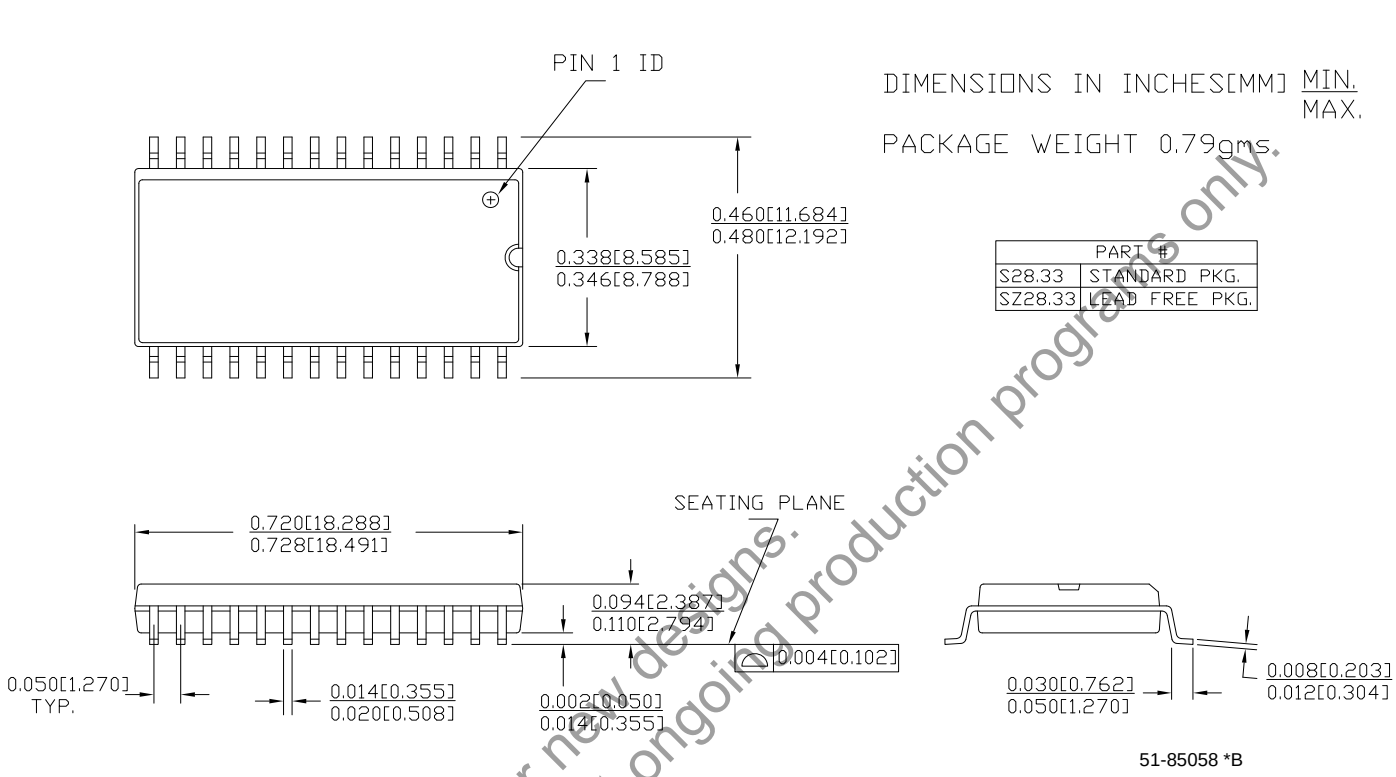
These parts are not recommended for new designs. They are in production to support ongoing production programs only.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	STK11C68-SF25TR	51-85058	28-Pin SOIC (330 mil)	Commercial
	STK11C68-SF25	51-85058	28-Pin SOIC (330 mil)	
	STK11C68-SF25ITR	51-85058	28-Pin SOIC (330 mil)	Industrial
	STK11C68-SF25I	51-85058	28-Pin SOIC (330 mil)	
35	STK11C68-L35	001-51696	28-Pin LCC (350 mil)	Commercial
35	STK11C68-C35I	001-51695	28-Pin CDIP (300 mil)	Industrial
	STK11C68-L35I	001-51696	28-Pin LCC (350 mil)	
45	STK11C68-SF45TR	51-85058	28-Pin SOIC (330 mil)	
	STK11C68-SF45	51-85058	28-Pin SOIC (330 mil)	
	STK11C68-L45	001-51696	28-Pin LCC (350 mil)	Commercial
	STK11C68-SF45ITR	51-85058	28-Pin SOIC (330 mil)	Industrial
	STK11C68-SF45I	51-85058	28-Pin SOIC (330 mil)	
	STK11C68-L45I	001-51696	28-Pin LCC (350 mil)	

All parts are Pb-free. The above table contains Final information. Contact your local Cypress sales representative for availability of these parts

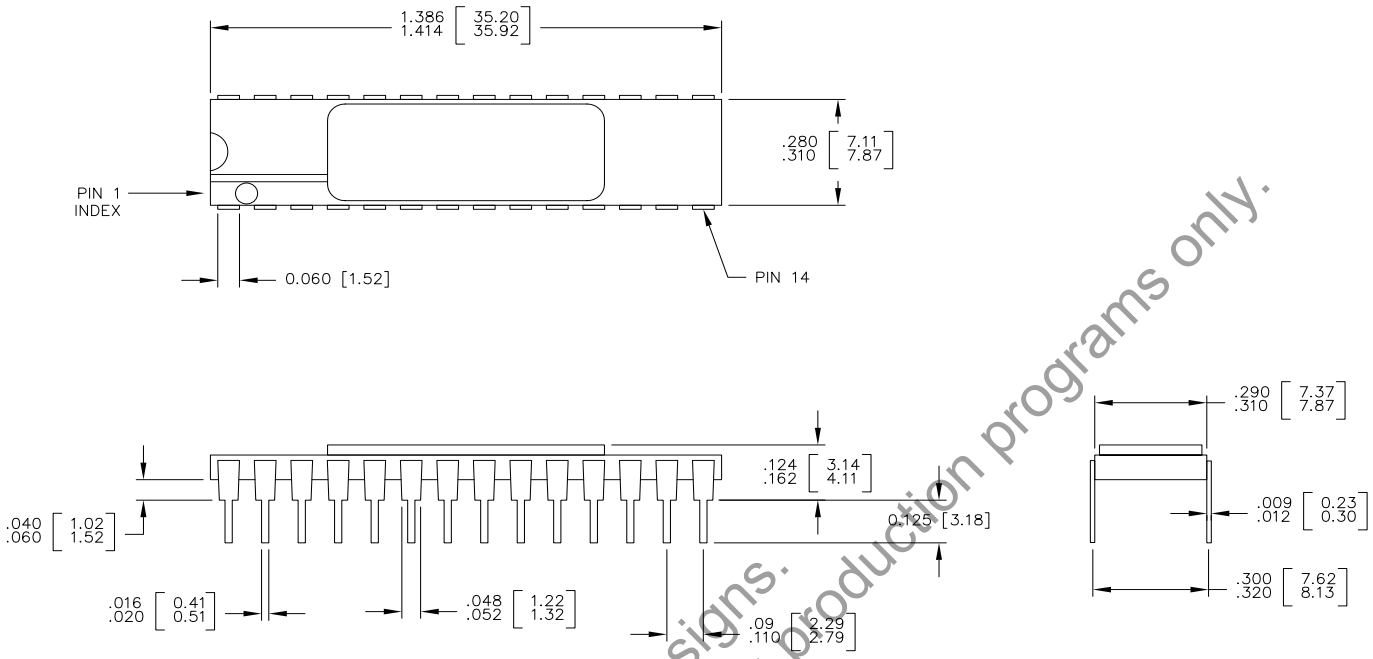
Package Diagrams

Figure 11. 28-Pin (330 Mil) SOIC (51-85058)



Package Diagrams (continued)

Figure 12. 28-Pin (300 Mil) Side Braze DIL (001-51695)

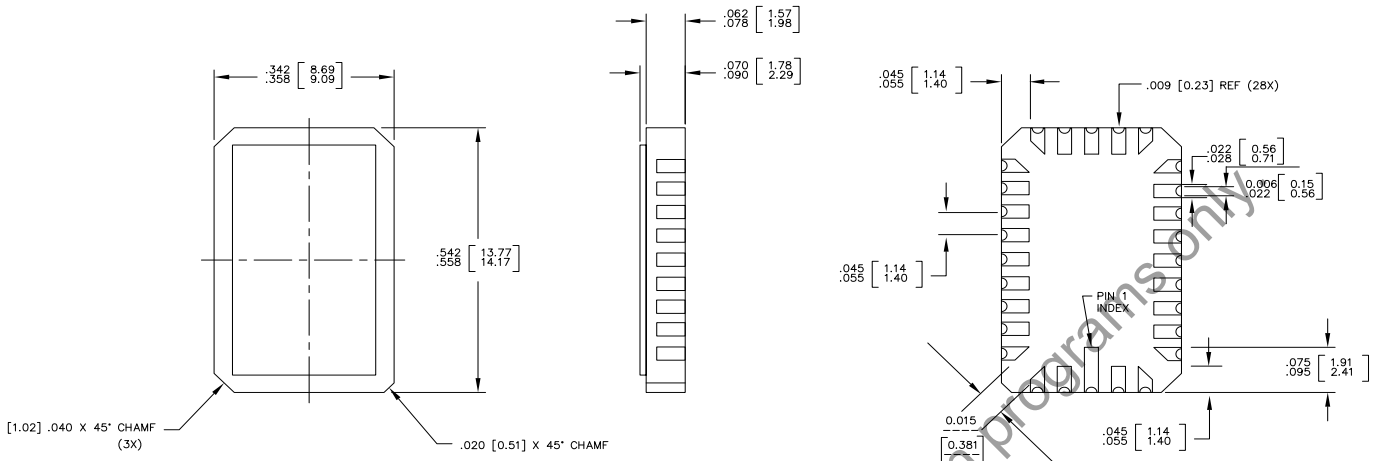


1. ALL DIMENSIONS ARE IN MILLIMETERS AND INCHS [MIN/MAX]
2. PACKAGE WEIGHT : TBD
3. JEDEC REFERENCE : MO–058

001-51695 *A

Package Diagrams (continued)

Figure 13. 28-Pad (350 Mil) LCC (001-51696)



1. ALL DIMENSION ARE IN INCHES AND MILLIMETERS [MIN/MAX]
2. JEDEC 95 OUTLINE# MO-041
3. PACKAGE WEIGHT : TBD

001-51696 *A

Document History Page

Document Title: STK11C68 64 Kbit (8K x 8) SoftStore nvSRAM Document Number: 001-50638				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2625084	GVCH/PYRS	01/30/09	New data sheet
*A	2826441	GVCH	12/11/2009	Added following text in the Ordering Information section: “These parts are not recommended for new designs. In production to support ongoing production programs only.” Added watermark in PDF stating “Not recommended for new designs. In production to support ongoing production programs only.” Added Contents on page 2.
*B	2902591	GVCH	04/05/2010	Removed inactive parts from Ordering Information. Updated Package Diagrams.

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