AMD ꓵ

Am29LV004T/Am29LV004B

4 Megabit (524,288 x 8-Bit) CMOS 3.0 Volt-only Sector Architecture Flash Memory

DISTINCTIVE CHARACTERISTICS

- ■ **Extended operating voltage range**
  - — 2.7 to 3.6 V for read and write operations
- ■ **Compatibility with JEDEC standards**
  - — Pinout and software compatible with single-power-supply Flash
  - — Superior inadvertent write protection
- ■ **Package options**
  - — 40-pin TSOP
  - — 44-pin SO
- ■ **Minimum 100,000 write/erase cycles guaranteed**
- ■ **High performance**
  - — Access times as fast as 100 ns
- ■ **Flexible, sector architecture**
  - — One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and seven 64 Kbyte sectors
- ■ **Embedded Erase™ algorithm**
  - — Automatically pre-programs and erases the chip or sector
- ■ **Embedded Program™ algorithm**
  - — Automatically writes and verifies data at specified address

- ■ **$\overline{\text{Data}}$ Polling and toggle bit**
  - — Detects program and erase cycle completion
- ■ **Ready/Busy output**
  - — Hardware method for detection of program or erase cycle completion
- ■ **Erase Suspend/Resume**
  - — Supports reading or programming to a non-busy sector
- ■ **Low current consumption (typical values at 5 MHz)**
  - — 10 mA active read current (word or byte mode)
  - — 20 mA program/erase current
- ■ **Advanced power management**
  - — 1 µA typical in standby mode
  - — 1 µA typical in automatic sleep mode
- ■ **Sector protection**
  - — Hardware method that disables any combination of sectors from write or erase operations
- ■ **Hardware reset pin**
  - — Resets the internal state machine to the read mode
- ■ **Top or bottom boot block configurations available**

GENERAL DESCRIPTION

The Am29LV004 is a 4 megabit, 3.0 Volt-only Flash memory organized as 512 Kbyte x 8. Table 1 shows how the Am29LV004 can be organized for top or bottom boot sector configuration.

Table 1. Sector Organization

Top Boot	Bottom Boot
One 16K Byte	Seven 64K Bytes
Two 8K Bytes	One 32K Byte
One 32K Byte	Two 8K Bytes
Seven 64K Bytes	One 16K Byte

The Am29LV004 is offered in 40-pin TSOP and 44-pin SO packages. Program and erase operations can be performed in-system with a standard 2.7 to 3.6 V V$_{CC}$ supply. The device can also be programmmed in industry-standard EPROM programming equipment.

The Am29LV004 offers access times of 100, 120, and 150 nanoseconds, allowing high speed microprocessors to operate with zero or minimum wait states. To eliminate bus contention, the Am29LV004 has separate chip enable ($\overline{\text{CE}}$), write enable ($\overline{\text{WE}}$), and output enable ($\overline{\text{OE}}$) controls. The Am29LV004 is entirely command-set compatible with the JEDEC single power supply Flash standard. Commands are written to the command register using standard microprocessor

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write timings. Register contents serve as input to an internal state machine that controls the erase and program circuitry. Write cycles internally latch addresses and data needed for programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM like devices.

The Am29LV004 is programmed by executing the program command sequence. This invokes the Embedded Program algorithm, which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Erase is accomplished by executing the erase command sequence. This invokes the Embedded Erase algorithm, an internal algorithm that automatically pre-programs the array, if not already programmed, before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The Am29LV004 also features hardware sector protection, implemented via external programming equipment, which disables program and erase operations in specified sectors. AMD has implemented an Erase Suspend feature which enables the user to suspend

erase for any period of time to read data from, or program data to, a sector not being erased. Thus a true background erase can be achieved.

The device features single-power-supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations during loss of power. The end of program or erase is detected by the Ready/Busy pin, $\overline{\text{Data}}$ polling of DQ7, or by the toggle bit (DQ6). Once the end of a program or erase cycle has been detected, the access for a new read, program, or erase can begin.

The Flash technology developed by AMD combines years of EPROM and EEPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am29LV004 Flash memory electrically erases the entire device or a specified sector simultaneously via Fowler-Nordheim tunneling. The bytes are programmed using the EPROM programming mechanism of hot electron injection.
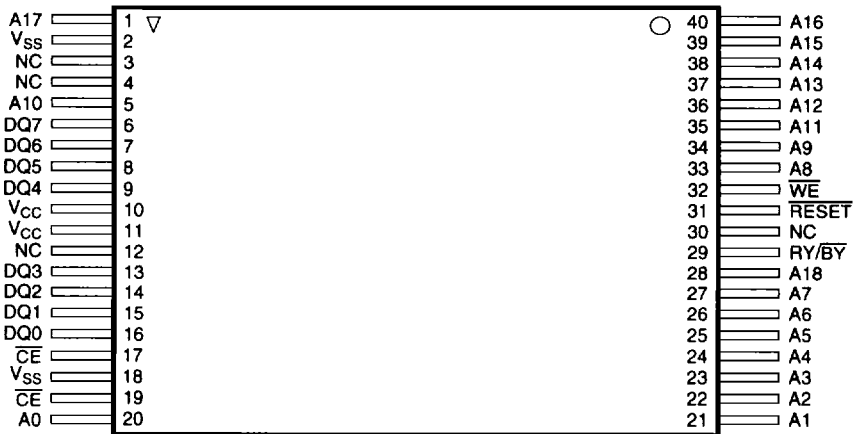
BLOCK DIAGRAM
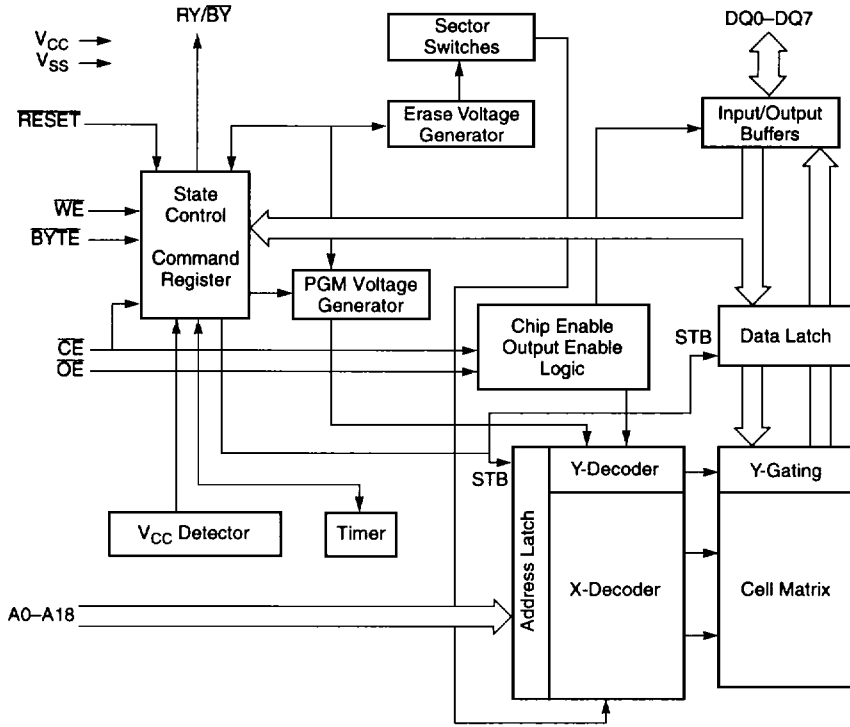
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PRODUCT SELECTOR GUIDE

Family Part Number	Am29LV004T/Am29LV004B		
Ordering Part Number V_{CC} = 3.0 V +20%, −10%	**-100**	**-120**	**-150**
Max access time (ns)	100	120	150
$\overline{CE}$ access time (ns)	100	120	150
$\overline{OE}$ access time (ns)	35	50	50

CONNECTION DIAGRAMS

Standard 40-Pin TSOP

Reverse 40-Pin TSOP

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CONNECTION DIAGRAMS (continued)

|			
NC	1	44	$\overline{RESET}$
RY/$\overline{BY}$	2	43	$\overline{WE}$
A18	3	42	A8
A7	4	41	A9
A6	5	40	A11
A5	6	39	A12
A4	7	38	A13
A3	8	37	A14
A2	9	36	A15
A1	10	35	A16
A0	11	34	A17
$\overline{CE}$	12	33	NC
V_{SS}	13	32	V_{SS}
$\overline{OE}$	14	31	NC
DQ0	15	30	A10
NC	16	29	DQ7
DQ1	17	28	DQ6
NC	18	27	NC
DQ2	19	26	DQ5
NC	20	25	NC
DQ3	21	24	DQ4
V_{CC}	22	23	V_{CC}
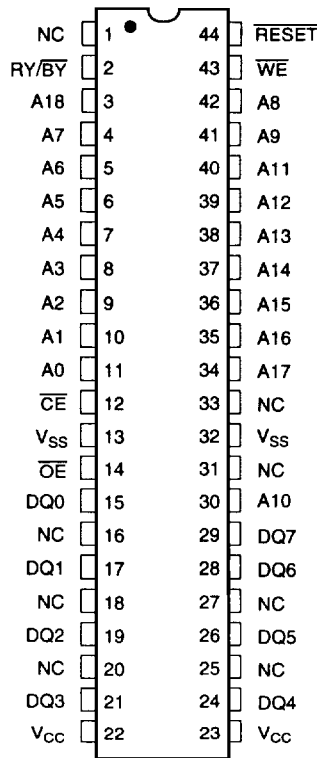
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44-Pin SO

PIN CONFIGURATION

A0–A18 = 19 addresses

DQ0–DQ7 = 8 data inputs/outputs

$\overline{CE}$ = Chip enable

$\overline{WE}$ = Write enable

$\overline{OE}$ = Output enable

$\overline{RESET}$ = Reset pin

RY/$\overline{BY}$ = Ready/$\overline{Busy}$ pin

V_{CC} = +3.0 volt single power supply (+20%/–10% for -100, -120, -150)

V_{SS} = Device ground
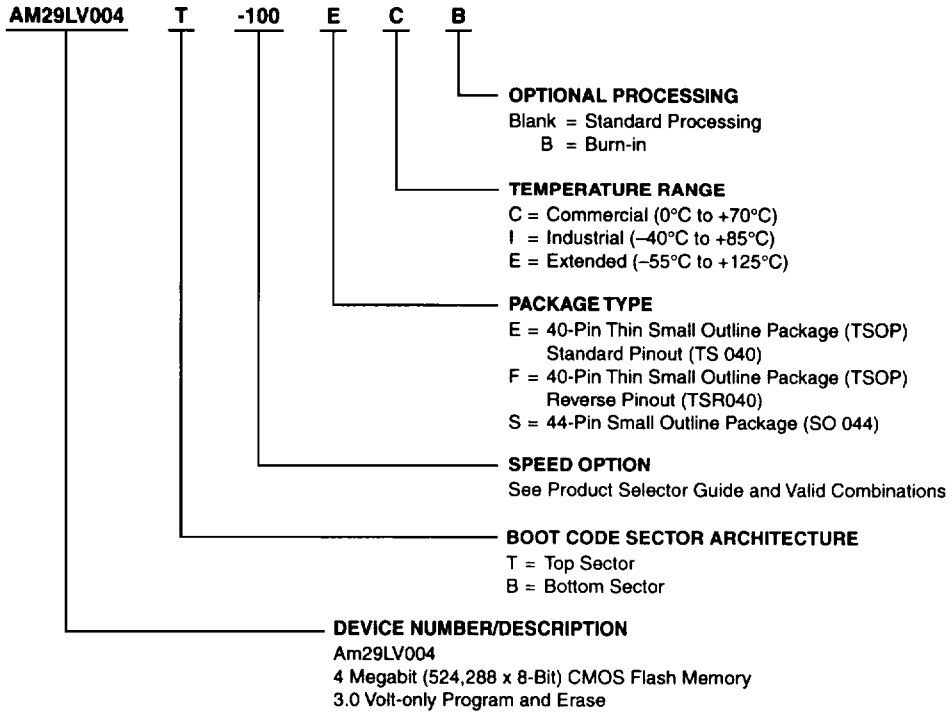
NC = Pin not connected

LOGIC SYMBOL
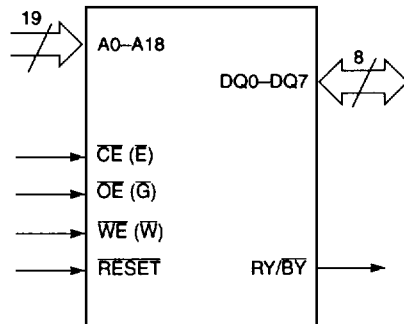
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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

AM29LV004   T   -100   E   C   B

OPTIONAL PROCESSING
Blank = Standard Processing
   B = Burn-in

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)
E = Extended (–55°C to +125°C)

PACKAGE TYPE
E = 40-Pin Thin Small Outline Package (TSOP)
    Standard Pinout (TS 040)
F = 40-Pin Thin Small Outline Package (TSOP)
    Reverse Pinout (TSR040)
S = 44-Pin Small Outline Package (SO 044)

SPEED OPTION
See Product Selector Guide and Valid Combinations

BOOT CODE SECTOR ARCHITECTURE
T = Top Sector
B = Bottom Sector

DEVICE NUMBER/DESCRIPTION
Am29LV004
4 Megabit (524,288 x 8-Bit) CMOS Flash Memory
3.0 Volt-only Program and Erase

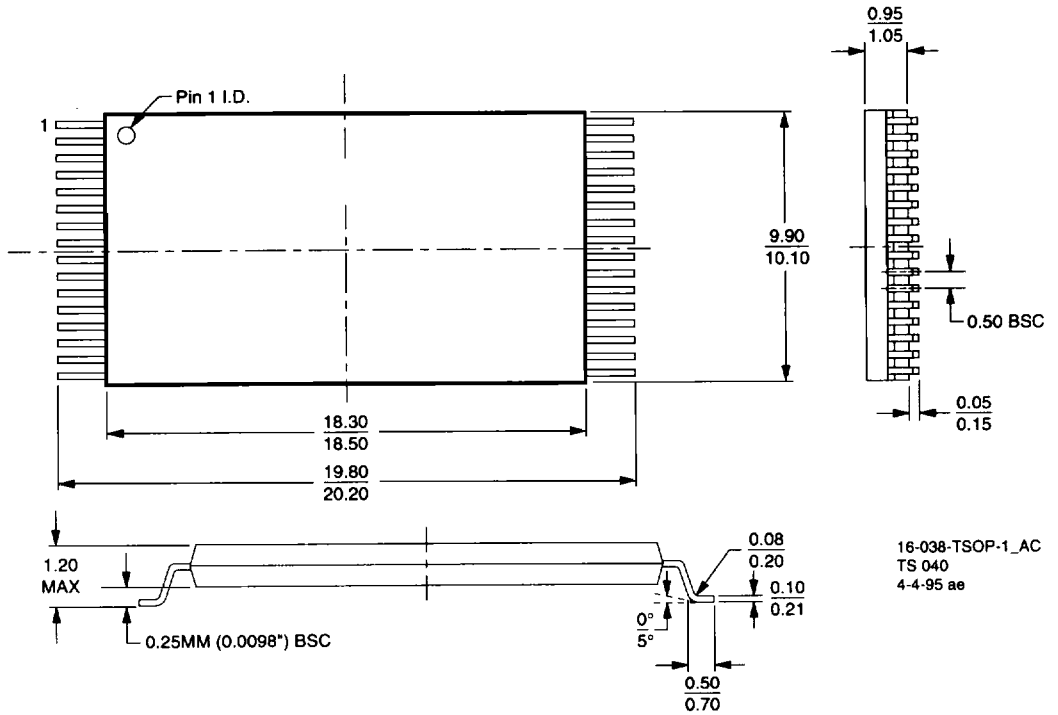| Valid Combinations	
AM29LV004T/B-100	EC, FC, SC
AM29LV004T/B-120	EC, EI, EE, EEB, FC, FI, FE, FEB, SC, SI, SE, SEB
AM29LV004T/B-150	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PHYSICAL DIMENSIONS*
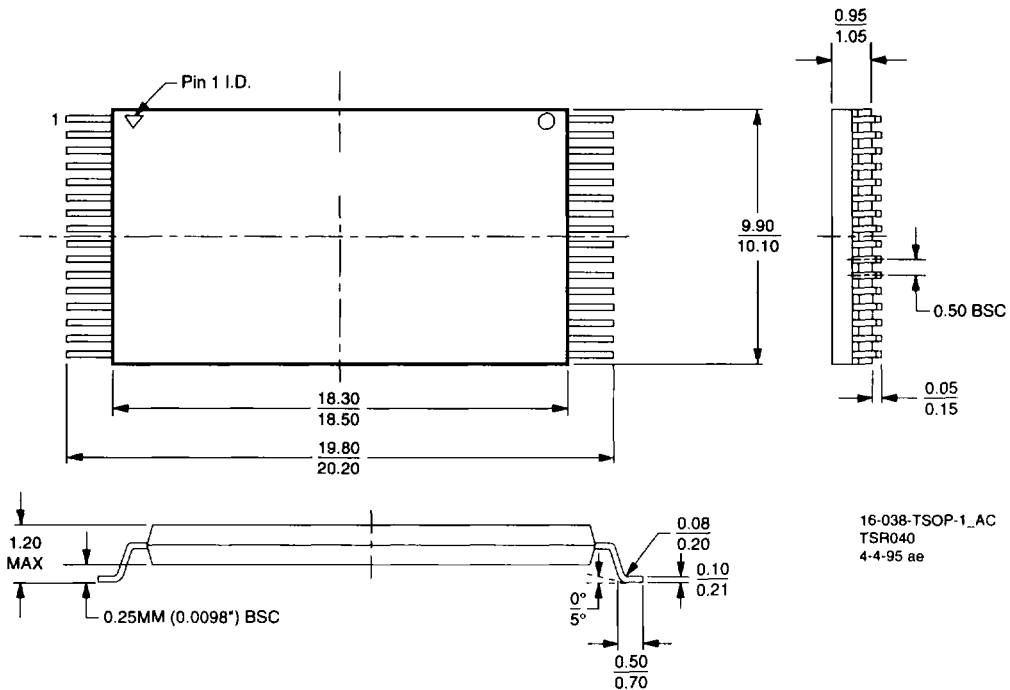## TS 040
40-Pin (measured in millimeters)

Pin 1 I.D.

$\frac{0.95}{1.05}$

$\frac{9.90}{10.10}$

0.50 BSC

$\frac{0.05}{0.15}$

$\frac{18.30}{18.50}$

$\frac{19.80}{20.20}$

1.20 MAX

0.25MM (0.0098") BSC

$\frac{0.08}{0.20}$

$\frac{0.10}{0.21}$

0°
5°

$\frac{0.50}{0.70}$

16-038-TSOP-1_AC
TS 040
4-4-95 ae

* For reference only. BSC is an ANSI standard for Basic Space Centering.
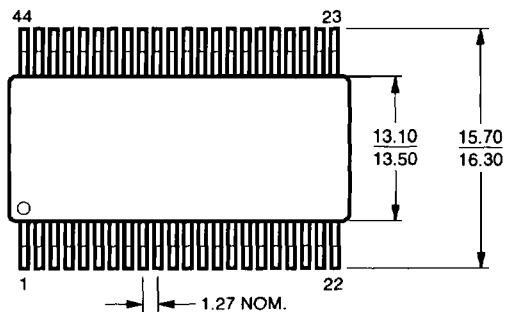
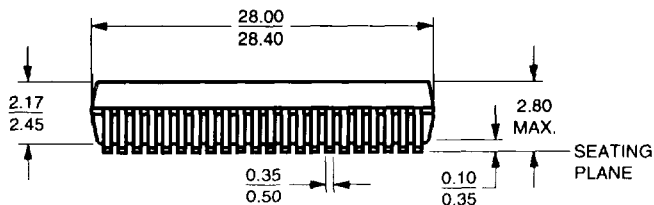## PHYSICAL DIMENSIONS (continued)
TSR040
40-Pin (measured in millimeters)

0.95
1.05

Pin 1 I.D.

9.90
10.10

0.50 BSC

0.05
0.15

18.30
18.50

19.80
20.20

0.08
0.20

0.10
0.21

16-038-TSOP-1_AC
TSR040
4-4-95 ae

1.20
MAX

0.25MM (0.0098") BSC

0°
5°

0.50
0.70

PHYSICAL DIMENSIONS (continued)
SO 044
44-Pin (measured in millimeters)

TOP VIEW

SIDE VIEW
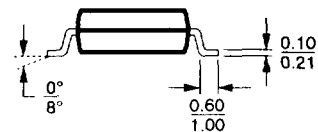
END VIEW

16-038-SO44-2
SO 044
DA82
11-9-95 lv

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