

Description

The HY23V08000 high performance read only memory is organized 1,048,576 x 8 bit (byte mode) and has an access time of 70/100/120ns. The low power feature allows the battery operation. The large size of 8M bit memory density is ideal for character generator, data or program memory in micro-processor application. The HY23V08000 is packaged 32pin DIP or 32 pin SOP.

Key features

- 1,048,576 X 8bit organization
- Single 3.3V power supply operation
- Access Time : 70/100/120ns (Max)
- Standby Current : 50 μ A (Max)
- Operating Current : 35mA (Max)
- TTL compatible inputs and outputs
- 3-State outputs for wired-OR expansion
- Programmable CE or OE pin
- Fully static operation
- Package
HY23V08000D : 32pin Plastic DIP(600 mil)
HY23V08000S : 32pin Plastic SOP(500mil)

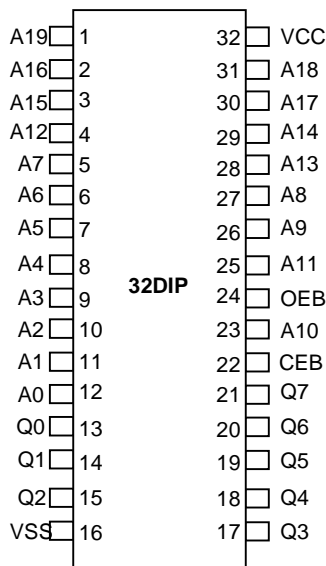
Pin Description

| Pin | Function |
|--------|---------------------|
| A0~A19 | Address inputs |
| Q0~Q7 | Data Outputs |
| CEB* | Chip Enable input |
| OEB* | Output Enable input |
| VCC | Power supply |
| VSS | Ground |

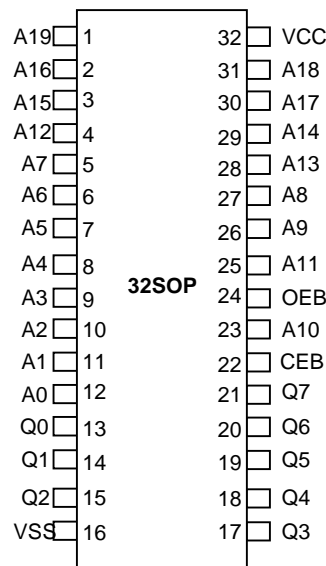
* User selectable polarity

- CEB : CE/CEB
- OEB : OE/OEB

Pin Configuration

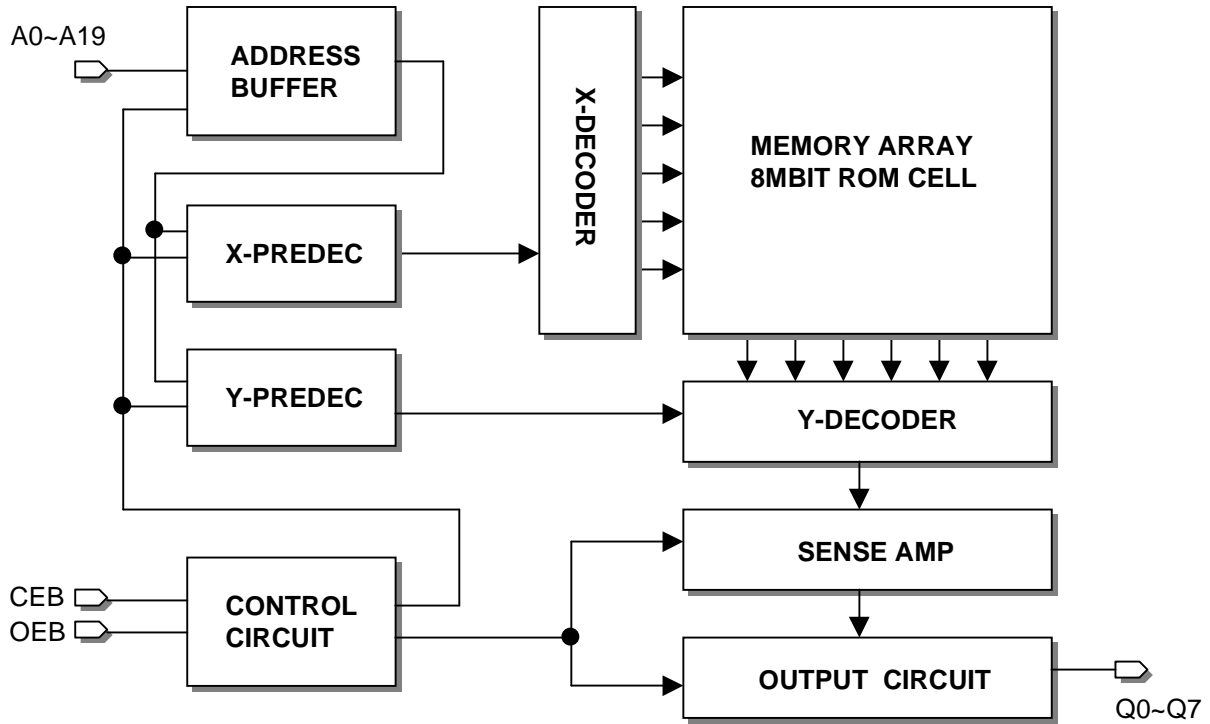


HY23V08000D



HY23V08000S

Block Diagram



□ Absolute Maximum Ratings

| Symbol | Parameter | Rating | Unit |
|--------|------------------------------------|--------------|------|
| TA | Ambient Operating Temperature | -10 ~ 80 | °C |
| TSTG | Storage Temperature | -55 ~ 150 | °C |
| VCC | Supply Voltage to Ground Potential | -0.3 ~ 4.5 | V |
| VOUT | Output Voltage | -0.3~Vcc+0.3 | V |
| VIN | Input Voltage | -0.3~Vcc+0.3 | V |

Stress above those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

□ Recommended DC Operating Conditions(VCC=3.3±0.3V, TA=0~70°C)

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------|--------------------|------|-----|---------|------|
| Vcc | Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| Vss | Supply Voltage | 0 | 0 | 0 | V |
| VIH | Input High Voltage | 2.2 | | Vcc+0.3 | V |
| VIL | Input Low Voltage | -0.3 | | 0.8 | V |

□ DC Electrical Characteristics(VCC=3.3±0.3V, TA=0~70 °C)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|---|--------------------------------|-----|-----|-----|------|
| VOH | Output High Voltage | IOH=-0.4mA | 2.4 | | | V |
| VOL | Output Low Voltage | IOL=2.1mA | | | 0.4 | V |
| IIL | Input Leakage Current | VIN=0V to VCC | | | ±10 | uA |
| IOL | Output Leakage Current | VOUT=0V to VCC | | | ±10 | uA |
| ICC | Operating Supply Current (tRC=100ns) | CEB=OEB=VIL All Output Open | | | 35 | mA |
| ISB1 | Standby Current(TTL) | CEB=VIH, all Output Open | | | 500 | uA |
| ISB2 | Standby Current(CMOS) | CEB=VCC, all Output Open | | | 50 | uA |

Capacitance($T_A=25^\circ\text{C}$, $f=1.0\text{MHz}$)

| Symbol | Parameter | Condition | Min | Max | Unit |
|----------------|--------------------|-----------------------|-----|-----|------|
| C _I | Input Capacitance | V _{IN} = 0V | | 10 | pF |
| C _O | Output Capacitance | V _{OUT} = 0V | | 10 | pF |

Capacitance is periodically sampled and not 100% tested

Function Table

| CE/ $\overline{\text{CE}}$ | OE/ $\overline{\text{OE}}$ | Mode | Data | Power |
|----------------------------|----------------------------|----------------|--------|---------|
| L/H | X | Standby | High Z | Standby |
| H/L | H/L | Operating | DOUT | Active |
| | L/H | Output Disable | High Z | |

AC Characteristics($V_{CC}=3.3\pm 0.3\text{V}$, $T_A=0\sim 70^\circ\text{C}$)

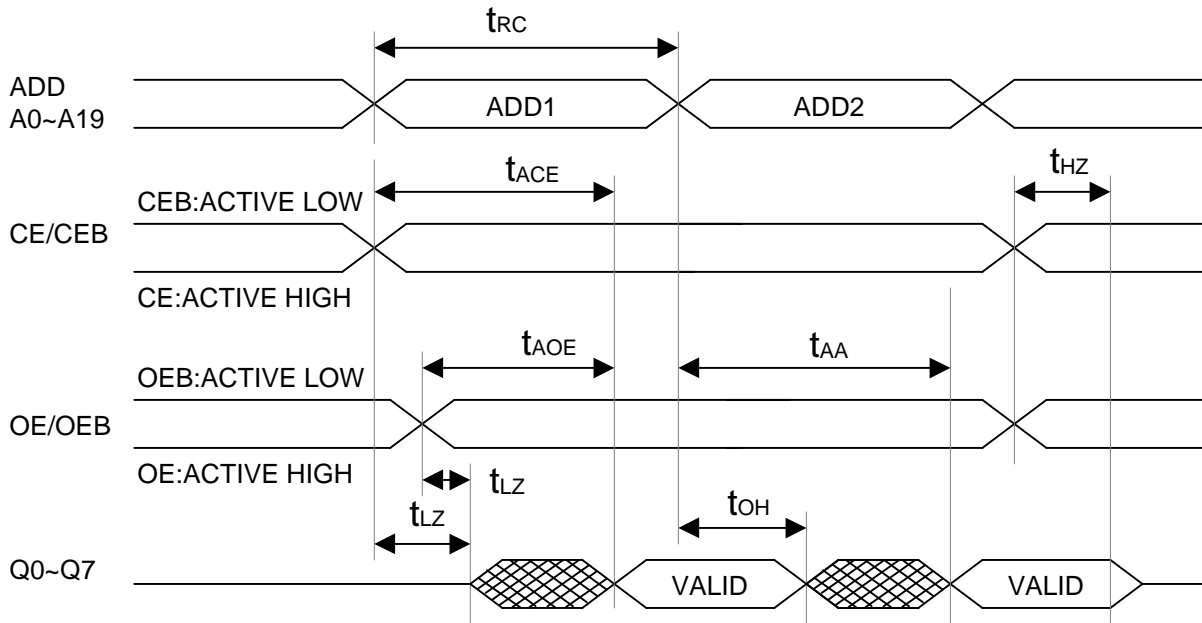
| Symbol | Parameter | 70ns | | 100ns | | 120ns | | Unit |
|------------------|---|------|-----|-------|-----|-------|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| t _{RC} | Read cycle time | 70 | | 100 | | 120 | | ns |
| t _{ACE} | Chip enable access time | | 70 | | 100 | | 120 | ns |
| t _{AA} | Address access time | | 70 | | 100 | | 120 | ns |
| t _{AOE} | Output enable access time | | 35 | | 50 | | 60 | ns |
| t _{OH} | Output hold time from address change | 0 | | 0 | | 0 | | ns |
| t _{HZ} | Output or chip disable to output High-Z | | 20 | | 20 | | 20 | ns |
| t _{LZ} | Output or chip Enable to output Low-Z | 10 | | 10 | | 10 | | ns |

AC Test Condition

- Input pulse level 0.4V to 2.4V
- Input rise and fall time 10ns
- Input and output timing level 1.5V
- Output load 1 TTL gate and CL=100pF(70ns product CL=30pF)

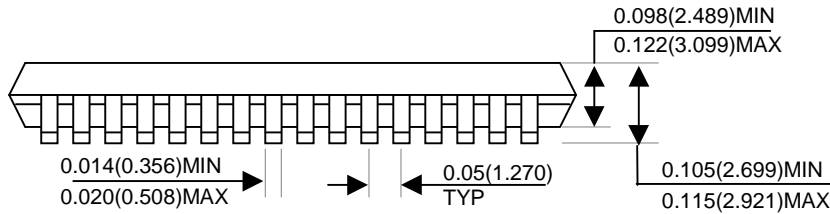
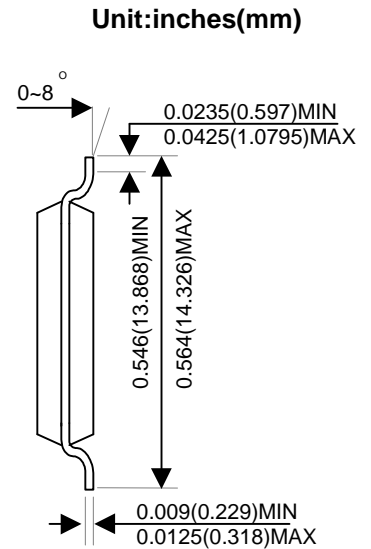
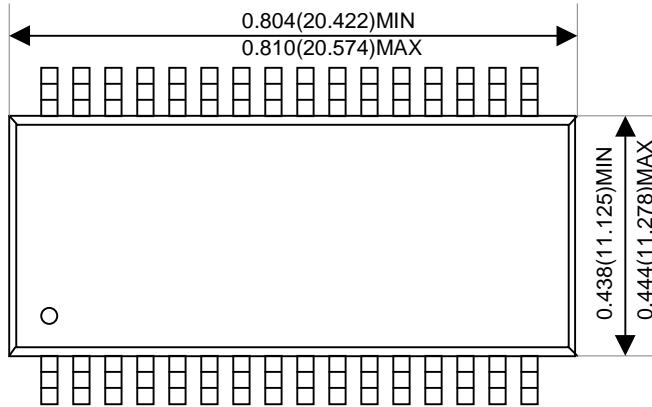
Timing Waveforms

READ MODE



Package Dimension

32SOP



32DIP

