

MNLM113-X REV 1B1

Original Creation Date: 06/30/95

Last Update Date: 04/18/00

Last Major Revision Date: 11/07/96

REFERENCE DIODE
General Description

The LM113 is a temperature compensated, low voltage reference diode. It features extremely-tight regulation over a wide range of operating currents in addition to an unusually-low breakdown voltage and good temperature stability.

The diode is synthesized using transistors and resistors in a monolithic integrated circuit. As such, it has the same low noise and long term stability as modern IC op amps. Further, output voltage of the reference depends only on highly-predictable properties of components in the IC; so they can be manufactured and supplied to tight tolerances.

The characteristics of this reference recommend it for use in bias-regulation circuitry, in low-voltage power supplies or in battery powered equipment. The fact that the breakdown voltage is equal to a physical property of silicon—the energy-band gap voltage—makes it useful for many temperature-compensation and temperature-measurement functions.

Industry Part Number

LM113

Prime Die

LM113

NS Part Numbers

 LM113H-QMLV
 LM113H-SMD
 LM113H/883
 LM113WG-QMLV
 LM113WG-SMD

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

| Subgrp | Description | Temp (°C) |
|--------|---------------------|------------|
| 1 | Static tests at | +25 |
| 2 | Static tests at | +125 |
| 3 | Static tests at | -55 |
| 4 | Dynamic tests at | +25 |
| 5 | Dynamic tests at | +125 |
| 6 | Dynamic tests at | -55 |
| 7 | Functional tests at | +25 |
| 8A | Functional tests at | +125 |
| 8B | Functional tests at | -55 |
| 9 | Switching tests at | +25 |
| 10 | Switching tests at | +125 |
| 11 | Switching tests at | -55 |

Features

- Low breakdown voltage: 1.220V
- Dynamic impedance of 0.3 Ohms from 500uA to 20mA
- Temperature stability typically 1% over -55 C to 125 C range

CONTROLLING DOCUMENTS:

| | |
|--------------|-----------------|
| LM113H-QMLV | 5962-9684301VXA |
| LM113H-SMD | 5962-8671101XA |
| LM113WG-QMLV | 5962-9684301VZA |
| LM113WG-SMD | 5962-8671101ZA |

(Absolute Maximum Ratings)

(Note 1)

| | | |
|---|----------------------|-----------------|
| Power Dissipation (Note 2) | | 100mW |
| Reverse Current | | 50mA |
| Forward Current | | 50mA |
| Storage Temperature Range | | -65 C to +150 C |
| Lead Temperature (Soldering, 10 seconds) | | 300 C |
| Operating Temperature Range | | -55 C to + 125C |
| Maximum Junction Temperature | | +150 C |
| Thermal Resistance | | |
| ThetaJA | | |
| Metal Can | (Still Air) | 440 C/W |
| | (500LF/Min Air Flow) | TBD |
| CERAMIC SOIC | (Still Air) | 218 C/W |
| | (500LF/Min Air Flow) | 140 C/W |
| ThetaJC | | |
| Metal Can | | 80 C/W |
| CERAMIC SOIC | | 27 C/W |
| ESD Tolerance (Note 3) | | 4000V |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{dmax} = (T_{jmax} - TA)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS

| SYMBOL | PARAMETER | CONDITIONS | NOTES | PIN-NAME | MIN | MAX | UNIT | SUB-GROUPS |
|-----------|---------------------------|---------------------|-------|----------|-------|-------|------|------------|
| Vzr | Zener Voltage | Ir = 1 mA | | | 1.16 | 1.28 | V | 1 |
| | | | | | 1.157 | 1.283 | V | 2, 3 |
| Delta Vzr | Delta Zener Voltage | 0.5mA <= Ir <= 20mA | | | | 15 | mV | 1 |
| | | 0.5mA <= Ir <= 10mA | | | | 15 | mV | 2, 3 |
| Vf | Forward Voltage Drop | If = 1mA | | | | 1 | V | 1, 2, 3 |
| Rr | Reverse Dynamic Impedance | Ir = 1mA | 1 | | | 1 | Ohm | 4 |
| | | Ir = 10mA | 1 | | | 0.8 | Ohm | 4 |

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
 DC: Delta calculations performed on JAN S and QMLV devices at Group B, Subgroup 5 "ONLY".

| | | | | | | | | |
|-----|---------------|----------|--|--|-------|------|---|---|
| Vzr | Zener Voltage | Ir = 1mA | | | -0.02 | 0.02 | V | 1 |
|-----|---------------|----------|--|--|-------|------|---|---|

Note 1: Guaranteed parameter not tested.

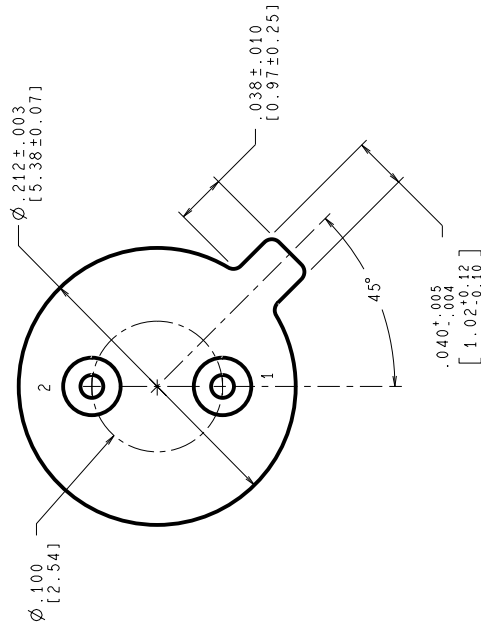
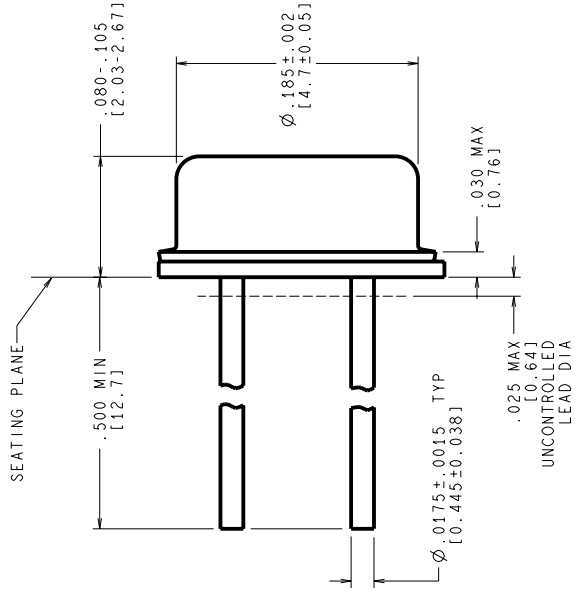
Graphics and Diagrams

| GRAPHICS# | DESCRIPTION |
|-----------|---|
| 06331HRA6 | CERAMIC SOIC (WG), 10 LEAD (B/I CKT) |
| 09385HRA1 | METAL CAN, TO-46,2LD, .100 DIA P.C. (B/I CKT) |
| H02ARE | METAL CAN, TO-46,2LD, .100 DIA P.C. (P/P DWG) |
| P000472A | CERAMIC SOIC (WG), 10 LEAD (PIN OUT) |
| P000475A | METAL CAN, TO-46,2LD, .100 DIA P.C. (PIN OUT) |
| WG10ARC | CERAMIC SOIC (WG), 10 LEAD (P/P DWG) |

See attached graphics following this page.

REVISIONS

| LTR | DESCRIPTION | E.C.N. | DATE | BY/APP'D |
|-----|---|--------|------------|----------|
| D | REVISE & REDRAW PER NEW STANDARD | 10402 | 05/04/1994 | TL/GY |
| E | UPDATE TITLE & MIL/AERO STAMP. CHANGE DWG SIZE FORMAT FROM B TO C. | 12131 | 11/17/1998 | MS/ |



CONTROLLING DIMENSION IS INCH
VALUES IN () ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

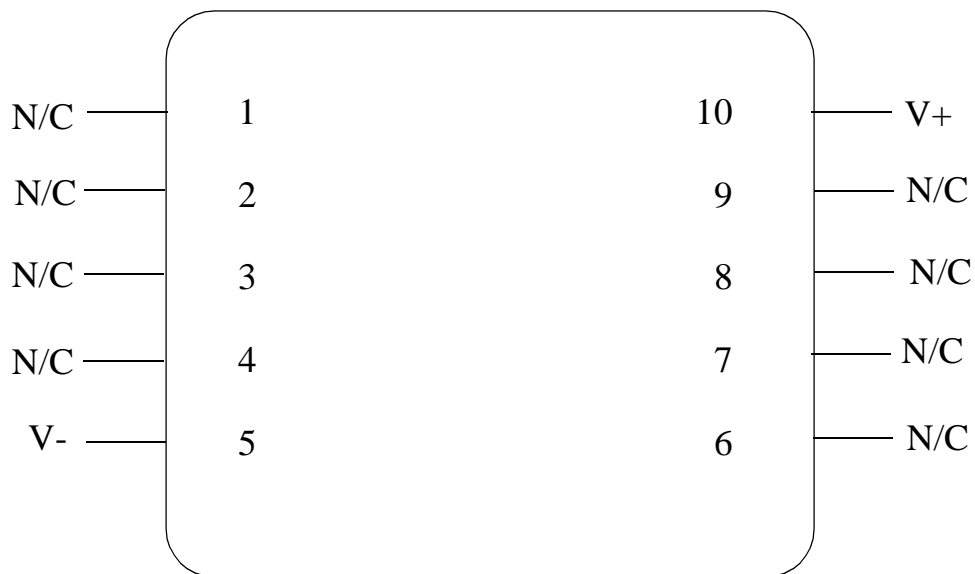
- LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
- STANDARD METAL CAN TYPE: SOLID BASE.
- APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
- REFERENCE JEDEC REGISTRATION TO-46, JEDEC PUBLICATION No. 95.

| APPROVALS | DATE | BY |
|------------------|------------|----|
| DRYAN T. LEQUANG | 05/04/1994 | |
| ENGR. CHK. | | |
| ENGR. CHK. | | |

| | | | | | |
|--|--|-------|------|----------------|-----|
| | | SCALE | SIZE | DRAWING NUMBER | REV |
| | | N/A | C | (SC)MKT-H02A | E |

| | |
|--|--|
| | |
| National Semiconductor | |
| 2800 Semiconductor dr., Santa Clara, CA 95052-8090 | |
| METAL CAN TO-46, 2 LEAD, .100 DIA P.C. | |

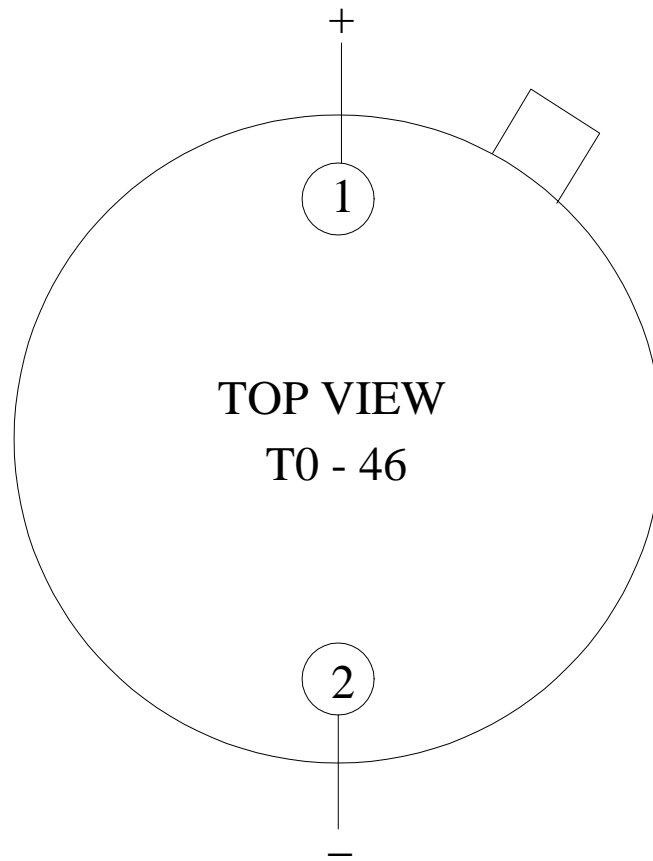
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|----------------------|--|--------------|--|
| DO NOT SCALE DRAWING | | SHEET 1 of 1 | |
|----------------------|--|--------------|--|



LM113WG
10 - LEAD CERPACK SOIC
CONNECTION DIAGRAM
TOP VIEW
P000472A



National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM103H, LM113H, LM129H
2 - LEAD TO-46
CONNECTION DIAGRAM
TOP VIEW
P000475A

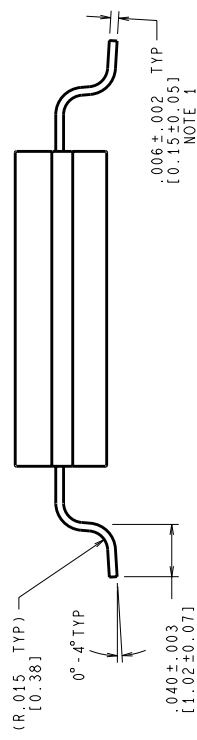
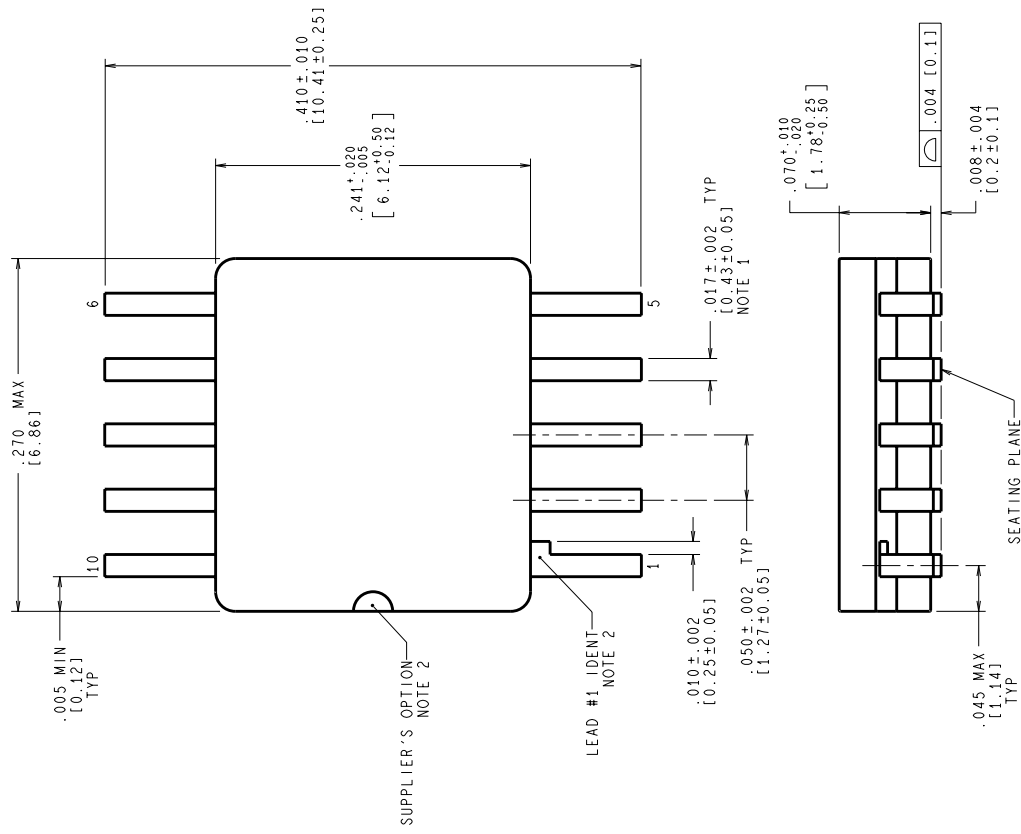


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2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS

| LTR | DESCRIPTION | E.C.N. | DATE | BY/APP'D |
|-----|---|--------|------------|----------|
| A | RELEASE TO DOCUMENT CONTROL | 11374 | 02/29/1996 | MS/KH |
| B | LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002 DIM. .040±.003 WAS .037±.003 | 11441 | 04/19/1996 | MS/KH |
| C | R .015(0.38) WAS R .006(0.15) | 11838 | 10/08/1997 | TL/ |



CONTROLLING DIMENSION IS INCH
VALUES IN | ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

- LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICRONS/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
- LEAD 1 IDENTIFICATION SHALL BE:
 - A NOTCH OR OTHER MARK WITHIN THIS AREA
 - A TAB ON LEAD 1, EITHER SIDE
- NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

| APPROVALS | DATE | SCALE | SIZE | DRAWING NUMBER | REV |
|------------------|----------|-------|------|----------------|-----|
| DRN: MARYA SUCHY | 02/29/96 | N/A | C | (SC)MKT-WG10A | C |
| DATE: 02/29/96 | | | | | |
| CHK: [Signature] | | | | | |
| CHK: [Signature] | | | | | |
| PROJECTION | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

National Semiconductor
 2800 Semiconductor Dr., Santa Clara, CA 95052-8090
**CERPACK,
 10 LEAD,
 GULL WING**

DO NOT SCALE DRAWING SHEET 1 of 1

Revision History

| Rev | ECN # | Rel Date | Originator | Changes |
|-----|----------|----------|-------------|---|
| 1B1 | M0003665 | 04/18/00 | Rose Malone | Update MDS: MNLM113-X, Rev. 1A0 to MNLM113-X, Rev. 1B1. Added reference to WG pkg and graphics to graphics section. Updated Absolute Section. |