

**MICRON**  
SEMICONDUCTOR INC.
**MT5C6408**  
**8K x 8 SRAM**

# SRAM

# 8K x 8 SRAM

**5 VOLT SRAM**

## FEATURES

- High speed: 9, 10, 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +5V  $\pm 10\%$  power supply
- Easy memory expansion with  $\overline{CE1}$ , CE2 and  $\overline{OE}$  options
- All inputs and outputs are TTL-compatible

## OPTIONS

- Timing
  - 9ns access
  - 10ns access
  - 12ns access
  - 15ns access
  - 20ns access
  - 25ns access
- Packages
  - Plastic DIP (300 mil)
  - Plastic SOJ (300 mil)
- 2V data retention

## MARKING

- |                              |      |
|------------------------------|------|
| • Timing                     |      |
| 9ns access                   | - 9  |
| 10ns access                  | -10  |
| 12ns access                  | -12  |
| 15ns access                  | -15  |
| 20ns access                  | -20  |
| 25ns access                  | -25  |
| • Packages                   |      |
| Plastic DIP (300 mil)        | None |
| Plastic SOJ (300 mil)        | DJ   |
| • 2V data retention          | L    |
| • Temperature                |      |
| Commercial (0°C to +70°C)    | None |
| Industrial (-40°C to +85°C)  | IT   |
| Automotive (-40°C to +125°C) | AT   |
| Extended (-55°C to +125°C)   | XT   |

- Part Number Example: MT5C6408DJ-15 AT

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

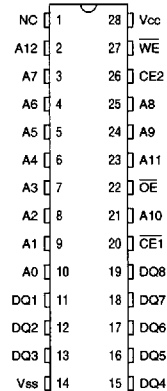
## GENERAL DESCRIPTION

The MT5C6408 is organized as a 8,192 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

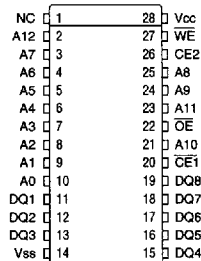
For flexibility in high-speed memory applications, Micron offers two chip enables and an output enable on the x8 organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

## PIN ASSIGNMENT (Top View)

### 28-Pin DIP (SA-4)



### 28-Pin SOJ (SD-2)

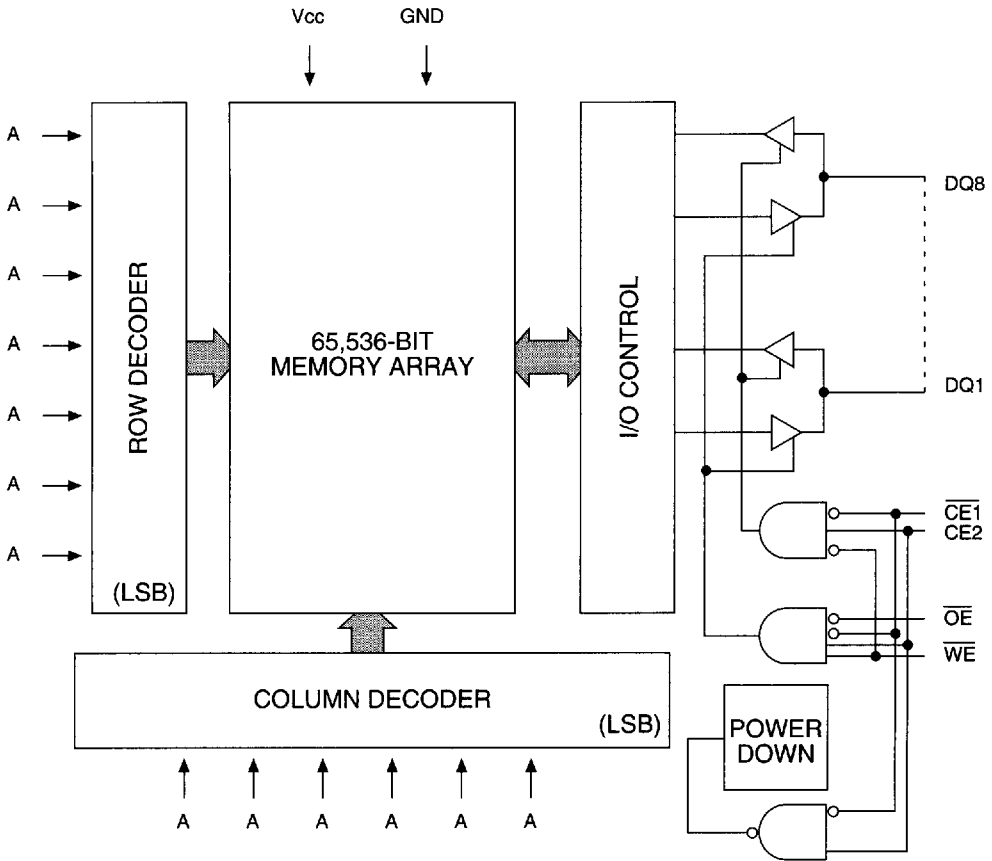


Writing to these devices is accomplished when write enable ( $\overline{WE}$ ) and  $\overline{CE1}$  inputs are LOW and CE2 is HIGH. Reading is accomplished when  $\overline{WE}$  and CE2 remain HIGH and  $\overline{CE}$  and  $\overline{OE}$  go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

**FUNCTIONAL BLOCK DIAGRAM**

**5 VOLT SRAM**



**TRUTH TABLE**

MODE	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	DQ	POWER
STANDBY	H	X	X	X	HIGH-Z	STANDBY
STANDBY	X	L	X	X	HIGH-Z	STANDBY
READ	L	H	H	L	Q	ACTIVE
NOT SELECTED	L	H	H	H	HIGH-Z	ACTIVE
WRITE	L	H	L	X	D	ACTIVE


**MT5C6408**  
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**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc supply relative to Vss ..... -1V to +7V  
 Storage Temperature (plastic) ..... -55°C to +150°C  
 Power Dissipation ..... 1W  
 Short Circuit Output Current ..... 50mA  
 Voltage on Any Pin Relative to Vss ..... -1V to Vcc +1V

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**5 VOLT SRAM**
**ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**
 $(0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}; V_{CC} = 5\text{V} \pm 10\%)$ 

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		$V_{IH}$	2.2	$V_{CC} + 1$	V	1
Input Low (Logic 0) Voltage		$V_{IL}$	-0.5	0.8	V	1, 2
Input Leakage Current	$0\text{V} \leq V_{IN} \leq V_{CC}$	$I_{LI}$	-5	5	$\mu\text{A}$	
Output Leakage Current	Output(s) disabled $0\text{V} \leq V_{OUT} \leq V_{CC}$	$I_{LO}$	-5	5	$\mu\text{A}$	
Output High Voltage	$I_{OH} = -4.0\text{mA}$	$V_{OH}$	2.4		V	1
Output Low Voltage	$I_{OL} = 8.0\text{mA}$	$V_{OL}$		0.4	V	1
Supply Voltage		$V_{CC}$	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX						UNITS	NOTES
				-9	-10	-12	-15	-20	-25		
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}; V_{CC} = \text{MAX}$ $f = \text{MAX} = 1/\text{tRC}$ outputs open	$I_{CC}$	125	190	185	175	165	140	130	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \geq V_{IH}; V_{CC} = \text{MAX}$ $f = \text{MAX} = 1/\text{tRC}$ outputs open	$I_{SB1}$	22	60	50	45	40	35	35	mA	14
	$\overline{CE} \geq V_{CC} - 0.2\text{V}; V_{CC} = \text{MAX}$ $V_{IN} \leq V_{SS} + 0.2\text{V}$ or $V_{IN} \geq V_{CC} - 0.2\text{V}; f = 0$	$I_{SB2}$	0.5	3	3	3	3	3	5	mA	14

**CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	$T_A = 25^{\circ}\text{C}; f = 1\text{MHz}$ $V_{CC} = 5\text{V}$	$C_I$	5	pF	4
Output Capacitance		$C_O$	7	pF	4


**MT5C6408**  
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**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

 (Note 5) ( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{CC} = 5V \pm 10\%$ )

**5 VOLT SRAM**

DESCRIPTION	SYM	-9		-10		-12		-15		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
<b>READ Cycle</b>															
READ cycle time	<sup>t</sup> RC	9		10		12		15		20		25		ns	
Address access time	<sup>t</sup> AA		9		10		12		15		20		25	ns	
Chip Enable access time	<sup>t</sup> ACE		9		9		10		12		15		20	ns	
Output hold from address change	<sup>t</sup> OH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	<sup>t</sup> LZCE	2		2		2		2		2		2		ns	7, 15
Chip disable to output in High-Z	<sup>t</sup> HZCE		5		5		6		7		8		8	ns	6, 7
Chip Enable to power-up time	<sup>t</sup> PU	0		0		0		0		0		0		ns	
Chip disable to power-down time	<sup>t</sup> PD		9		10		12		15		20		25	ns	
Output Enable access time	<sup>t</sup> AOE		4.5		5		6		7		8		8	ns	
Output Enable to output in Low-Z	<sup>t</sup> LZOE	0		0		0		0		0		0		ns	
Output disable to output in High-Z	<sup>t</sup> HZOE		4.5		5		5		6		7		8	ns	6
<b>WRITE Cycle</b>															
WRITE cycle time	<sup>t</sup> WC	9		10		12		15		20		25		ns	
Chip Enable to end of write	<sup>t</sup> CW	7		8		10		12		15		20		ns	
Address valid to end of write	<sup>t</sup> AW	7		8		10		12		15		20		ns	
Address setup time	<sup>t</sup> AS	0		0		0		0		0		0		ns	
Address hold from end of write	<sup>t</sup> AH	0		0		0		0		0		0		ns	
WRITE pulse width	<sup>t</sup> WP1	6		7		8		10		12		15		ns	
WRITE pulse width	<sup>t</sup> WP2	8		9		10		14		18		20		ns	
Data setup time	<sup>t</sup> DS	5		6		7		8		9		10		ns	
Data hold time	<sup>t</sup> DH	1		1		1		1		1		1		ns	
Write disable to output in Low-Z	<sup>t</sup> LZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	<sup>t</sup> HZWE		4		5		5		6		8		8	ns	6, 7



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**INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)**

The following specifications are to be used for Industrial Temperature (IT) MT5C6408 SRAMs.  
(-40°C ≤ T<sub>A</sub> ≤ 85°C)

DESCRIPTION	CONDITIONS	SYMBOL	MAX					UNITS	NOTES
			-10	-12	-15	-20	-25		
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}$ ; V <sub>CC</sub> = MAX f = MAX = 1/ t <sub>RC</sub> outputs open	I <sub>CC</sub>	195	185	175	150	140	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \geq V_{IH}$ ; V <sub>CC</sub> = MAX f = MAX = 1/ t <sub>RC</sub> outputs open	I <sub>SB1</sub>	60	50	45	40	40	mA	13
	$\overline{CE} \geq V_{CC} - 0.2V$ ; V <sub>CC</sub> = MAX V <sub>IN</sub> ≤ V <sub>SS</sub> + 0.2V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V; f = 0	I <sub>SB2</sub>	5	5	5	5	5	mA	13

**5 VOLT SRAM**

**DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)**

DESCRIPTION	CONDITIONS		SYMBOL	TYP	MAX	UNITS	NOTES
Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ V <sub>IN</sub> ≥ (V <sub>CC</sub> - 0.2V) or ≤ 0.2V	V <sub>CC</sub> = 2V	I <sub>CCDR</sub>	130	300	μA	14
		V <sub>CC</sub> = 3V	I <sub>CCDR</sub>	210	550	μA	14

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

Refer to commercial temperature timing parameters for specifications not listed here.  
(Notes 5, 14) (-40°C ≤ T<sub>A</sub> ≤ 85°C)

DESCRIPTION	SYM	-12		-15		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
<b>READ Cycle</b>											
Output hold from address change	t <sub>OH</sub>	2		2		2		2		ns	
Chip Enable to output in Low-Z	t <sub>LZCE</sub>	1		1		1		1		ns	7
<b>WRITE Cycle</b>											
Write disable to output in Low-Z	t <sub>LZWE</sub>	1		1		1		1		ns	7


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**5 VOLT SRAM**
**AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)**

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C6408 SRAMs. (-40°C ≤ T<sub>A</sub> ≤ 125°C - AT) (-55°C ≤ T<sub>A</sub> ≤ 125°C - XT)

DESCRIPTION	CONDITIONS	SYMBOL	MAX				UNITS	NOTES
			-12	-15	-20	-25		
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}$ ; V <sub>CC</sub> = MAX f = MAX = 1/1RC outputs open	I <sub>CC</sub>	185	175	150	140	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \geq V_{IH}$ ; V <sub>CC</sub> = MAX f = MAX = 1/1RC outputs open	I <sub>SB1</sub>	50	45	40	40	mA	13
	$\overline{CE} \geq V_{CC} - 0.2V$ ; V <sub>CC</sub> = MAX V <sub>IN</sub> ≤ V <sub>SS</sub> + 0.2V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V; f = 0	I <sub>SB2</sub>	5	5	5	5	mA	13

**DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)**

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES	
Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ V <sub>IN</sub> ≥ (V <sub>CC</sub> - 0.2V) or ≤ 0.2V	V <sub>CC</sub> = 2V	I <sub>CCDR</sub>	130	300	μA	14
		V <sub>CC</sub> = 3V	I <sub>CCDR</sub>	210	550	μA	14

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

Refer to commercial temperature timing parameters for specifications not listed here.

(Notes 5, 14) (-40°C ≤ T<sub>A</sub> ≤ 125°C; -55°C ≤ T<sub>A</sub> ≤ 125°C; V<sub>CC</sub> = 5V ± 10%)

DESCRIPTION	SYM	-12		-15		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
<b>READ Cycle</b>											
Output hold from address change	t <sub>OH</sub>	2		2		2		2		ns	
Chip Enable to output in Low-Z	t <sub>LZCE</sub>	1		1		1		1		ns	7
<b>WRITE Cycle</b>											
Write disable to output in Low-Z	t <sub>LZWE</sub>	1		1		1		1		ns	7



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**AC TEST CONDITIONS**

Input pulse levels .....	Vss to 3.0V
Input rise and fall times .....	3ns
Input timing reference levels .....	1.5V
Output reference levels .....	1.5V
Output load .....	See Figures 1 and 2

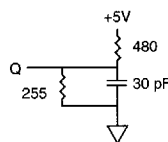


Fig. 1 OUTPUT LOAD EQUIVALENT

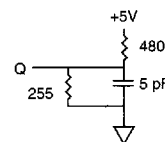


Fig. 2 OUTPUT LOAD EQUIVALENT

**5 VOLT SRAM**

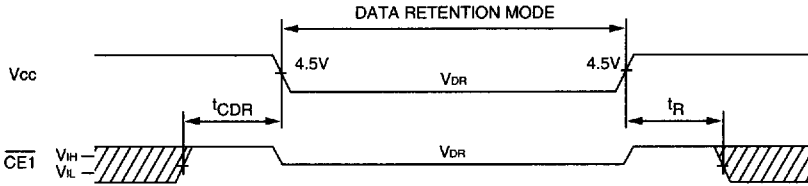
**NOTES**

1. All voltages referenced to Vss (GND).
2. -3V for pulse width <sup>t</sup>RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. <sup>t</sup>HZCE, <sup>t</sup>HZWE and <sup>t</sup>HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE and <sup>t</sup>HZWE is less than <sup>t</sup>LZWE.
8. <sup>WE</sup> is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. <sup>t</sup>RC = Read Cycle Time.
12. CE2 timing is the same as <sup>CE1</sup> timing. The wave is inverted.
13. Chip enable and write enable can initiate and terminate a WRITE cycle.
14. Typical values are measured at 5V, 25°C and 15ns cycle time.
15. Typical currents are measured at 25°C.
16. Output enable (<sup>OE</sup>) is inactive (HIGH).
17. Output enable (<sup>OE</sup>) is active (LOW).

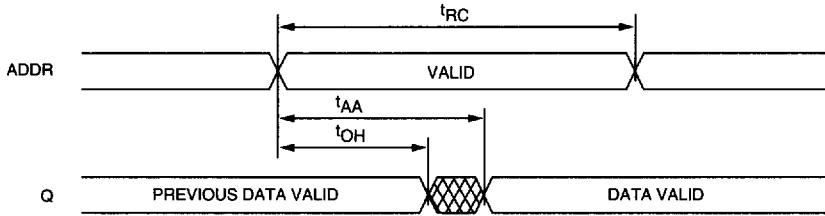
**DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)**

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V <sub>DR</sub>	2			V	
Data Retention Current	<sup>CE</sup> ≥ (Vcc - 0.2V) <sup>VIN</sup> ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc = 2V	I <sub>CCDR</sub>		130	300	μA	15
		Vcc = 3V	I <sub>CCDR</sub>		210	400	μA	15
Chip Deselect to Data Retention Time			<sup>t</sup> CDR	0			ns	4
Operation Recovery Time			<sup>t</sup> R	<sup>t</sup> RC			ns	4, 11

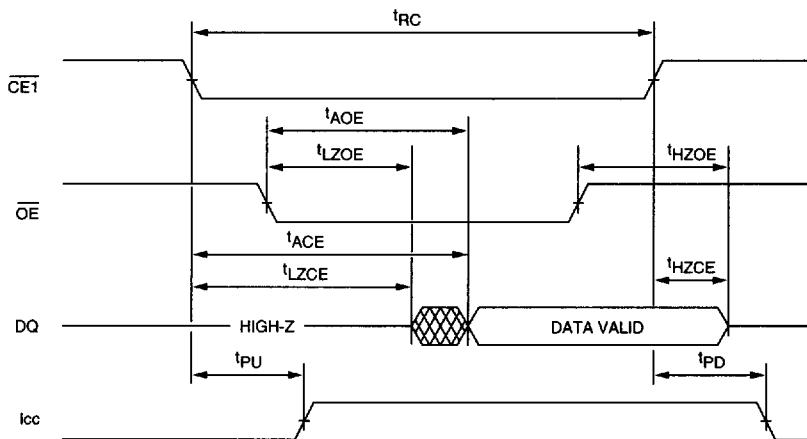
**LOW V<sub>CC</sub> DATA RETENTION WAVEFORM <sup>12</sup>**



**READ CYCLE NO. 1 <sup>8, 9</sup>**



**READ CYCLE NO. 2 <sup>7, 8, 10, 12</sup>**

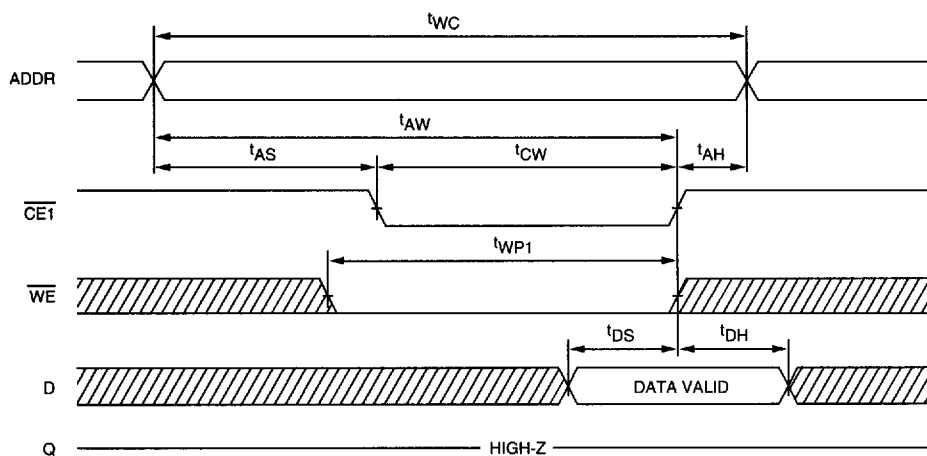


DON'T CARE  
 UNDEFINED

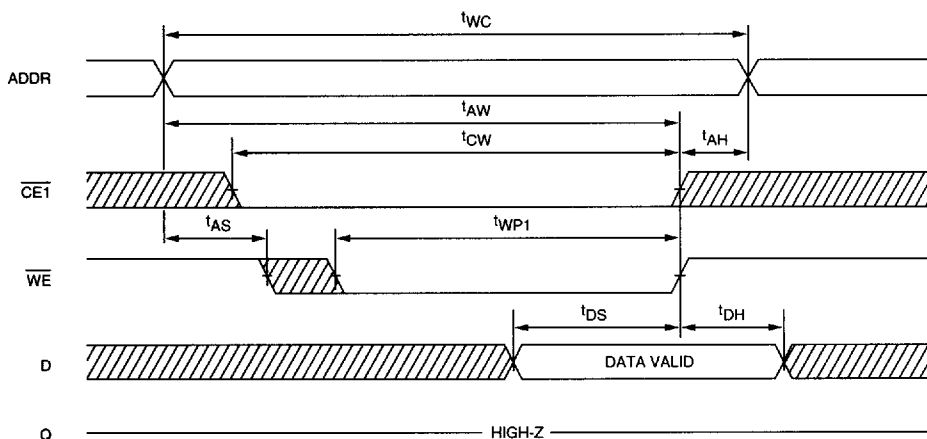
**5 VOLT SRAM**





**WRITE CYCLE NO. 1** <sup>12</sup>  
 (Chip Enable Controlled)



**WRITE CYCLE NO. 2** <sup>12, 13, 16</sup>  
 (Write Enable Controlled)



 DON'T CARE  
 UNDEFINED

**5 VOLT SRAM**

**WRITE CYCLE NO. 3** 7, 12, 13, 17  
(Write Enable Controlled)

