W83194BR-K8/W83194BG-K8
Winbond Clock Generator for AMD® K8™ Microprocessors and Chipsets

Date: 05/02/2006 Revision: 0.61

W83194BR-K8 Datasheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1	n.a.	06/08/2004	0.5	n.a.	All of the versions before 0.50 are for internal use.
2	1-16,19	03/31/2005	0.6	n.a.	Please see red text.
3		05/02/2006	0.61		Add Lead free part
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CLOCK GEN. FOR AMD® K8™ MICROPROCESSORS AND CHIPSET

1. GENERAL DESCRIPTION

The W83194BR-K8 is a Clock Synthesizer for AMD ATHLON 64™ and OPTERON™ Processors and support chipsets. W83194BR-K8 provides all clocks required for the high-speed microprocessors and provides step-less frequency programming and 32 different frequencies of CPU, HTTCLK and PCI clock settings. All clocks are externally selectable with smooth transitions.

The W83194BR-K8 provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and provides 1% & 0.5% center type and down type spread spectrum or programmable S.S.T. scale to reduce EMI.

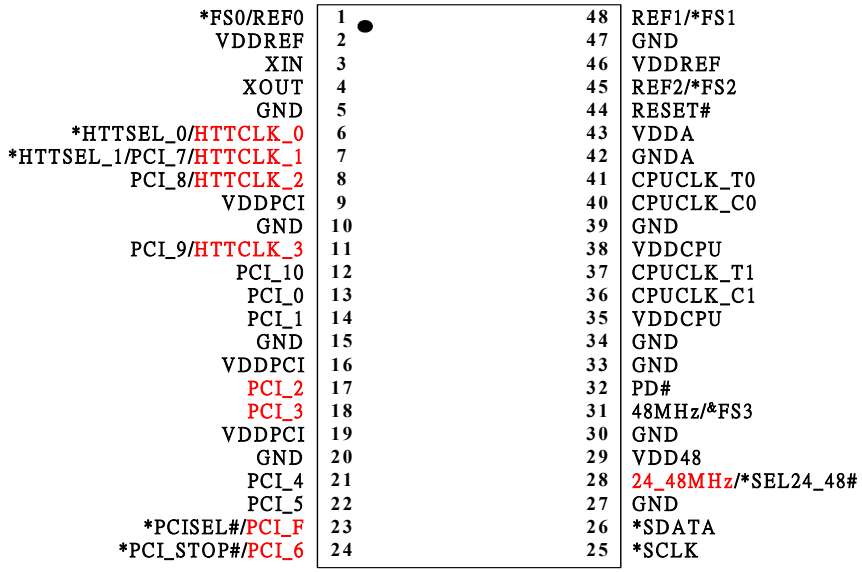
The W83194BR-K8 also has watchdog timer and reset output pin to support auto-reset when systems stop functioning caused by improper frequency setting.

The W83194BR-K8 accepts a 14.318 MHz reference crystal as its input and runs on 3.3V supply.

2. PRODUCT FEATURES

- 2 pairs push-pull differential clock for CPU and Chipset
- 3 selectable PCI/HTTCLK clock outputs
- 1 HTTCLK clock output
- 9 PCI synchronous clocks, 1 free running
- 1 48MHz clock outputs
- 1 24_48MHz for I/O chip, default 24MHz
- 3 REF 14.318MHz clock outputs
- I^2C 2-wire serial interface supports block and byte mode read/write
- Step-less frequency programming
- Smooth frequency switch with selections from 100 to 309MHz
- Programmable clock outputs slew rate control and skew control
- Support 1% & 0.5% center type and down type spread spectrum in table mode
- Programmable S.S.T. scale to reduce EMI in M/N mode
- Programmable registers to enable/disable each output and select modes
- Watch dog timer and RESET# output pins
- 48-pin SSOP package

3. PIN CONFIGURATION

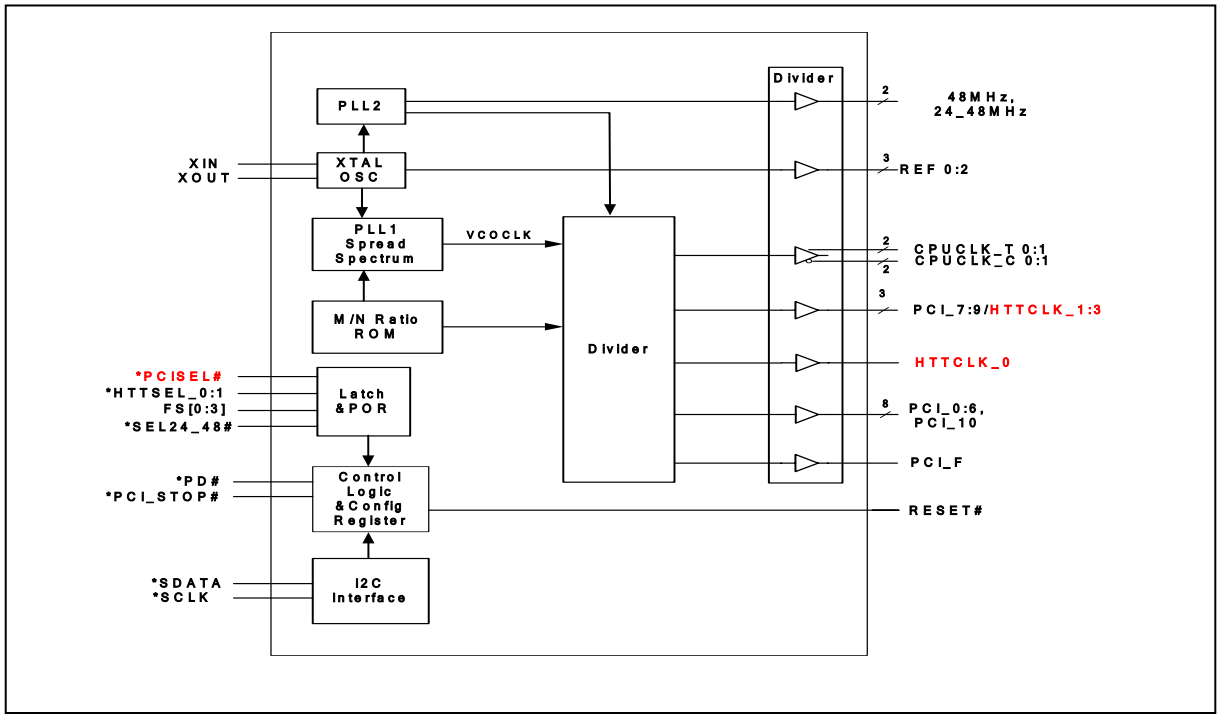


#: Active low

*: Internal pull up resistor 120KΩ to VDD

&: Internal Pull-down resistor 120KΩ to GND

4. BLOCK DIAGRAM



5. PIN DESCRIPTION

BUFFER TYPE SYMBOL	DESCRIPTION
IN	Input
IN_{td120k}	Latch input pin and internal 120KΩ pull down
IN_{tp120k}	Latch input pin and internal 120KΩ pull up
OUT	Output
I/O	Bi-directional Pin
I/OD	Bi-directional Pin, Open Drain
OD	Open Drain
#	Active Low
*	Internal 120kΩ pull-up
&	Internal 120kΩ pull-down

5.1 Crystal I/O

PIN	PIN NAME	TYPE	DESCRIPTION
3	XIN	IN	Crystal input with internal loading capacitors and feedback resistors.
4	XOUT	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors.

5.2 CPU, PCI/HT66, PCI Clock Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
41,37,40,36	CPUCLK_T 0:1 CPUCLK_C 0:1	OUT	3.3V push-pull differential clock outputs for CPU and Chipset.
6	HTTCLK_0	OUT	3.3V HTTCLK output clock
	*HTTSEL_0	IN_{tp120k}	Latched input at initial power up for PCI/HTTCLK selecting the output frequency clocks. This pin has internal 120KΩ pull up.
7	PCI_7/HTTCLK_1	OUT	3.3V PCI 33MHz or HTTCLK (default) output clock select by HTTSEL [0:1]
	*HTTSEL_1	IN_{tp120k}	Latched input at initial power up for PCI/HTTCLK selecting the output frequency clocks. This pin has internal 120KΩ pull up.
8,11	PCI_8:9/HTTCLK_2:3	OUT	3.3V PCI 33MHz(default) or HTTCLK output clocks select by HTTSEL [0:1]
13, 14, 17, 18, 21, 22,12	PCI_0:5 PCI_10	OUT	3.3V PCI clock outputs,

CPU, PCI/HT66, PCI Clock Outputs, continued.

PIN	PIN NAME	TYPE	DESCRIPTION
23	PCI_F	OUT	3.3V Free-Run PCI clock output, not affected by PCI_STOP#.
	*PCISEL#	IN_{tp120k}	Latched input at initial power up for pin 24 PCI_STOP/PCI_6 selecting the output, This pin has internal 120KΩ pull up, when PCISEL# = 0 pin24 is PCI_6, = 1 pin 24 is PCI_STOP#(default)
24	PCI_6	OUT	3.3V PCI clock outputs,
	*PCI_STOP#	IN_{tp120k}	Input pins; when low, stop all PCI clock except PCI_F (pin 23); This pin has internal 120KΩ pull up (default).

5.3 Fixed Frequency Outputs and Function Control pin

PIN	PIN NAME	TYPE	DESCRIPTION
1	REF0	OUT	14.318MHz output.
	*FS0	IN_{tp120k}	Latched input for FS0 at initial power up selecting the output frequency clocks. This pin has internal 120KΩ pull up.
48	REF1	OUT	14.318MHz output.
	*FS1	IN_{tp120k}	Latched input for FS1 at initial power up selecting the output frequency clocks. This pin has internal 120KΩ pull up.
45	REF2	OUT	14.318MHz clock output.
	*FS2	IN_{tp120k}	Latched input for FS2 at initial power up selecting the output frequency clocks. This pin has internal 120KΩ pull up.
28	24_48MHz	OUT	24 or 48MHz clock output,
	*SEL24_48#	IN_{tp120k}	Latched input for 24_48MHz at initial power up selecting the output frequency clocks. This pin has internal 120KΩ pull up, 1 = 24 MHz (default), 0= 48MHz.
31	48MHz	OUT	48MHz clock output.
	&FS3	IN_{td120k}	Latched input for FS3 at initial power up selecting the output frequency clocks. This pin has internal 120KΩ pull down.
32	*PD#	IN_{tp120k}	Low active input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal oscillator are stopped. This pin has internal 120KΩ pull up.
44	RESET#	OD	250mS low level system reset signal when Watchdog Timer times out. Application circuit must add external pull high.

5.4 I²C Control Interface

PIN	PIN NAME	TYPE	DESCRIPTION
26	*SDATA	I/OD	Serial data of I²C 2-wire control interface with internal pull-up resistor
25	*SCLK	IN	Serial clock of I²C 2-wire control interface with internal pull-up resistor

5.5 Power and GND Pins

PIN	PIN NAME	DESCRIPTION
2,46	VDDREF	3.3V power supply for REF.
9,16,19	VDDPCI	3.3V power supply for PCI.
29	VDD48	3.3V power supply for 48MHz.
35,38	VDDCPU	3.3V power supply for CPU.
43	VDDA	3.3V power supply analog core.
42	GNDA	Ground pin for analog core.
5,10,15,20,27,30,33,34,39,47	GND	Ground pin for 3.3V.

5.6 HTTSEL table

HTTSEL_0	HTTSEL_1	PCI_7/HTTLK_1(PIN7)	PCI_8/HTTCLK_2(PIN8)	PC_9I/HTTCLK_3(PIN11)
0	0	HTTCLK_1	HTTCLK_2	PCI_9
0	1	HTTCLK_1	HTTCLK_2	HTTCLK_3
1	0	PCI_7	PCI_8	PCI_9
1	1	HTTCLK_1	PCI_8	PCI_9

6. FREQUENCY SELECTION BY HARDWARE OR SOFTWARE

This frequency table uses the power-on latched FS [3:0] value or register bits SSEL [4:0] (Register 0 bit 7 ~ 3). When FS [3:0] pins are no-connecting in the application circuit, CPU, HTTCLK and PCI clock frequency will have the values shown in grey color.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	CPU (MHZ)	HTTCLK (MHZ)	PCI (MHZ)
FS4	FS3	FS2	FS1	FS0			
0	0	0	0	0	100.9	67.27	33.63
0	0	0	0	1	133.9	66.95	33.47
0	0	0	1	0	168.0	67.2	33.6
0	0	0	1	1	202.0	67.33	33.66
0	0	1	0	0	100.2	66.8	33.4
0	0	1	0	1	133.5	66.75	33.34
0	0	1	1	0	166.7	66.68	33.34
0	0	1	1	1	200.4	66.8	33.4
0	1	0	0	0	150.0	60.0	30.0
0	1	0	0	1	180.0	60.0	30.0
0	1	0	1	0	210.0	70.0	35.0
0	1	0	1	1	240.0	60.0	30.0
0	1	1	0	0	270.0	67.50	33.75
0	1	1	0	1	233.3	66.67	33.33
0	1	1	1	0	266.6	66.67	33.33
0	1	1	1	1	300.0	75.0	37.5
1	0	0	0	0	100.0	66.67	33.33
1	0	0	0	1	133.3	66.67	33.33
1	0	0	1	0	166.6	66.67	33.33
1	0	0	1	1	200.0	66.67	33.33
1	0	1	0	0	103.0	68.67	34.33
1	0	1	0	1	137.3	68.66	34.33
1	0	1	1	0	171.6	68.66	34.33
1	0	1	1	1	206.0	68.67	34.33
1	1	0	0	0	154.5	61.8	30.9

Frequency Selection BY hardware or Software, continued.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	CPU (MHZ)	HTTCLK (MHZ)	PCI (MHZ)
FS4	FS3	FS2	FS1	FS0			
1	1	0	0	1	185.4	61.8	30.9
1	1	0	1	0	216.3	72.1	36.0
1	1	0	1	1	247.2	61.8	30.9
1	1	1	0	0	278.1	69.53	34.76
1	1	1	0	1	240.3	68.67	34.33
1	1	1	1	0	274.6	68.67	34.33
1	1	1	1	1	309.0	77.25	38.62

7. I²C CONTROL AND STATUS REGISTERS

PWD: Power on default bit value.

7.1 Register 0: Frequency Select (Default = 38h)

BIT	NAME	PWD	DESCRIPTION
7	SSEL 4	0	Software frequency table selection through I²C
6	SSEL 3	0	
5	SSEL 2	1	
4	SSEL 1	1	
3	SSEL 0	1	
2	EN_SSEL		Enable software table selection FS [4:0]. 0 = Hardware table setting. 1 = Software table setting through Bit 7~3.
1	EN_SPSP	0	Enable spread spectrum mode at clock outputs 0 = Spread Spectrum mode disable 1 = Spread Spectrum mode enable
0	EN_SAFE_FREQ	0	After watchdog timeout 0 = Reload the hardware FS [3:0] latched pins setting. 1 = Reload the frequency table selection as defined in Reg-5 Bit 4~0.

7.2 Register 1: CPU & PCI_F Control (1 = Enable, 0 = Disable) & FS0~FS3 latch (Default = E7h)

BIT	NAME	PWD	DESCRIPTION
7	PCI_FEN	1	Pin 23 PCI_F output control
6	CPUCLKEN1	1	Pin 37,36 CPUCLK_T1/C1 output control
5	CPUCLKEN0	1	Pin 41,40 CPUCLK_T0/C0 output control
4	FS4	0	Fix in low level. (Read only)
3	&FS3	X	Power on latched value of FS3 pin 31. (Read only)
2	*FS2	X	Power on latched value of FS2 pin 45. (Read only)
1	*FS1	X	Power on latched value of FS1 pin 48. (Read only)
0	*FS0	X	Power on latched value of FS0 pin 1. (Read only)

7.3 Register 2: PCI Control (1 = Enable, 0 = Disable) (Default = FFh)

BIT	NAME	PWD	DESCRIPTION
7	PCI_6EN	1	Pin 24 PCI_6 output control
6	PCI_10EN	1	Pin 12 PCI_10 output control
5	PCI_5EN	1	Pin 22 PCI_5 output control
4	PCI_4EN	1	Pin 21 PCI_4 output control
3	PCI_3EN	1	Pin 18 PCI_3 output control
2	PCI_2EN	1	Pin 17 PCI_2 output control
1	PCI_1EN	1	Pin 14 PCI_1 output control
0	PCI_0EN	1	Pin 13 PCI_0 output control

7.4 Register 3: HTTCLK, REF (1 = Enable, 0 = Disable) (Default = FFh)

BIT	NAME	PWD	DESCRIPTION
7	-	1	Reserved for Winbond internal use, don't modify it
6	REF2EN	1	Pin 45 REF2 output control
5	REF1EN	1	Pin 48 REF1 output control
4	REF0EN	1	Pin 1 REF0 output control
3	HTTCLK_0EN	1	Pin 6 HTTCLK_0 output control
2	HTTCLK_3EN	1	Pin 11 PCI_9/HTTCLK_3 output control
1	HTTCLK_2EN	1	Pin 8 PCI_8/HTTCLK_2 output control
0	HTTCLK_1EN	1	Pin 7 PCI_7/HTTCLK_1 output control

7.5 Register 4: 24_48MHz Control (1 = Enable, 0 = Disable) (Default = F8h)

BIT	NAME	PWD	DESCRIPTION
7	SEL_24	X	Pin 28 SEL24 _48 MHz output selection, 1: 24 MHz (default), 0: 48 MHz, Default values depend on latched value of SEL24_48# pin duration power on reset.
6	24_48MEN	1	Pin 28 24_48MHz output control
5	48EN	1	Pin 31 48MHz output control
4	HTTSEL_0*	X	Pin 6 Power on latched value of HTTSEL_0* pin.
3	HTTSEL_1*	X	Pin 7 Power on latched value of HTTSEL_1* pin.
2	PCISEL#*	X	Pin 23 Power on latched value of PCISEL#* pin.
1	-	0	Reserved for Winbond internal use, don't modify it
0	-	0	Reserved for Winbond internal use, don't modify it

7.6 Register 5: Watchdog Control (Default = 00h)

BIT	NAME	PWD	DESCRIPTION
7	-	0	Reserved for Winbond internal use, user must not modify it
6	EN_WD	0	1: Enable Watchdog Timer. 0: Disable Watchdog Timer. During timer count down reading this bit returns 1. If count to zero, reading this bit returns 0.
5	WD_TIMEOUT	0	Read only. Timeout Flag. 1: Watchdog has ever started and counts to zero. 0: Watchdog is restarted and counting.
4	SAF_FREQ 4	0	When Watchdog Timer times out and EN_SAFE_FREQ=1, these bits will be reloaded to Reg-0 bit 7~3 to select the clock frequencies.
3	SAF_FREQ 3	0	
2	SAF_FREQ 2	0	
1	SAF_FREQ 1	0	
0	SAF_FREQ 0	0	

7.7 Register 6: Watchdog Timer (Default = 08h)

BIT	NAME	PWD	DESCRIPTION
7	WD_TIME [7]	0	Watchdog Timer timeout duration. The bit resolution is 250mS. The default time is 8*250mS = 2.0 seconds. If Watchdog Timer is started, this register will down count. Reading this register will return the down count value.
6	WD_TIME [6]	0	
5	WD_TIME [5]	0	
4	WD_TIME [4]	0	
3	WD_TIME [3]	1	
2	WD_TIME [2]	0	
1	WD_TIME [1]	0	
0	WD_TIME [0]	0	

7.8 Register 7: M/N Program (Default = 8Bh)

BIT	NAME	PWD	DESCRIPTION
7	N_DIV<8>	X	Programmable N divisor value. Bit 7~0 are defined in the Register 8.
6	M<6>	X	Programmable M divisor value.
5	M>5>	X	
4	M<4>	X	
3	M<3>	X	
2	M<2>	X	
1	M<1>	X	
0	M<0>	X	

7.9 Register 8: M/N Program (Default = 30h)

BIT	NAME	PWD	DESCRIPTION
7	N_DIV [7]	X	Programmable N divisor value bit 7 ~0. The bit 8 is defined in Register 7, bit 9~11 is defined in register 10 bit 3~5.
6	N_DIV [6]	X	
5	N_DIV [5]	X	
4	N_DIV [4]	X	
3	N_DIV [3]	X	
2	N_DIV [2]	X	
1	N_DIV [1]	X	
0	N_DIV [0]	X	

Note: About N value bit 9 ~ 11 descriptions only for Winbond internal and BOIS program use; the release version please reserved this description.

7.10 Register 9: Spread Spectrum Programming (Default = 1Fh)

BIT	NAME	PWD	DESCRIPTION
7	SP_UP [3]	0	Spread Spectrum Up Counter bit 3.
6	SP_UP [2]	0	Spread Spectrum Up Counter bit 2.
5	SP_UP [1]	0	Spread Spectrum Up Counter bit 1.
4	SP_UP [0]	1	Spread Spectrum Up Counter bit 0
3	SP_DOWN [3]	1	Spread Spectrum Down Counter bit 3
2	SP_DOWN [2]	1	Spread Spectrum Down Counter bit 2
1	SP_DOWN [1]	1	Spread Spectrum Down Counter bit 1
0	SP_DOWN [0]	1	Spread Spectrum Down Counter bit 0

7.11 Register 10: Divisor and Step-less Enable Control (Default = 01h)

BIT	NAME	PWD	DESCRIPTION
7	EN_MN_PROG	0	0: using frequency table 1: using M/N register to synthesize clock frequency The equation is **VCO freq. = 14.318MHz * (N+4)/ M**. Once the watchdog timer times out, this bit will be cleared. Then the frequency will be decided by hardware strapping FS<3:0> or frequency select bits SAF_FREQ [4:0] when EN_SAFE_FREQ (Reg0 - bit 0) is set
6	Reserved	0	Reserved.
5	N_DIV<11>	0	Programmable N divisor bit 11,10,9. Set these bits prior to enable M/N programming method.
4	N_DIV<10>	X	
3	N_DIV<9>	X	
2	KVAL<2>	X	Define the CPU/HTTCLK/PCI divider ratio
1	KVAL<1>	X	Refer to Table-1
0	KVAL<0>	X	

Note: This Byte 3:5 only for Winbond internal and BOIS program use; the release version please reserved this byte.

Table-1 CPU, HTTCLK, PCI divider ratio selection Table

KVAL2~KVAL0	CPU	HTTCLK	PCI
000	2	5	10
001	2	6	12
010	2	7	14
011	2	8	16
100	4	6	12
101	4	8	16
110	4	10	20
111	3	6	12

7.12 Register 11: Spread Spectrum Programming (Default = CAh)

BIT	NAME	PWD	DESCRIPTION
7	SPSP1	1	Spread Spectrum type select. 00 : Down 1%, 01 : Down 0.5% 10 : Center 1%, 11 : Center 0.5%
6	SPSP0	1	
5	SPCNT [5]	0	Spread Spectrum Programmable time, the resolution is 280ns The frequency of Spread Spectrum is 33KHz.
4	SPCNT [4]	0	
3	SPCNT [3]	1	
2	SPCNT [2]	0	
1	SPCNT [1]	1	
0	SPCNT [0]	0	

Note: Bits 0:5 only for Winbond internal and BOIS program use; the release version please reserved these bits

7.13 Register 12: SKEW Control (Default = 84h)

BIT	NAME	PWD	DESCRIPTION
7	CPU_PCI_SKEW [2]	1	CPU to PCI skew control, Skew resolution is 300ps The decision of skew direction is same as CPU_PCI_SKEW [2:0] setting.
6	CPU_PCI_SKEW [1]	0	
5	CPU_PCI_SKEW [0]	0	
4	Reserved	0	Reserved
3	FIX_HTTCLK_PCI	0	0: normal mode: the HTTCLK/PCI is synchronous with CPU 1: fix mode: the HTTCLK/PCI is asynchronous with CPU and fix in 72/36 MHz output frequency.
2	CPU_HTTCLK_SKEW [2]	1	CPU to PCI_HTTCLK skews control. Skew resolution is 300ps The decision of skew direction is same as CPU_HTTCLK_SKEW [2:0] setting.
1	CPU_HTTCLK_SKEW [1]	0	
0	CPU_HTTCLK_SKEW [0]	0	

Note: The skew rate control select bit fit value Please felloe below table.

SKEW bit[2:0]	000	001	010	011	100	101	110	111
Unit	-4	-3	-2	-1	0	1	2	3

Note: Each unit means 300ps

Note: skew bits only for Winbond internal and BOIS program use; the release version please reserved these bits.

7.14 Register 13: Winbond Chip ID (Default = 46h) (Read Only)

BIT	NAME	PWD	DESCRIPTION
7	CHPI_ID [7]	0	Winbond Chip ID. W83194BR-K8 (SA5846).
6	CHPI_ID [6]	1	Winbond Chip ID.
5	CHPI_ID [5]	0	Winbond Chip ID.
4	CHPI_ID [4]	0	Winbond Chip ID.
3	CHPI_ID [3]	0	Winbond Chip ID.
2	CHPI_ID [2]	1	Winbond Chip ID.
1	CHPI_ID [1]	1	Winbond Chip ID.
0	CHPI_ID [0]	0	Winbond Chip ID.

7.15 Register 14: Winbond Chip ID (Default = 55h) (Read Only)

BIT	NAME	PWD	DESCRIPTION
7	MAS_ID [1]	0	Winbond Master-Chip ID.
6	MAS_ID [0]	1	Winbond Master-Chip ID.
5	SUB_ID [1]	0	Winbond Sub-Chip ID.
4	SUB_ID [0]	1	Winbond Sub-Chip ID.
3	MAS_VER_ID [1]	0	Winbond Master's Version ID.
2	MAS_VER_ID [0]	1	Winbond Master's Version ID.
1	SUB_VER_ID [1]	0	Winbond Sub's Version ID.
0	SUB_VER_ID [0]	1	Winbond Sub's Version ID.

Note: The slew rate control select bit fit value Please felloe below table.

S2	S1	SLEW RATE STATUS
0	0	Weak
0	1	Normal
1	0	Strong
1	1	More Strong

7.16 Register 15: REF & PCI Output Slew-Rate control (Default = 25h)

BIT	NAME	PWD	DESCRIPTION
7	REF_S1	0	REF Pin 1, 48, 45 output slew rate control bit.
6	REF_S2	0	This slew rate status default is Weak
5	PCIA_S1	1	PCI Pin 12, 13,14,21,22 output slew rate control bit.
4	PCIA_S2	0	This slew rate status default is normal
3	PCIB_S1	0	PCI Pin 17, 18, 24 output slew rate control bit.
2	PCIB_S2	1	This slew rate status default is strong
1	PCIF_S1	0	PCI Pin 23 output slew rate control bit.
0	PCIF_S2	1	This slew rate status default is strong

7.17 Register 16: HTTCLK & 24_48MHz Slew-Rate control (Default = 95h)

BIT	NAME	PWD	DESCRIPTION
7	HTTCLK_0_S1	1	HTTCLK_0 Pin 6 output slew rate control bit.
6	HTTCLK_0_S2	0	This slew rate status default is normal
5	HTTCLK_12_S1	0	HTTCLK_1:2 Pin 7, 8 output slew rate control bit.
4	HTTCLK_12_S2	1	This slew rate status default is strong
3	HTTCLK_3_S1	0	HTTCLK_3 Pin 11 output slew rate control bit.
2	HTTCLK_3_S2	1	This slew rate status default is strong
1	P24M_S1	0	24_48MHz Pin 28 output slew rate control bit.
0	P24M_S2	1	This slew rate status default is strong

7.18 Register 17: Slew Rate Control (Default = AAh)

BIT	NAME	PWD	DESCRIPTION
7	P48M_S1	1	48MHz Pin 31 output slew rate control bit.
6	P48M_S2	0	This slew rate status default is Normal
5	CPU_S1	1	CPU Pin 36,37,40,41 output slew rate control bit.
4	CPU_S2	0	This slew rate status default is Normal
3	IVAL<3>	1	Charge pump current selection
2	IVAL<2>	X	Charge pump current selection
1	IVAL<1>	X	Charge pump current selection
0	IVAL<0>	X	Charge pump current selection

Note: This Byte 0:3 only for Winbond internal and BIOS program use; the release version please reserved this byte.

8. ACCESS INTERFACE

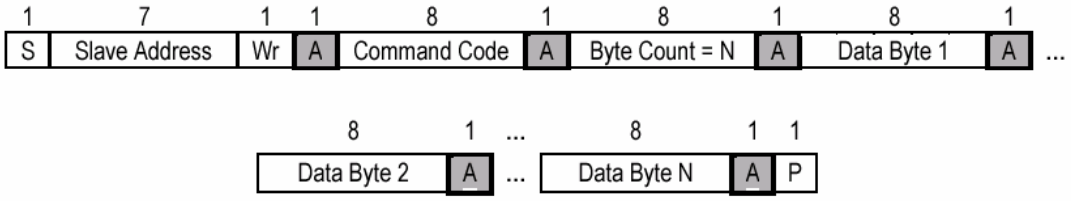
The W83194BR-K8 supports I^2C Serial Bus Block Read/Block Write and Byte-Data Read/Write protocol for microprocessor to read/write internal registers The I^2C address is 0xD2h.

The register number is incremented by one if using byte data read/write protocol.

Example: In block mode, byte number of program register is 1
In byte mode, byte number of program register is 2 (Byte number of block mode +1)

Block Read and Block Write Protocol

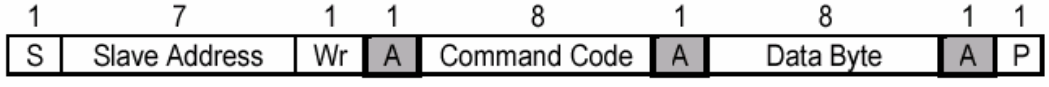
8.1 Block Write protocol



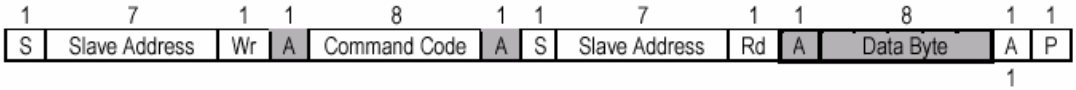
8.2 Block Read protocol

In block mode, the command code must filled 00H

8.3 Byte Write protocol



8.4 Byte Read protocol



9. SPECIFICATIONS

9.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or VDD) by external of internal pull-up or pull-down resistors.

PARAMETER	RATING
Absolute 3.3V Core Supply Voltage	-0.5V to +4.6V
Absolute 3.3V I/O Supple Voltage	- 0.5 V to + 4.6 V
Operating 3.3V Core Supply Voltage	3.135V to 3.465V
Operating 3.3V I/O Supple Voltage	3.135V to 3.465V
Storage Temperature	- 65°C to + 150°C
Ambient Temperature	- 55°C to + 125°C
Operating Temperature	0°C to + 70°C
Input ESD protection (Human body model)	2000V

9.2 DC Operating Characteristics

VDDREF =VDDA=VDDCPU=VDDPCI=VDD48= 3.3V ± 5 %, TA = 0℃ to +70℃, CI=10pF					
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Input Low Voltage	V_{IL}		0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0		V_{dc}	
Output Low Voltage	V_{OL}		0.4	V_{dc}	All outputs using 3.3V power
Output High Voltage	V_{OH}	2.4		V_{dc}	All outputs using 3.3V power
Operating Supply Current	I_{dd}		300	mA	CPU = 100 to 309 MHz PCI = 33.3 MHz with load
Input pin capacitance	Cin		5	pF	
Output pin capacitance	Cout		6	pF	
Input pin inductance	Lin		7	nH	

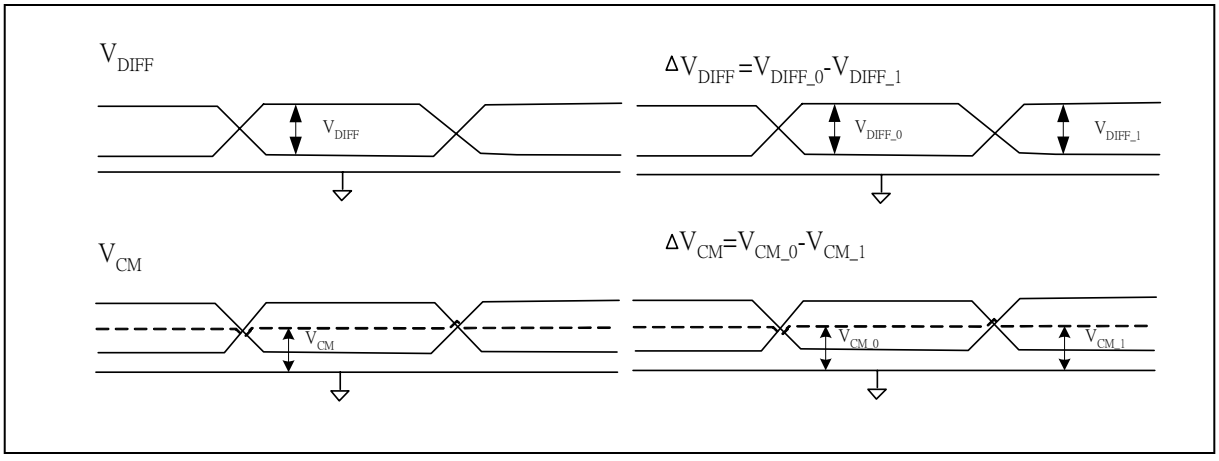
9.3 Clock Skews

VDDREF =VDDA=VDDCPU=VDDPCI=VDD48= 3.3V ± 5 %, TA = 0℃ to +70℃, CI=10pF					
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**	**TEST CONDITIONS**
CPU to CPU Skew			250	ps	Crossing point for CPUT rising edge
CPU to PCI Skew			500	ps	Crossing point for CPUT rising edge and 1.5V for PCI clocks
CPU to HTTCLK Skew			500	Ps	Crossing point for CPUT rising edge and 1.5V for HTTCLK clocks
PCI to PCI Skew			500	ps	Measured between rising edges at 1.5V
PCI to HTTCLK Skew			500	ps	Measured between rising edges at 1.5V
HTTCLK to HTTCLK Skew			500	ps	Measured between rising edges at 1.5V
48MHz to 48MHz Skew			1000	ps	Measured between rising edges at 1.5V
REF to REF Skew			500	ps	Measured between rising edges at 1.5V

9.4 CPU Clock Electrical Characteristics

VDDCPU= 3.3V ± 5 %, TA = 0℃ to +70℃, CI=10pF,					
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Edge Rate	2		10	V/ns	Measured at CPU test load. 0V ± 400mV (differential measurement)
Fall Edge Rate	2		10	V/ns	Measured at CPU test load. 0V ± 400mV (differential measurement)
V_{DIFF}: Differential Voltage (Single ended)	0.4	1.25	2.3	V	Measured at CPU test load. (Single ended measurement)
Δ V_{DIFF}: Change in V_{DIFF_DC} Magnitude	-150		+150	mV	Measured at CPU test load. (Single ended measurement)
V_{CM}: Common Mode Voltage	1.05	1.25	1.45	V	Measured at CPU test load. (Single ended measurement)
ΔV_{CM}: Change Common Voltage	-200		+200	mV	Measured at CPU test load. (Single ended measurement)
Duty Cycle	45	50	53	%	Measure at the differential crossing point
Cycle to Cycle Jitter		100	200	ps	Measured at the differential crossing point. Maximum difference of cycle time between two adjacent cycles.
Frequency Stabilization from Power-up (cold start)	0		3	ms	Measured from full supply voltage

Single-Ended Measurement Definitions



9.5 HTTCLK Clock Electrical Characteristics

VDDPCI= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, CI=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Edge Rate	1	4	V/ns	Measured from 20% to 60%
Fall Edge Rate	1	4	V/ns	Measured from 20% to 60%
Cycle to Cycle jitter		250	ps	Measured on rising edge at 1.5V, Maximum difference of cycle time between two adjacent cycles.
Jitter Accumulated	-1000	1000	ps	Measured using the JIT2 software package
Duty Cycle	45	55	%	Measured on rising and falling edge at 1.5V
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.6 PCI Clock Electrical Characteristics

VDDPCI= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, CI=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Edge Rate	1	4	V/ns	Measured from 20% to 60%
Fall Edge Rate	1	4	V/ns	Measured from 20% to 60%
Cycle to Cycle jitter		250	ps	Measured on rising edge at 1.5V, Maximum difference of cycle time between two adjacent cycles.
Jitter Accumulated	-1000	1000	ps	Measured using the JIT2 software package
Duty Cycle	45	55	%	Measured on rising and falling edge at 1.5V
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.7 24M, 48M Clock Electrical Characteristics

VDD48= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Edge Rate	0.5	2	V/ns	Measured from 20% to 80%
Fall Edge Rate	0.5	2	V/ns	Measured from 20% to 80%
Cycle to Cycle jitter		500	ps	Measured on rising edge at 1.5V, Maximum difference of cycle time between two adjacent cycles.
Jitter Accumulated	-1000	1000	ps	Measured using the JIT2 software package
Duty Cycle	45	55	%	Measured on rising and falling edge at 1.5V
Pull-Up Current Min	-29		mA	Vout=1.0V
Pull-Up Current Max		-23	mA	Vout=3.135V
Pull-Down Current Min	29		mA	Vout=1.95V
Pull-Down Current Max		27	mA	Vout=0.4V

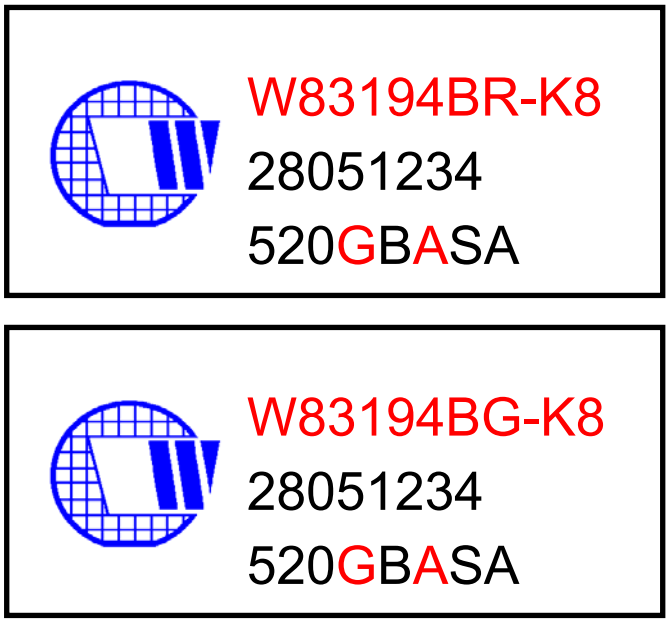
9.8 REF Electrical Characteristics

VDDREF= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Edge Rate	0.5	2	V/ns	Measured from 20% to 80%
Fall Edge Rate	0.5	2	V/ns	Measured from 20% to 80%
Cycle to Cycle jitter		1000	ps	Measured on rising edge at 1.5V, Maximum difference of cycle time between two adjacent cycles.
Jitter Accumulated	-1000	1000	ps	Measured using the JIT2 software package
Duty Cycle	45	55	%	Measured on rising and falling edge at 1.5V
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

10. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83194BR-K8	48 PIN SSOP	Commercial, 0°C to +70°C
W83194BG-K8	48 PIN SSOP(Lead free part)	Commercial, 0°C to +70°C

11. HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: Normal: W83194BR-K8, Lead free part: W83194BG-K8

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 520 G B A SA

520: packages made in '2005, week 20

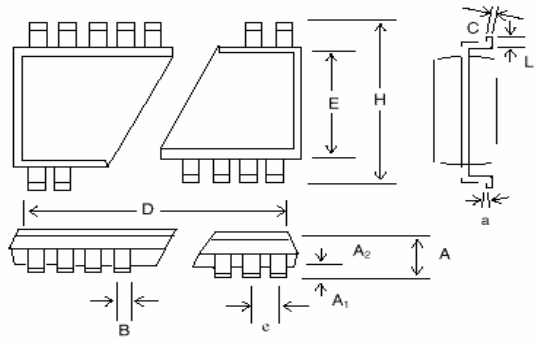
G: assembly house ID; O means OSE, G means GR

B: Internal use code

A: IC revision

SA: Internal use code

12. PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

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