Signetics

FAST 74F30240,74F30244
30Ω Line Drivers

FAST Products

'F30240 Octal 30Ω Line Driver With Enable, Inverting (Open Collector)
'F30244 Octal 30Ω Line Driver With Enable, Non-Inverting (Open Collector)
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F30240	9.5ns	62.5mA
74F30244	10.5ns	69mA

FEATURES

- Ideal for driving transmission lines or backplanes. 160mA I_{OL} ideal for applications with impedance as low as 30Ω
- Guaranteed threshold voltages on the incident wave while driving line as low as 30Ω.
- High impedance NPN base inputs for reduced loading (20μA in High and Low states)
- Ideal for applications which require high output drive and minimal bus loading
- Octal interface
- 'F30240 Inverting
- 'F30244 Non-Inverting
- Open-Collector outputs sink 160mA
- Multiple side pins are used for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)
- Available in 24-pin standard slim DIP (300mil) plastic or CERDIP packages

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Cerdip (300 mil)	N74F30240F, N74F30244F
24-Pin Plastic Slim DIP(300 mil)[1]	N74F30240N, N74F30244N

NOTE:
1.Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

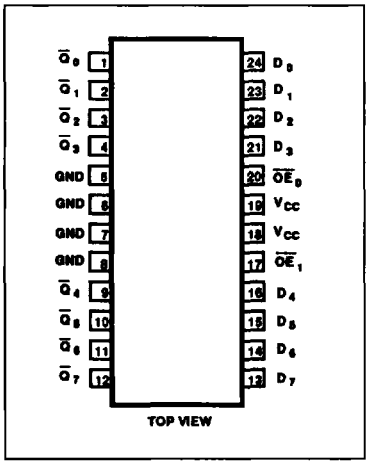
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0- D_7	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_0$- $\overline{OE}_1$	Output Enable inputs (active Low)	1.0/0.033	20μA/20μA
$\overline{O}_0$- $\overline{O}_7$	Data outputs (OC) for 'F30240	OC/266.7	OC/160mA
O_0- O_7	Data outputs (OC) for 'F30244	OC/266.7	OC/160mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC = Open Collector

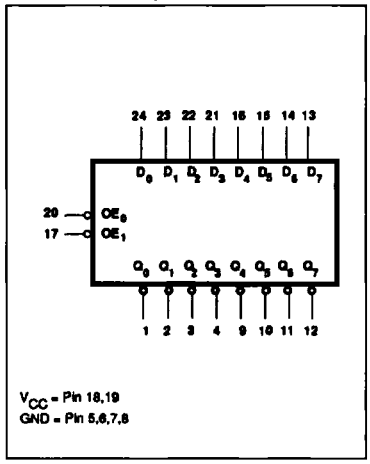
DESCRIPTION

The 74F30240/F30244 are high current open collectors octal buffers composed of eight inverters. The 'F30240 has inverting data paths and the 'F30244 has non-inverting paths. Each device has eight inverters with two Output Enables($\overline{OE}_0$, $\overline{OE}_1$) each controlling four outputs. Both drivers are designed to deal with the low-impedance transmission line effects found on printed circuit boards when fast edge rates are used. The 160 mA I_{OL} provides ample power to achieve TTL switching voltages on the incident wave.

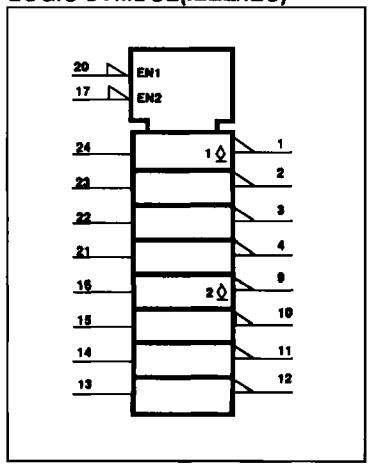
PIN CONFIGURATION



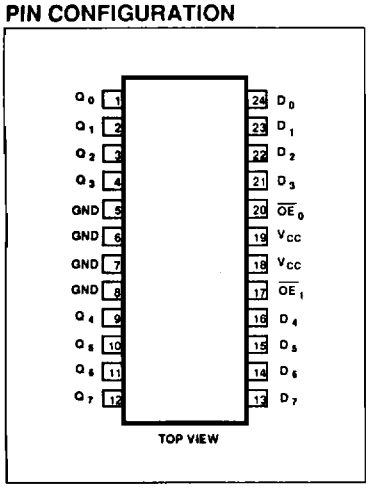
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



PIN CONFIGURATION



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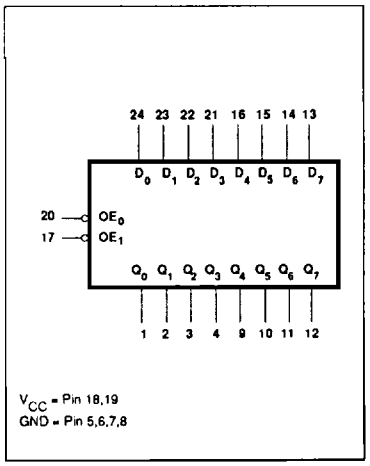

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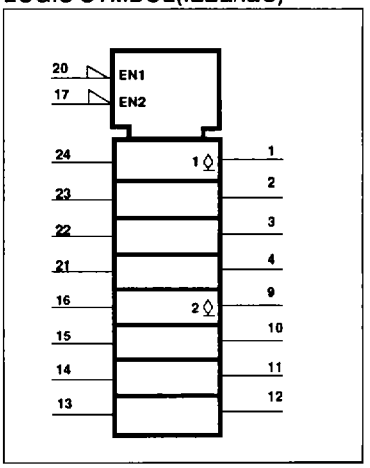
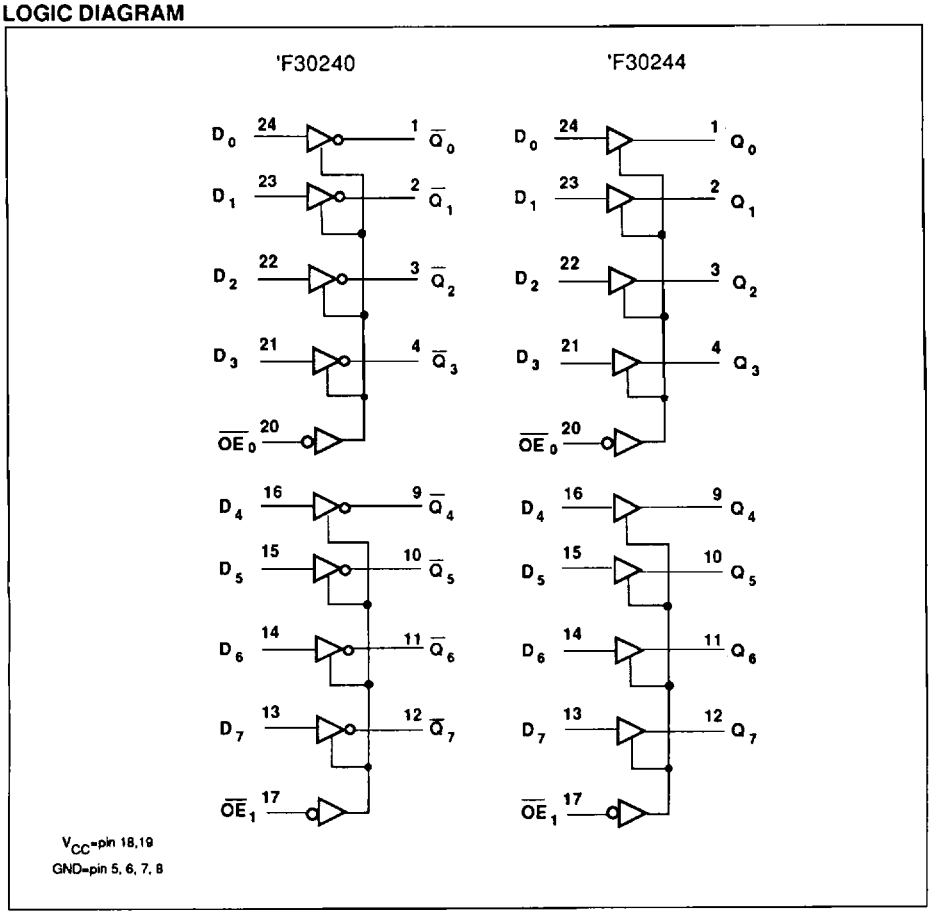


LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS	
		'F30240	'F30244
$\overline{OE}_n$	D_n	$\overline{Q}_n$	Q_n
L	L	H	L
L	H	L	H
H	X	OFF	OFF

H=High voltage level
L=Low voltage level
X=Don't care
OFF=Pulled up through resistor (open collector)

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	320	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			160	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

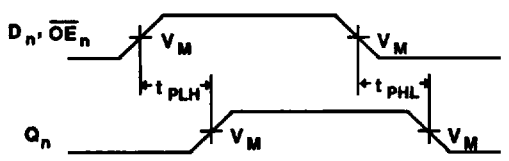
SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
I_{OH}	High-level output current			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OL}	Low-level output current			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		.42	.55	V
					I_{OL} = 160mA[3]	±5%V_{CC}			.80	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{CC}	Supply current [total]	'F30240	I_{CCH}	V_{CC} = MAX				13	23	mA
			I_{CCL}					70	95	mA
		'F30244	I_{CCH}					19	27	mA
			I_{CCL}					70	100	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30Ω transmission line on the incident wave.

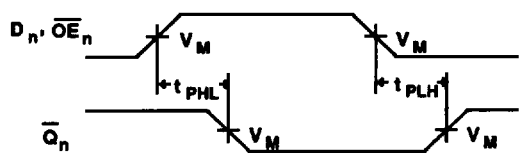
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	LIMITS T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{O}_n$	'F30240	Waveform 2	4.0 1.0	10.0 2.0	14.5 5.0	4.0 1.0	15.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_n$ to $\overline{O}_n$	'F30240	Waveform 1,2	4.0 3.5	10.0 6.0	14.0 9.0	4.0 3.5	14.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{O}_n$	'F30244	Waveform 1	4.0 3.0	10.5 5.5	14.5 9.0	4.0 3.0	15.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_n$ to $\overline{O}_n$	'F30244	Waveform 1,2	4.0 3.5	9.5 6.0	14.0 9.0	4.0 3.5	14.5 10.5	ns

AC WAVEFORMS



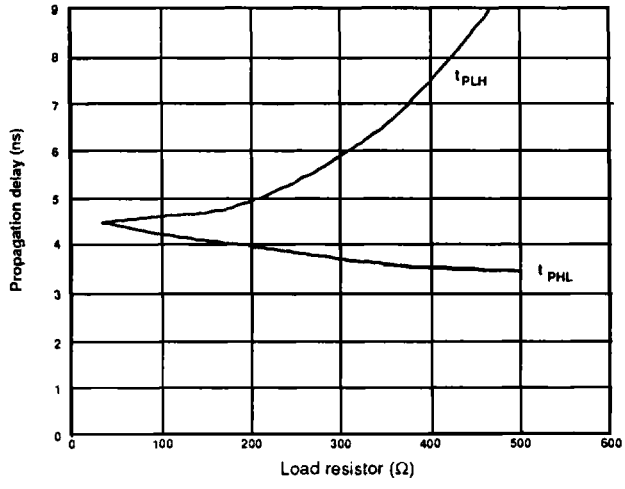
Waveform 1. Propagation Delay For Data To Output



Waveform 2. Propagation Delay For Data To Output

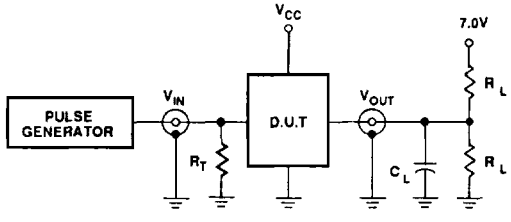
NOTE: For all waveforms, V_M = 1.5V.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

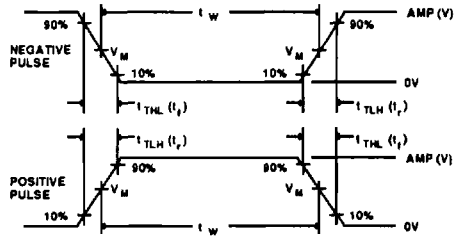


NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns