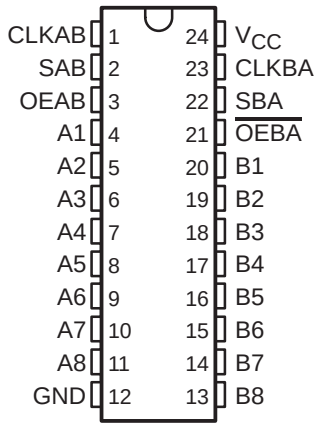
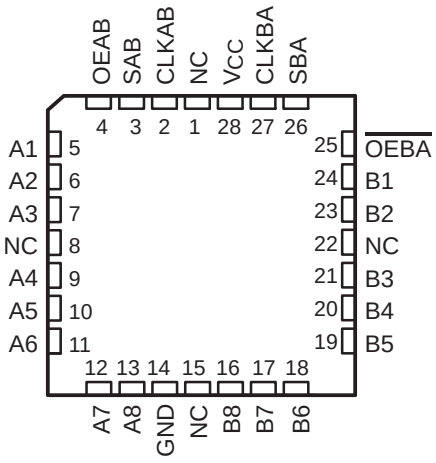
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Power-Up High-Impedance Mode**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic and Ceramic 300-mil DIPs (JT, NT)**

SN54BCT652 . . . JT OR W PACKAGE
SN74BCT652 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54BCT652 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the ′BCT652.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration each output reinforces its input. Therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remain at its last state.

The SN54BCT652 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74BCT652 is characterized for operation from 0°C to 70°C.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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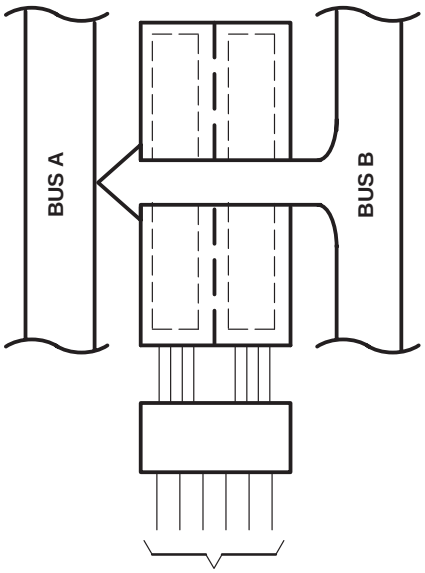
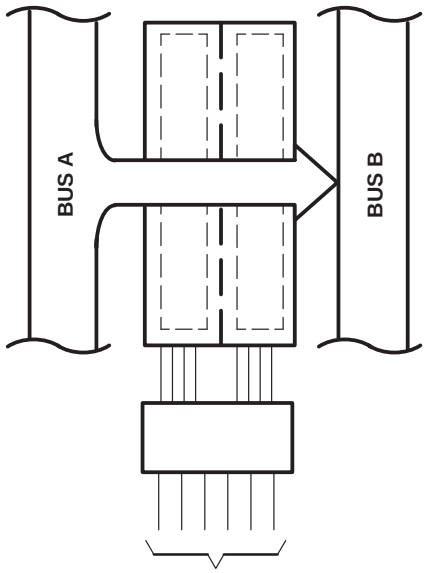


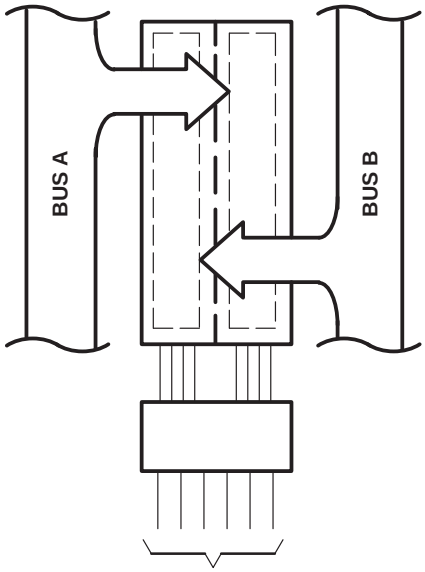
3	21	1	23	2	22
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



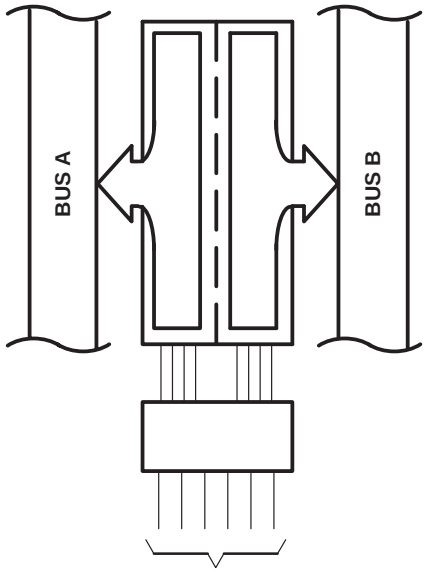
3	21	1	23	2	22
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



3	21	1	23	2	22
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



3	21	1	23	2	22
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
H	L	L	L	H	H
L	L	X	L	X	H
H	H	L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

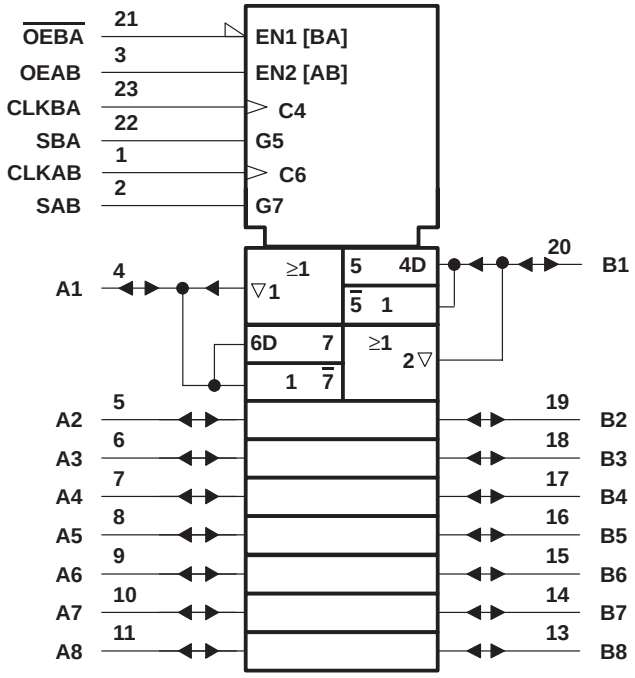
Pin numbers shown are for the DW, JT, NT, and W packages.

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

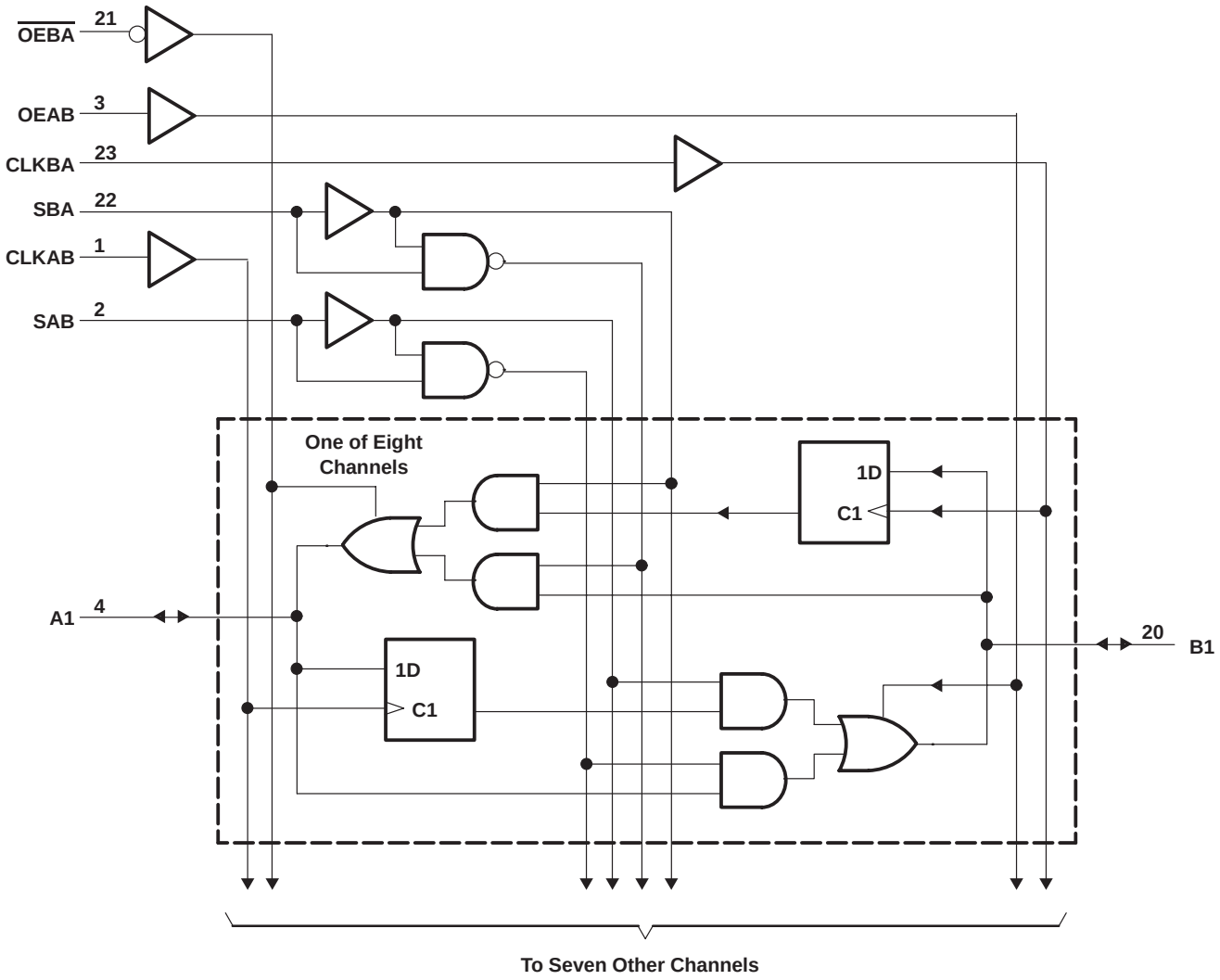
† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{\text{OEBA}}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.
‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered in order to load both registers.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, NT, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . – 0.5 V to 7 V
Input voltage range: Control inputs (see Note 1) . . . . . – 0.5 V to 7 V
I/O ports (see Note 1) . . . . . – 0.5 V to 5.5 V
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . – 0.5 V to 7 V
Voltage range applied to any output in the high state, V_O . . . . . – 0.5 V to V_{CC}
Current into any output in the low state: SN54BCT652 . . . . . 96 mA
SN74BCT652 . . . . . 128 mA
Operating free-air temperature range: SN54BCT652 . . . . . – 55°C to 125°C
SN74BCT652 . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		SN54BCT652			SN74BCT652			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			–18			–18	mA
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT652			SN74BCT652			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V	I_{OH} = –3 mA	2.4	3.3		2.4	3.3		V
			I_{OH} = –12 mA	2	3.2					
			I_{OH} = –15 mA				2	3.1		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
			I_{OL} = 64 mA					0.42	0.55	
I_I	A or B port	V_{CC} = 5.5 V,	V_I = 5.5 V			1			1	mA
	Control inputs					1			1	
I_{IH}‡	A or B port	V_{CC} = 5.5 V,	V_I = 2.7 V			70			70	µA
	Control inputs					20			20	
I_{IL}‡	A or B port	V_{CC} = 5.5 V,	V_I = 0.5 V			–0.7			–0.7	mA
	Control inputs					–0.7			–0.7	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	–100		–225	–100		–225	mA
I_{CCL}	A or B port	V_{CC} = 5.5 V,	V_I = 0		43	69		43	69	mA
I_{CCH}	A or B port	V_{CC} = 5.5 V,	V_I = 4.5 V		6	10		6	10	mA
I_{CCZ}	A or B port	V_{CC} = 5.5 V,	V_I = 0		10	17		10	17	mA
C_i	Control inputs	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		6			6		pF
C_{io}	A or B port	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V		14			14		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V_{CC} = 5 V, T_A = 25°C		SN54BCT652		SN7BCTT652		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	77	0	77	0	77	MHz
t_w	Pulse duration, CLK high or low	6.5		7		6.5		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	5		6		5		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	1		1		1		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54BCT652		SN74BCT652		UNIT
			MIN	TYP	MIN	MIN	MAX	MIN	MAX	
f_{max}			77			77		77		MHz
t_{PLH}	CLKBA	A	2.6	6.9	8.9	2.6	11.6	2.6	10.5	ns
t_{PHL}			2.8	6.8	8.8	2.8	10.7	2.8	9.9	
t_{PLH}	CLKAB	B	2.6	6.9	8.9	2.6	11.6	2.6	10.5	ns
t_{PHL}			2.8	6.8	8.8	2.8	10.7	2.8	9.9	
t_{PLH}	A	B	1.7	5.8	7.5	1.7	10.3	1.7	8.9	ns
t_{PHL}			2.4	6.5	8.2	2.4	11	2.4	9.8	
t_{PLH}	B	A	1.7	5.8	7.5	1.7	10.3	1.7	8.9	ns
t_{PHL}			2.4	6.5	8.2	2.4	11	2.4	9.8	
t_{PLH}	SBA† (with B high)	A	3.5	8.8	10.8	3.5	14.2	3.5	13.1	ns
t_{PHL}			2.4	5.9	7.7	2.4	9.1	2.4	8.5	
t_{PLH}	SBA† (with B low)	A	3	7.6	9.7	3	12.4	3	11.3	ns
t_{PHL}			3.8	8.3	10.4	3.8	12.9	3.8	12.5	
t_{PLH}	SAB† (with A high)	B	3.5	8.8	10.8	3.5	14.2	3.5	13.1	ns
t_{PHL}			2.4	5.9	7.7	2.4	9.1	2.4	8.5	
t_{PLH}	SAB† (with A low)	B	3	7.6	9.7	3	12.4	3	11.3	ns
t_{PHL}			3.8	8.3	10.4	3.8	12.9	3.8	12.5	
t_{PZH}	OEBA	A	2.5	7.2	8.9	2.5	11.2	2.5	10.6	ns
t_{PZL}			3.2	8.1	10.1	3.2	12.6	3.2	12	
t_{PHZ}	$\overline{OEBA}$	A	2.8	6.7	8.6	2.8	10.9	2.8	10	ns
t_{PLZ}			2.4	6.3	8.4	2.4	10.5	2.4	9.5	
t_{PZH}	OEAB	B	1.5	5.4	7.1	1.5	9	1.5	8.1	ns
t_{PZL}			2.3	6.2	8.1	2.3	10.3	2.3	9.3	
t_{PHZ}	OEAB	B	3.5	8.2	10	3.5	12.2	3.5	11.6	ns
t_{PLZ}			2.8	7.2	9.5	2.8	12	2.8	11.3	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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SN54BCT652, Octal Bus Transceivers And Registers With 3-State Outputs

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54BCT652	SN74BCT652
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.5 to 5.5
Input Level	TTL	TTL
Output Level	TTL	TTL
No. of Outputs	8	8
Static Current		39.5

FEATURES

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- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Power-Up High-Impedance Mode
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic and Ceramic 300-mil DIPs (JT, NT)

DESCRIPTION

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These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and $\overline{OEBA}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the ´BCT652.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins.

When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration each output reinforces its input. Therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remain at its last state.

The SN54BCT652 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT652 is characterized for operation from 0°C to 70°C.

TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: sn54bct652.pdf (112 KB,Rev.A) (Updated: 11/01/1993)

APPLICATION NOTES

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Product Folder: SN54BCT652, Octal Bus Transceivers And Registers With 3-State Outputs

View Application Notes for Digital Logic

- Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A) (SCBA012A - Updated: 08/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C - Updated: 02/01/1998)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- TI IBIS File Creation, Validation, and Distribution Processes (SZZA034 - Updated: 08/29/2002)
- Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh (Rev. A) (SZZA036A - Updated: 02/27/2003)

MORE LITERATURE

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- Enhanced Plastic Portfolio Brochure (SGZB004, 387 KB - Updated: 08/19/2002)
- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- Military Brief (SGYN138, 803 KB - Updated: 10/10/2000)
- Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet (Rev. A) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- Palladium Lead Finish User's Manual (SDYV001, 2041 KB - Updated: 11/01/1996)
- QML Class V Space Products Military Brief (Rev. A) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

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- LOGIC Pocket Data Book (SCYD013, 4837 KB - Updated: 12/05/2002)

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION
Updated Daily

ORDERABLE DEVICE	STATUS	PACKAGE TYPE | PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY
5962-9155301MKA	ACTIVE	CFP (W) | 24	-55 TO 125		View Contents	1KU | 13.13	1
5962-9155301MLA	ACTIVE	CDIP (JT) | 24	-55 TO 125		View Contents	1KU | 9.50	1
SNJ54BCT652FK	ACTIVE	LCCC (FK) | 28	-55 TO 125		View Contents	1KU | 13.83	1
SNJ54BCT652JT	ACTIVE	CDIP (JT) | 24	-55 TO 125	5962-9155301MLA	View Contents	1KU | 9.50	1
SNJ54BCT652W	ACTIVE	CFP (W) | 24	-55 TO 125	5962-9155301MKA	View Contents	1KU | 13.13	1

TI INVENTORY STATUS
As Of 09:00 AM GMT, 17 Apr 2003

IN STOCK	IN PROGRESS QTY | DATE	LEAD TIME
0*	>10k | 20 May	8 WKS
0*	>10k | 20 May	8 WKS
0*	3889 | 20 May	8 WKS
	>10k | 27 May	
249*	>10k | 20 May	8 WKS
0*	>10k | 20 May	8 WKS

REPORTED DISTRIBUTOR INVENTORY
As Of 09:00 AM GMT, 17 Apr 2003

DISTRIBUTOR COMPANY | REGION	IN STOCK	PURCHASE
None Reported View Distributors		
None Reported View Distributors		
None Reported View Distributors		
Avnet-SILICA | Europe	1	BUY NOW
None Reported View Distributors		

Table Data Updated on: 4/17/2003

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Product Folder: SN54BCT652, Octal Bus Transceivers And Registers With 3-State Outputs

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