C9929

Low EMI Clock Generator for Intel® 133MHz/3DIMM Chipset Systems

Product Features

- Designed for Intel's 133MHz/SDRAM chipset
- 2 copies of CPU Clock (CPU[0:1])
- 13 copies of SDRAM Clock (SDRAM[0:12])
- 7 copies of PCI Clocks
- 3 copies of 3V66 Clock
- 1 IOAPIC Clock, synchronous to PCI Clock
- 1 REF Clock
- 1 USB Clock (Non SSC)
- 1 DOT Clock (Non SSC)
- IMI Spread Spectrum for best EMI reduction
- Dial-a-Frequency™ Feature
- Dial-a-dB™ Feature
- 56 Pin SSOP

Block Diagram

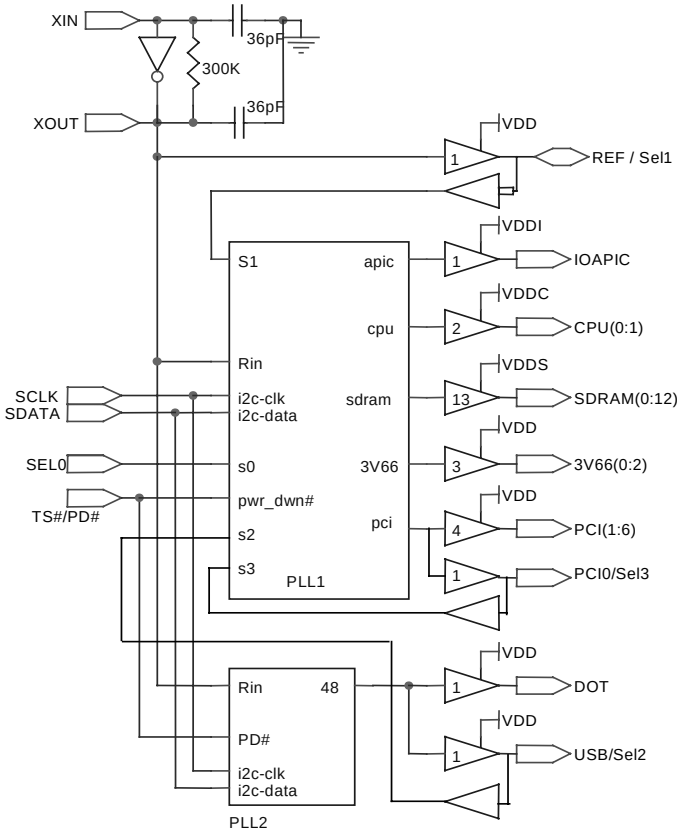


Fig.1

Frequency Table (MHz)

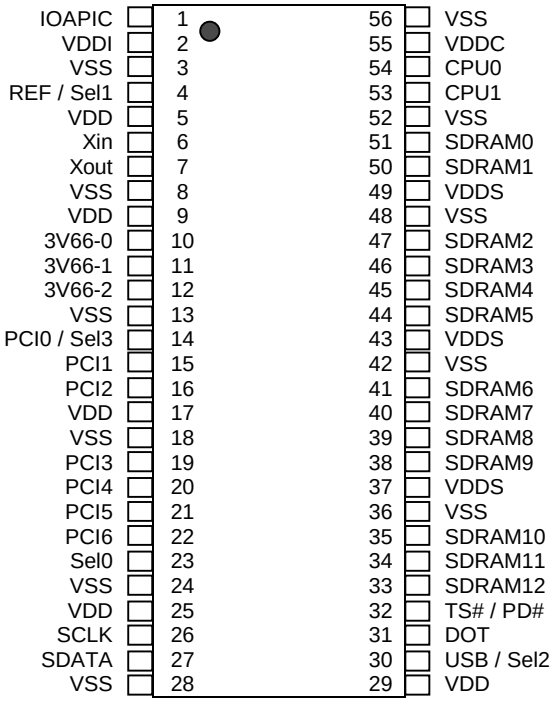
SEL (3:0)**	CPU	SDRAM	3V66	PCI /IOAPIC	REF	DOT	USB
0000	66.67	100.00*	66.67	33.33	14.318M	48M	48M
0001	100.00	100.00*	66.67	33.33	14.318M	48M	48M
0010	133.33	133.33	66.67	33.33	14.318M	48M	48M
0011	133.33	100.00*	66.67	33.33	14.318M	48M	48M
0100	83.35	125.02	83.35	41.67	14.318M	48M	48M
0101	106.91	106.91	71.27	35.64	14.318M	48M	48M
0110	150.00	150.00	75.00	37.50	14.318M	48M	48M
0111	120.96	120.96	80.64	40.32	14.318M	48M	48M
1000	89.90	134.86	89.90	44.95	14.318M	48M	48M
1001	125.02	125.02	83.35	41.67	14.318M	48M	48M
1010	200.00	200.00	100.00	50.00	14.318M	48M	48M
1011	116.87	116.87	77.91	38.96	14.318M	48M	48M
1100	100.00	133.33	66.67	33.33	14.318M	48M	48M
1101	112.00	112.00	74.67	37.33	14.318M	48M	48M
1110	166.53	166.53	83.27	41.63	14.318M	48M	48M
1111	140.00	105.00	70.00	35.00	14.318M	48M	48M

Table1

*Will be set to 133 MHz, SMBus Byte3, Bit0 is set to a Logic 1.

**Sel0 also controls TS# functionality if TS# is 0 at power up.

Pin Configuration



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Pin Description

PIN No.	Pin Name	PWR	I/O	TYPE	Description
1	**IOAPIC**	VDDI	O		2.5V IOAPIC clock output. See fig.3 p.4 for timing relationship.
4	**SEL1 / REF**	VDD	I/O	PD	This is a bi-directional pin (see app. note, p.6). At power up, it is an input pin Sel1 for frequency selection (see table 1 p.1). When the power reaches the rail, the state of Sel1 is latched, and this pin becomes REF, a buffer output of the signal applied at Xin, typically 14.318MHz.
6	**XIN**	VDD	I	OSC1	On-chip reference oscillator input pin. Requires either an external parallel resonant crystal (nominally 14.318 MHz) or externally generated reference signal
7	**XOUT**	VDD	O		On-chip reference oscillator pin. Drives an external parallel resonant crystal. When an externally generated reference signal is used at Xin, this pin remains unconnected.
14	**SEL3 / PCI0**	VDD	I/O	PD	This is a bi-directional pin (see app. note, p.6). At power up, it is an input pin Sel3 for frequency selection (see table 1 p.1). When the power reaches the rail, the state of Sel3 is latched, and this pin becomes PCI clock output.
15, 16, 19, 20, 21, 22	**PCI(1:6)**	VDD	O		3.3V PCI clock outputs. They are Synchronous to CPU clocks. See fig.3, page4.
10, 11, 12	**3V66(0:2)**	VDD	O		3.3V Hub/AGP clock outputs. See fig.3 page 4.
30	**SEL2 / USB**	VDD	I/O	PD	This is a bi-directional pin (see app. note, p.6). At power up, it is an input pin Sel2 for frequency selection (see table 1 p.1). When the power reaches the rail, the state of Sel2 is latched, and this pin becomes a fixed 48MHz clock output for USB.
31	**DOT**	VDD	O		3.3V Fixed 48 MHz DOT clock output.
23	**SEL0**	VDD	I	PU	3.3V LVTTL inputs for frequency selection, see table 1 page 1. Sel0 also controls TS# functionality if TS# is 0 during power up (See pg.7).
27	**SDATA**	VDD	I		Serial data input pin. Conforms to the SMBus specification of a Slave Receive/Transmit device. This pin is an input when receiving data. It is an open drain output when acknowledging or transmitting data. See SMBus function description, pp. 8,9,10.
26	**SCLK**	VDD	I		Serial clock input pin. Conforms to the SMBus specification.
32	**TS# / PD#**	VDD	I	PU	This is a dual function pin. During power up, if TS# is low, it serves as a Tristate control (TS#). Once high, this pin becomes a Power Down control (PD#). See page 7 for detailed description.
33,34,35,38, 39,40,41,44, 45,46,47,50,51	**SDRAM (0:12)**	VDDS	O		3.3V SDRAM DIMM clocks. See table1, p.1 for frequency selection. See fig.3, page 4 for timing relationship and SMBus Byte3, Bit0.
53, 54	**CPU(0:1)**	VDDC	O		2.5V Host clock outputs. See table1,p.1 for frequency selection.
5,9,17,25,29	**VDD**	-			3.3V Common Power Supply
55, 2	**VDDC,VDDI**	-			2.5V Power Supply for CPU(0:1) and IOAPIC clock respectively.
3,8,13,18,24, 28,36,42,48, 52,56	**VSS**	-		-	Common Ground pins.
37,43,49	**VDDS**	-		-	3.3V power support for SDRAM(0:12) clock output drivers.

PU = Internal Pull-Up. Typical 250KΩ (range 200KΩ to 500KΩ). PD = Internal Pull-Down. Typical 50KΩ (range 20KΩ to 70KΩ)

Test Mode Function

Test Mode Functionality

TS#	SEL0	CPU (0:1)	SDRAM (0:12)	3V66 (0:2)	PCI (_F, 1:5)	DOT/USB	REF	IOAPIC
0	1	TCLK/2	TCLK/2	TCLK/3	TCLK/6	TCLK/2	TCLK	TCLK/6
0	0	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate

Table 2

Note: TCLK is a test clock over driven on the XIN input during test mode. Test Mode/Tristate mode set during power up and if TS# is low. Also can be set through SMBus when Byte 3 bit6 = 1, Byte0 bit 0 = 1, and bit 4 = 4.

Power Management Functions

Power Management on this device is controlled by a single pin, PD# (pin32). When PD# is high (default) the device is in normal running mode and all signals are active.

When PD# is asserted (forced) low, the device is in shutdown (or in power down) mode and all power may be removed. When in power down, all outputs are synchronously stopped in a low state (see Fig.2 below), all PLL's are shut off, and the crystal oscillator is disabled. When the device is shutdown, the I²C function is also disabled.

Power Management Timing

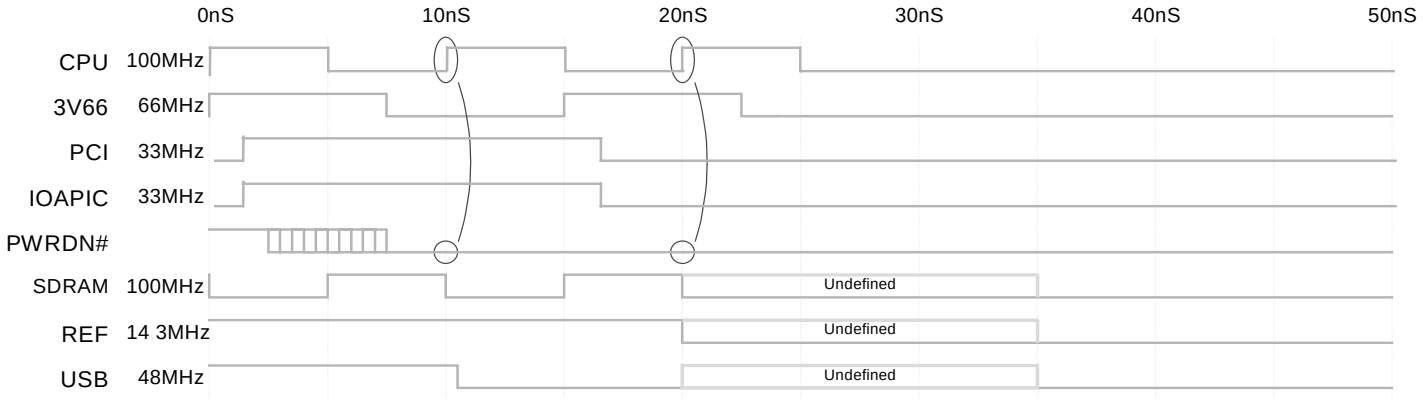


Fig.2

Power Management Current

PD#, SEL3, SEL2, SEL1, SEL0	Maximum 2.5 Volt Current Consumption (VDDC = VDDI =2.625)	Maximum 3.3 Volt Current Consumption (VDD = VDDA = VDDS = 3.465 V)
0XXXX (Power down)	10mA	10mA
10000 (66MHz)	70 mA	280 mA
10001 (100MHz)	100 mA	360 mA
1001X (133MHz)	133 mA	440 mA

Table 3

When exiting the power down mode, the designer must supply power to the VDD pins first, a minimum of 200mS before releasing the PD# pin high.

Clock Phase Relationships

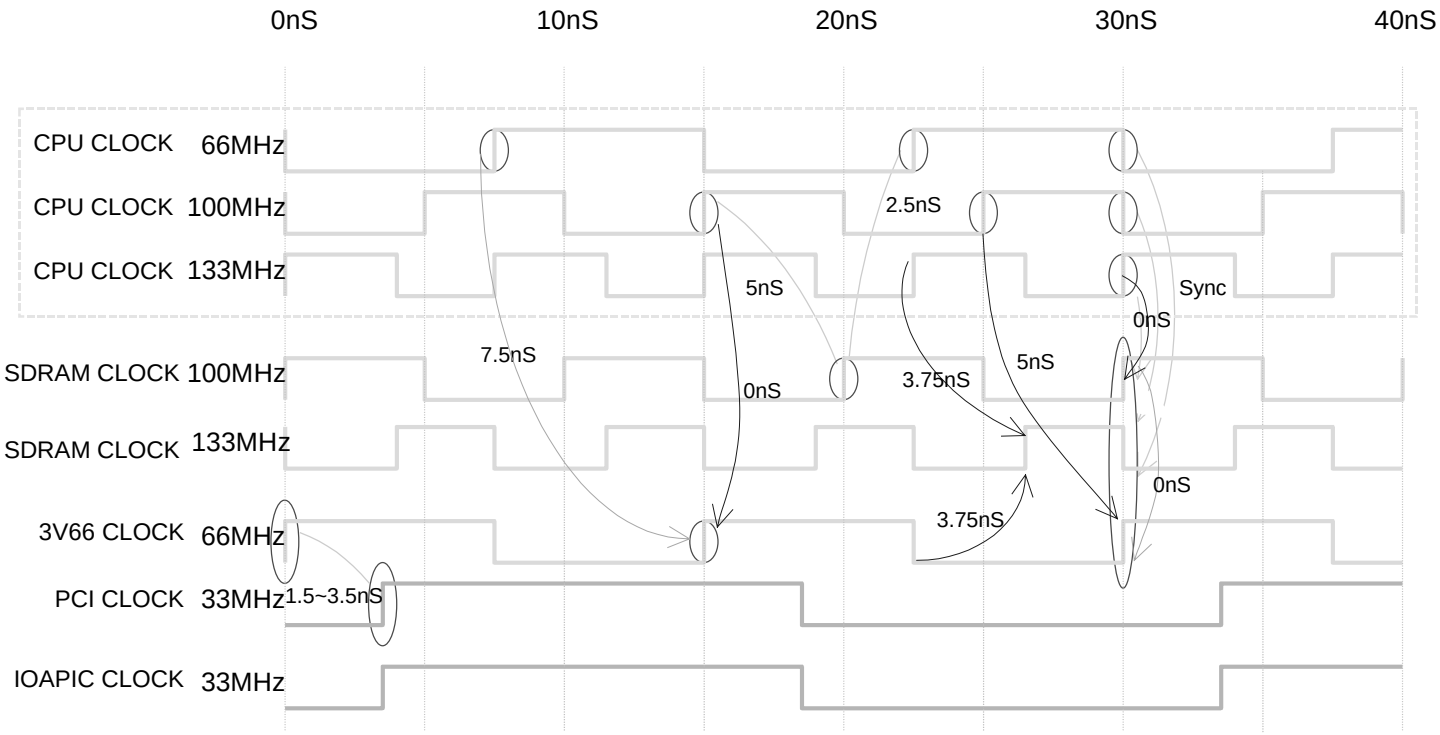


Fig.3

Group Timing Relationships and Tolerances

	CPU = 66.6 MHz, SDRAM = 100 MHz		
	Offset (nS)	**Tolerance (pS)**	**Conditions**
CPU to SDRAM	2.5	500	
CPU to 3V66	7.5	500	180 degrees phase shift
SDRAM to 3V66	0	500	When rising edges line-up
3V66 to PCI	1.5-3.5	500	3V66 leads
PCI to IOAPIC	0	1000	
	CPU = 100 MHz, SDRAM = 100 MHz		
	Offset (nS)	**Tolerance (pS)**	**Conditions**
CPU to SDRAM	5	500	180 degrees phase shift
CPU to 3V66	5	500	
SDRAM to 3V66	0	500	When rising edges line-up
3V66 to PCI	1.5-3.5	500	3V66 leads
PCI to IOAPIC	0	1000	
	CPU = 133.3 MHz, SDRAM = 100 MHz		
	Offset (nS)	**Tolerance (pS)**	**Conditions**
CPU to SDRAM	0	500	When rising edges line-up
CPU to 3V66	0	500	
SDRAM to 3V66	0	500	When rising edges line-up
3V66 to PCI	1.5-3.5	500	3V66 leads
PCI to IOAPIC	0	1000	
	CPU = 133.3 MHz, SDRAM = 133.3 MHz		
	Offset (nS)	**Tolerance (pS)**	**Conditions**
CPU to SDRAM	3.75	500	180 degrees phase shift
CPU to 3V66	0	500	
SDRAM to 3V66	3.75	500	
3V66 to PCI	1.5-3.5	500	3V66 leads
PCI to IOAPIC	0	1000	

Power on Bi-Directional Pins

Power Up Condition:

Pins 4, 14, 30 are Power up bi-directional pins and are used for selecting the host frequency in page 1, table 1. During power-up of the device, these pins are in input mode (see Fig 4, below), therefore; they are considered input select pins, Sel(1:3) internal to the IC. After a settling time, the selection data is latch into the internal control register and these pins become a clock output.

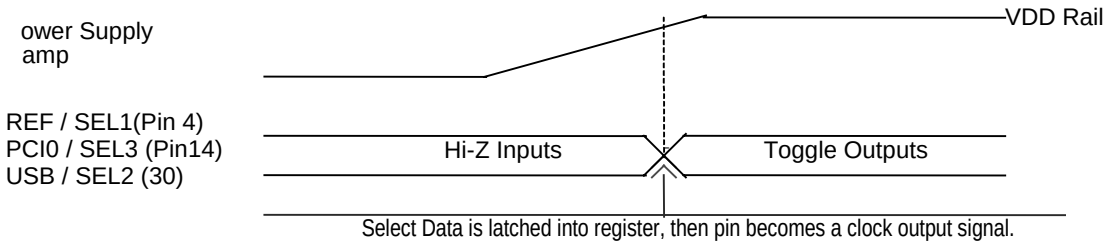


Fig.4

Strapping Resistor Options:

The power up bi-directional pins have a large value pull-down (50KΩ+/–20KΩ), therefore, a selection "0" is the default. If the system uses a slow power supply (over 10mS settling time), then **it is recommended** to use an external Pull-down (Rdn) in order to insure a low selection. In this case, the designer may choose one of two configurations, see Fig.5A and B.

Fig. 5A represents an additional pull down resistor 5KΩ connected from the pin to the power line, which allows a faster down to a high level.
If a selection "1" is desired, then a jumper is placed on JP1 to a 1 KΩ resistor as shown in Fig.5A. Please note the selection resistors (Rup and Rdn) are placed before the Damping resistor (Rd) close to the pin.

Fig. 5B represent a single resistor 5KΩ connected to a 3-way jumper, JP2. When a "1" selection is desired, a jumper is placed between leads1 and 3. When a "0" selection is desired, a jumper is placed between leads 1 and 2.

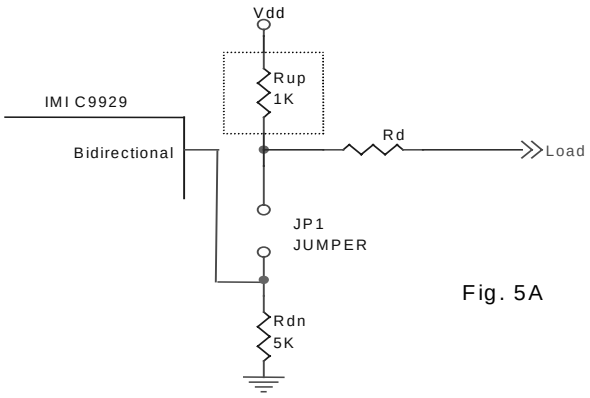


Fig. 5A

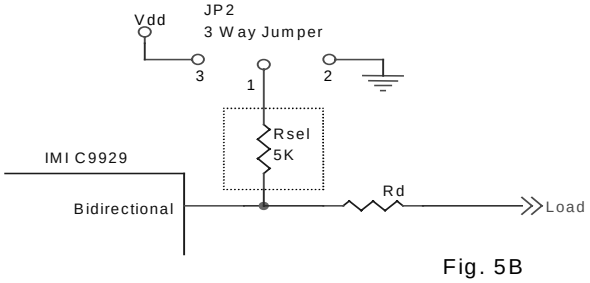


Fig. 5B

Power on Bi-Functional Pins (Cont.)

Pin 32 (TS# / PD#) is a bi-functional pin, See Fig.6. If this pin is externally held low during power up, the device is forced into tristate/or test mode depending on the state of Sel0.

In Tristate mode, all outputs assume the high impedance (Hi-Z) state. In test, all outputs toggle as described in table 2, page 3.

All outputs remain in their Hi-Z state (or test mode) until the external signal applied to pin 32 is released (set high). After a minimum of 1.5mS from a stable 3.3V power supply or until TS# is released (whichever is longer), pin 32 changes from a tristate controller (TS#) to Power Down controller (PD#) and remains in that function unless otherwise programmed through the SMBus to return to the TS# function by setting byte3, bit1 to a "0". Once the TS# signal is released (high), pin 32 may be toggled repetitively to force the device in and out of power down mode.

The device is considered in power down when PD# is asserted low, consequently, all clocks are stopped synchronously and after the completion of a full period (glitch-free).

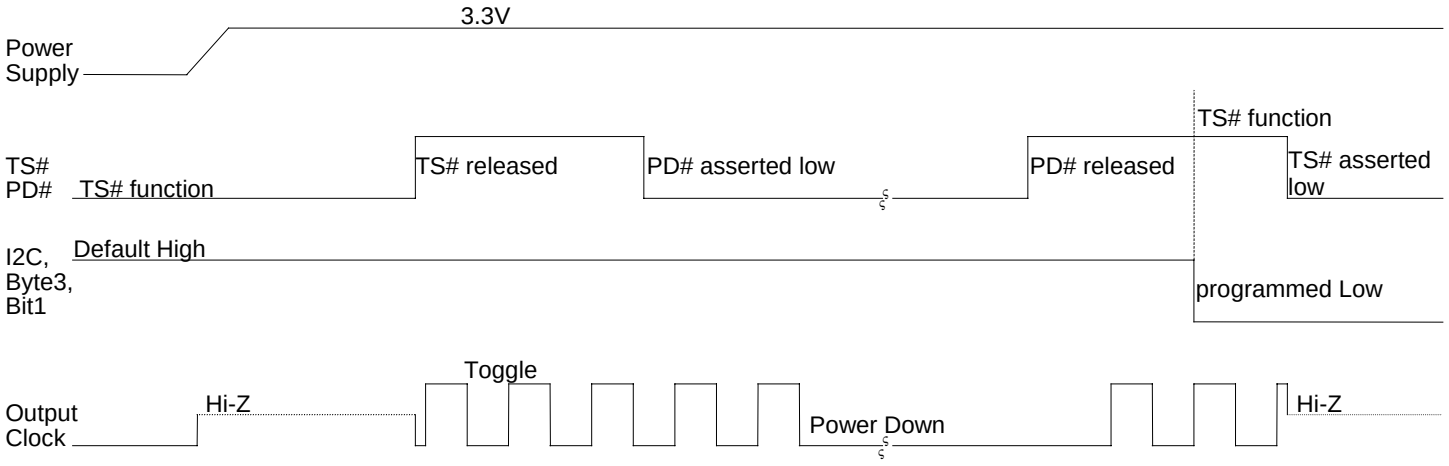


Fig.6

2-Wire SMBus Control Interface

The 2-wire control interface implements a read/write slave only interface according to SMBus specification. (See Fig. 7 below). The device can be read back by using standard SMBus command bytes. Sub addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled. 100 Kbits/second (standard mode) data transfer is supported.

2-Wire SMBus Control Interface (Cont.)

During normal data transfer, the SDATA signal only changes when the SCLK signal is low, and is stable when SCLK is high. There are two exceptions to this. A high to low transition on SDATA while SCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is an 8-bit address. The LSB address Byte = 0 in write mode.

The device will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. Data is transferred MSB first at a max rate of 100kbits/S. This device will also respond to a **D3** address which sets it in a read mode. It will not respond to any other control interface conditions, and previously set control registers are retained.

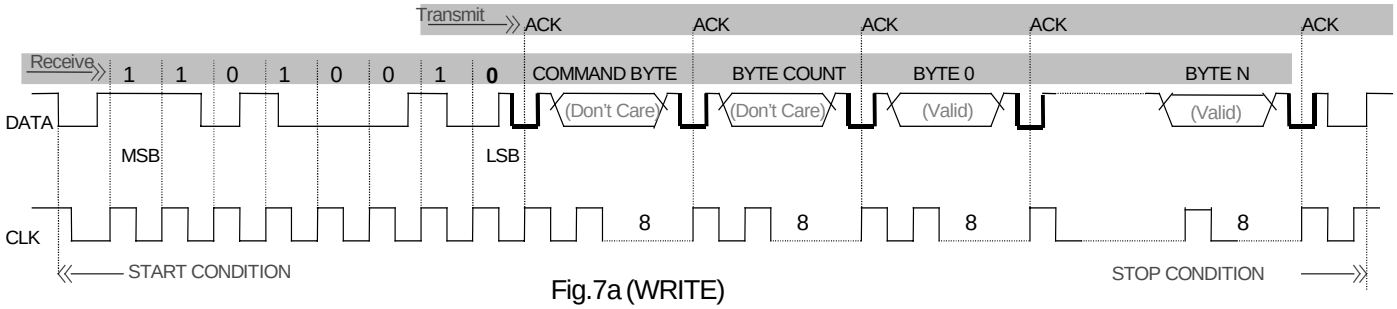


Fig.7a (WRITE)

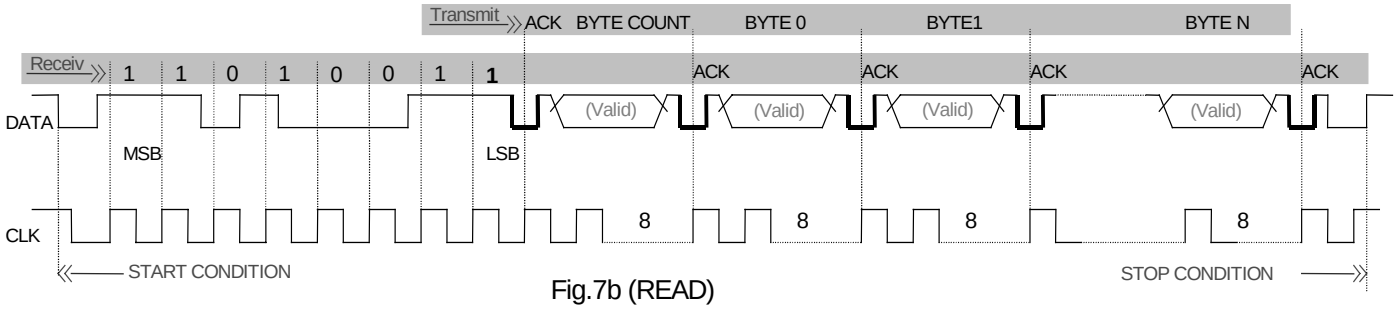


Fig.7b (READ)

Figure 7
SMBus Communications Waveforms

Serial Control Registers

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up.

Following the acknowledge of the Address Byte, two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
Although the data (bits) in these two bytes are considered "don't care"; they must be sent and will be acknowledged.

After the Command Code and the Count bytes have been acknowledged, the below described sequence (Byte 0, Byte 1, and Byte2) will be valid and acknowledged.

Byte 0: CPU Clock Register (1=Enable, 0=Disable)

Bit	@Pup	Pin#	Description
7	0	-	Sel3 selector
6	0	-	Sel2 selector
5	0	-	Sel1 selector
4	0	-	Sel0 selector
3	0	-	1 = Spread Spectrum Enabled 0 = Spread Spectrum Disabled
2	1	31	DOT
1	1	30	USB
0	0	-	High enables bit(7:4) selectors.

Byte 2: SDRAM Clock Register (1=Enable, 0=Disable)

Bit	@Pup	Pin#	Description
7	1	12	3V66-2
6	1	33	SDRAM12
5	1	34	SDRAM11
4	1	35	SDRAM10
3	1	38	SDRAM9
2	1	39	SDRAM8
1	1	15	PCI1
0	0	-	Reserved

Byte 4: PCI Clock Register (1=Enable, 0=Disable)

Bit	@Pup	Pin#	Description
7	0	-	RESERVED
6	0	-	RESERVED
5	0	-	RESERVED
4	1	22	PCI6
3	1	21	PCI5
2	1	20	PCI4
1	1	19	PCI3
0	1	16	PCI2

Byte 1: SDRAM Clock Register (1=Enable, 0=Disable)

Bit	@Pup	Pin#	Description
7	1	40	SDRAM7
6	1	41	SDRAM6
5	1	44	SDRAM5
4	1	45	SDRAM4
3	1	46	SDRAM3
2	1	47	SDRAM2
1	1	50	SDRAM1
0	1	51	SDRAM0

Byte 3: Reserved Register

Bit	@Pup	Pin#	Description
7	0	-	RESERVED
6	0	-	High puts device in TEST mode.
5	0	-	RESERVED
4	0	-	RESERVED
3	0	-	RESERVED
2	0	-	RESERVED
1	1	32	1 enables std functionality TS#/PD# 0 enables TS# only
0	0	-	0 = SDRAM runs at 100MHz 1= SDRAM runs at 133.3MHz

Byte 5: SSCG Control Register

Bit	@Pup	Pin#	Description
7	0	-	Spread Mode (0=down, 1=center)
6	0	-	Selects spread bandwidth. Ref. Table 4
5	0	-	Selects spread bandwidth. Ref. Table 4
4	0	-	Reserved
3	0	-	Reserved
2	0	-	Reserved
1	0	-	Reserved
0	0	-	Reserved

Byte 6: Dial-a-Frequency™ Register

Bit	@Pup	Pin#	Description
7	0	-	N9, MSB
6	0	-	N8
5	0	-	N7
4	0	-	N6
3	0	-	N5
2	0	-	N4
1	0	-	N3
0	0	-	N2

Byte 7: Dial-a-Frequency™ Register

Bit	@Pup	Pin#	Description
7	0	-	N1
6	0	-	N0, LSB
5	0	-	Enable SMBus N values
4	0	-	Enable SMBus R values
3	0	-	Reserved
2	0	-	Reserved
1	0	-	Reserved
0	0	-	Reserved

Byte 8: Dial-a-Frequency™ Register

Bit	@Pup	Pin#	Description
7	0	-	R7, MSB
6	0	-	R6
5	0	-	R5
4	0	-	R4
3	0	-	R3
2	0	-	R2
1	0	-	R1
0	0	-	R0, LSB

Dial-a-Frequency™ Feature

SMBus Dial-a-frequency feature is available in this device via bytes 6, 7 and 8.
These bytes allow the user to enter the N and R values that will enable them to program any CPU frequency desired following the formula:

$$Fcpu = \frac{P \times N}{R}$$

Where N and R values are programmed in binary into bytes 6 & 7 for N and byte 8 for R. See table below for min and max allowed values.

R	Min N	Max N
42	44	87
43	45	90
44	46	92
45	47	94
46	48	96
47	49	98
48	50	100
49	51	102
50	52	104
51	53	107

Dial-a-Frequency™ Feature (Cont.)

P is a large value PLL constant that depends on the last frequency selection achieved through the hardware selectors (S3, S2, S1, S0) or through the software selectors (byte0, bits7, 6, 5, 4). P value may be determined from the following table:

S(3:0)	P
0000	32005333
0001, 1100	48008000
0010, 0011, 0100, 1000, 1111	64010666
0110, 0111, 0101, 1001, 1010, 1011, 1101, 1110	96016000

Therefore, if a 145MHz (use $145x10^6$)value is desired, then we should apply 145 into equation 1, and start by choosing R to be 47 (assume the last frequency selection has the value P = 96016000):

$$145X10^6 = \frac{96016000 \times N}{47} \quad => \quad N = 70.97775371$$

Since this N number must be entered in Binary, it can only be an integer, so it must be rounded up or down. Here we can rounded it up to 71, which will give us an exact CPU frequency of:

$$Fcpu = \frac{96016000 \times N}{47} = 145.045 \text{ MHz (accuracy + 310 ppm)}$$

If the above frequency is not accurate enough, then you must choose another R value and start from the beginning. For example choose R = 49 and this will yield an N = 73.99808365, which is rounded to 74. If the 74 is applied in the formula 1, then Fcpu = 145.0038 MHz (accuracy + 26 ppm).

Other R values within the above limits may also be evaluated.

Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is a modulation technique applied here for maximum efficiency in minimizing Electro-Magnetic Interference radiation generated from repetitive digital signals mainly clocks. A clock accumulates EM energy at the center frequency it is generating. Spread Spectrum distributes this energy over a small frequency bandwidth therefore spreading the same amount of energy over a spectrum. This technique is achieved by modulating the clock down from (Fig.8A) or around the center (Fig.8B) of its resting frequency by a certain percentage (which also determines the energy distribution bandwidth). In this device, Spread Spectrum is enabled by setting SMBus byte0, bit3 = 1. The default of the device at power up keeps the Spread Spectrum disabled, it is therefore, important to have SMBus accessibility to turn-on the Spread Spectrum function. Once the Spread Spectrum is enabled, the spread bandwidth option is selected by SMBus byte 5, bits 5, 6 & 7 following tables 4A, and 4B below.

In Down Spread mode the center frequency is shifted down from its rested (non-spread) value by ½ of the total spread %. (eg.: assuming the center frequency is 100MHz in non-spread mode; when down spread of –0.5% is enabled, the center frequency shifts to 99.75MHz.).

In Center Spread mode, the Center frequency remains the same as in the non-spread mode.

Down Spread

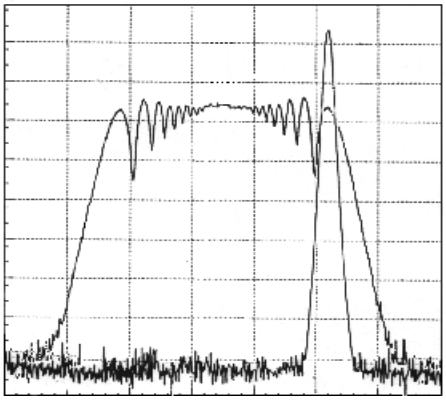


Fig.8A

Center Spread

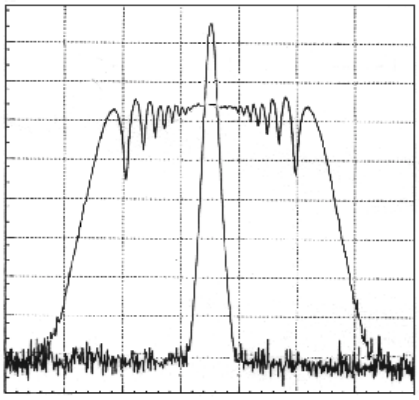


Fig.8B

Spread Spectrum Selection Tables

I²C BYTE5 Bit[7:5]	Spread %
000	- 0.5
001	- 0.7
010	N/A
011	- 0.25

Table 4A

I²C BYTE5 Bit[7:5]	Spread %
100	± 0.25
101	± 0.35
110	± 0.5
111	+/- 0.125

Table 4B

Maximum Ratings

Maximum Input Voltage Relative to VSS: VSS - 0.3V

Maximum Input Voltage Relative to VDD: VDD + 0.3V

Storage Temperature: -65ºC to + 150ºC

Operating Temperature: 0ºC to +85ºC

Maximum ESD protection 2KV

Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters (All outputs loaded per table 5, page 12)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL1	-	-	1.0	Vdc	Note 1
Input High Voltage	VIH1	2.0	-	-	Vdc	
Input Low Voltage	VIL2	-	-	1.0	Vdc	Note 2
Input High Voltage	VIH2	2.2	-	-	Vdc	
Input Low Current (@VIL = VSS)	IIL1	-66		-5	µA	For internal Pull up resistors, Notes 1,3
Input High Current (@VIL =VDD)	IIH1	-5	-	5	µA	
Input Low Current (@VIL = VSS)	IIL2	-5	-	5	µA	For internal Pull Down resistor Note 4
Input High Current (@VIL =VDD)	IIH2	5	-	66	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd3.3V	-	-	360	mA	Sel(3:0) = 0001
Dynamic Supply Current	Idd2.5V	-	-	100	mA	Sel(3:0) = 0001
Static Supply Current	Isdd	-	-	10	mA	PD# =0, Sel(3:0) = x
Input pin capacitance	Cin	-	-	5	pF	
Output pin capacitance	Cout	-	-	6	pF	
Pin inductance	Lpin	-	-	7	nH	
Crystal pin capacitance	Cxtal	32	34	38	pF	Measured from Pin to Ground. Note 5
Crystal DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Crystal Startup time	Txs	-	-	40	µS	From Stable 3.3V power supply.
VDD=VDDS = 3.3V ±5%, VDDC = VDDI = 2.5 ± 5%, TA = 0º to +70ºC						

Note1: Applicable to input signals: Sel(0:3), TS# / PD#

Note2: Applicable to Sdata, and Sclk.

Note3: Although internal pull-up resistors have a typical value of 250K, this value may vary between 200K and 500K.

Note4: Although internal pull-down resistor has a typical value of 50K, this value may vary between 30K and 70K.

Note5: Although the device will reliably interface with crystals of a 17pF – 20pF C_L range, it is optimized to interface with a typical C_L = 18pF crystal specifications.

Clock Name	Max Load (in pF)
CPU(0:1), IOAPIC, REF, USB	20
PCI(0:6), SDRAM(0:12),3V66(0:2)	30
DOT	15

Table 5.

SMBus Test Circuitry

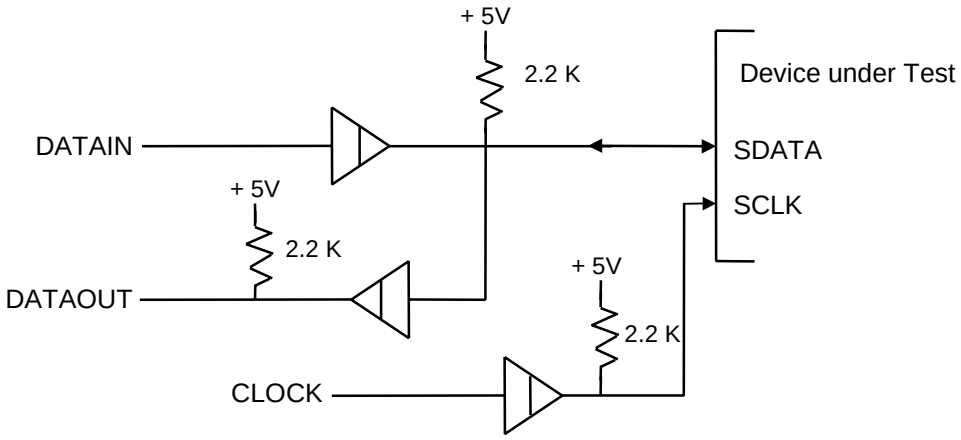
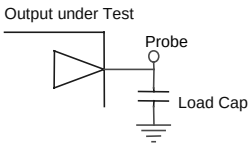


Fig.9

Note: Buffer is 7407 with VCC @ 5.0 V

Test and Measurement Condition



3.3V signals

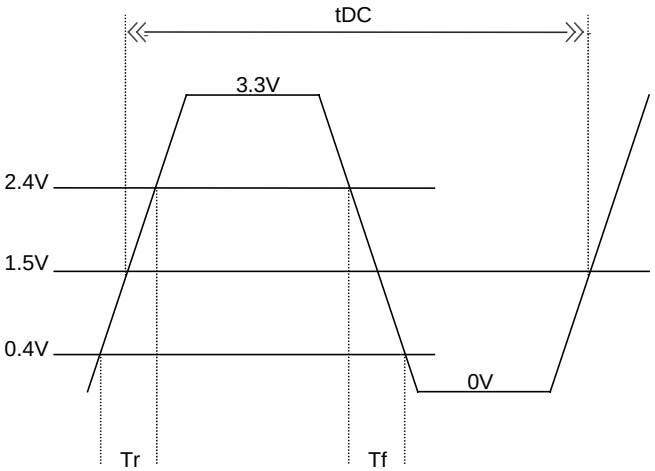


Fig.10A

2.5V signals

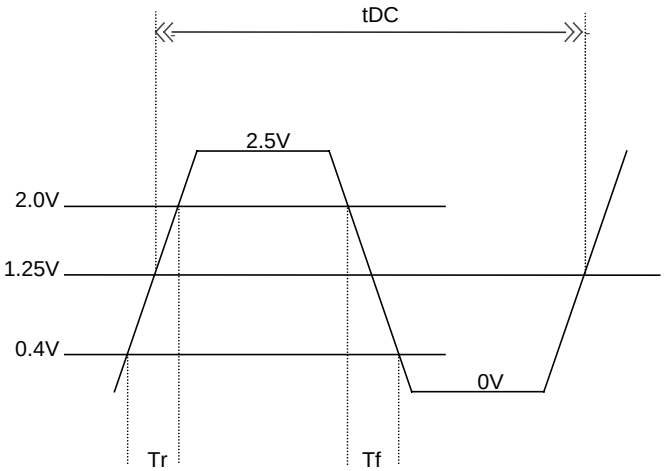


Fig.10B

AC Parameters

Symbol	Parameter	133 MHz Host		100 MHz Host		66 MHz Host		Units
		Min	Max	Min	Max	Min	Max	
TPeriod	CPU(0:1) period[1,2]	7.5	8.0	10.0	10.5	15.0	15.5	nS
THIGH	CPU(0:1) high time[6]	1.87	-	3.0	-	5.2	-	nS
TLOW	CPU(0:1) low time[7]	1.67	-	2.8	-	5.0	-	nS
Tr / Tf	CPU(0:1) rise and fall times[3]	0.4	1.6	0.4	1.6	0.4	1.6	nS
TSKEW	CPU0 to CPU Skew[2,5]	-	175	-	175	-	175	pS
TCCJ	CPU(0:1) Cycle to Cycle Jitter[2,5]	-	250	-	250	-	250	pS
TPeriod	SDRAM(0:12) period[1,2]	7.5	8.0	10.0	10.5	10.0	10.5	nS
THIGH	SDRAM(0:12) high time[16]	1.87	-	3.0	-	3.0	-	nS
TLOW	SDRAM(0:12) low time[7]	1.67	-	2.8	-	2.8	-	nS
Tr / Tf	SDRAM(0:12) rise and fall times[3]	0.4	1.6	0.4	1.6	0.4	1.6	nS
TSKEW	(Any SDRAM) to (any SDRAM) Skew[2,5]	-	250	-	250	-	250	pS
TCCJ	SDRAM(0:12) Cycle to Cycle Jitter[2,5]	-	250	-	250	-	250	pS
TPeriod	IOAPIC period[1,2]	30.0	-	30.0	-	30.0	-	nS
THIGH	IOAPIC high time[6]	12.0	-	12.0	-	12.0	-	nS
TLOW	IOAPIC low time[7]	12.0	-	12.0	-	12.0	-	nS
Tr / Tf	IOAPIC rise and fall times[3]	0.4	1.6	0.4	1.6	0.4	1.6	nS
TCCJ	IOAPIC Cycle to Cycle Jitter[2,5]	-	500	-	500	-	500	pS
TPeriod	3V66-(0:2) period[1,2]	15.0	16.0	15.0	16.0	15.0	16.0	nS
THIGH	3V66-(0:2) high time[6]	5.25	-	5.25	-	5.25	-	nS
TLOW	3V66-(0:2) low time[7]	5.05	-	5.05	-	5.05	-	nS
Tr / Tf	3V66-(0:2) rise and fall times[3]	0.5	2.0	0.5	2.0	0.5	2.0	nS
TSKEW	(Any 3V66) to (any 3V66) Skew[2,5]	-	175	-	175	-	175	pS
TCCJ	3V66-(0:2) Cycle to Cycle Jitter[2,5]	-	500	-	500	-	500	pS
TPeriod	PCI(0:6) period[1,2]	30.0	-	30.0	-	30.0	-	nS
THIGH	PCI(0:6) period[6]	12.0	-	12.0	-	12.0	-	nS
TLOW	PCI(0:6) low time[7]	12.0	-	12.0	-	12.0	-	nS
Tr / Tf	PCI(0:6) rise and fall times[3]	0.5	2.0	0.5	2.0	0.5	2.0	nS
TSKEW	(Any PCI) to (Any PCI) Skew[2,5]	-	500	-	500	-	500	pS
TCCJ	PCI(0:6) Cycle to Cycle Jitter[2,5]	-	500	-	500	-	500	pS
TPeriod	DOT & USB period (conforms to +167ppm max) [1,2]	20.8299	20.8333	20.8299	20.8333	20.829	20.833	nS
Tr / Tf	DOT & USB rise and fall times[3]	1.0	4.0	1.0	4.0	1.0	4.0	nS
TCCJ	DOT & USB Cycle to Cycle Jitter[2,5]	-	500	-	500	-	500	pS

Symbol	Parameter	133 MHz Host		100 MHz Host		66 MHz Host		Units
		Min	Max	Min	Max	Min	Max	
TPeriod	REF period[1,2]	69.8413	71.0	69.8413	71.0	69.8413	71.0	nS
Tr / Tf	REF rise and fall times[3]	1.0	4.0	1.0	4.0	1.0	4.0	nS
TCCJ	REF Cycle to Cycle Jitter[2]	-	1000	-	1000	-	1000	pS
tpZL, tpZH	Output enable delay (all outputs)[4]	1.0	10.0	1.0	10.0	1.0	10.0	nS
tstable	All clock Stabilization from power-up[8]		3		3		3	mS
Tduty	Duty Cycle for All outputs[1,3,9]	45	55	45	55	45	55	%

Note 1: This parameter is measured as an average over 1uS duration, with a crystal center frequency of 14.31818MHz
Note 2: All outputs loaded as per table 5. Probes are placed on the pins and taken at 1.5V levels for 3.3V signals and at 1.25V for 2.5V signals (figs. 10A and 10B).
Note 3: Probes are placed on the pins, and measurements are acquired between 0.4V and 2.4V for 3.3V signals and between 0.4V and 2.0V for 2.5V signals (see Fig.10A and Fig.10B)
Note 4: Measured from when TS# is switched to high (enable).
Note 5: This measurement is applicable with Spread ON or Spread OFF.
Note 6: Probes are placed on the pins, and measurements are acquired at 2.4V for 3.3V signals and at 2.0V for 2.5V signals, (see Figs. 10A & 10B)
Note 7: Probes are placed on the pins, and measurements are acquired at 0.4V.
Note 8: The time specified is measured from when all VDD's reach their respective supply rail (3.3V and 2.5V) till the frequency output is stable and operating within the specifications
Note 9: Device designed for Typical Duty Cycle of 50%.

Output Buffer Characteristics

CPU and IOAPIC

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-15	-31	-50	mA	Vout =VDDC - 0.5V (or VDDI - 0.5V)
Pull-Up Current	IOH_2	-26	-58	-101	mA	Vout = 1.2 V
Pull-Down Current	IOL_1	12	24	40	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	27	56	93	mA	Vout = 1.2 V

PCI, 3V66 and DOT

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-20	-25	-33	mA	Vout =VDD - 1.0 V
Pull-Up Current	IOH_2	-30	-54	-184	mA	Vout = 1.5 V
Pull-Down Current	IOL_1	9.4	18	38	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	28	55	148	mA	Vout = 1.5 V

USB and REF

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-12	-20	-30	mA	Vout =VDD - 1.0 V
Pull-Up Current	IOH_2	-27	-43	-92	mA	Vout = 1.5 V
Pull-Down Current	IOL_1	9	13	27	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	26	39	79	mA	Vout = 1.5 V

SDRAM

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-30	-40	-60	mA	Vout =VDDS - 1. 0 V
Pull-Up Current	IOH_2	-68	-110	-188	mA	Vout = 1.4 V
Pull-Down Current	IOL_1	23	34	53	mA	Vout = 0.4 V
Pull-Down Current	IOL_1	64	98	159	mA	Vout = 1.5 V
VDD = VDDS = 3.3V ±5%, VDDC = VDDI = 2.5±5%, TA = 0 to 70ºC						

Suggested Crystal Oscillator Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerance	TC	-	-	+/-100	PPM	Note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) Note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) Note 1
Mode	OM	-	-	-		Parallel Resonant, Note 1
Load Capacitance	CL	-	20	-	pF	The crystal's rated load. Note 1
Effective Series resistance (ESR)	R1	-	40	-	Ohms	Note 1
Power Dissipation	DL	-	-	0.10	mW	Note 1

Note1: For best performance and accurate Center frequencies of this device, It is recommended but not mandatory that the chosen crystal meets these specifications

For maximum accuracy, the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.
Budgeting Calculations
Device pin capacitance: Cxtal = 36pF
In order to meet the specification for CL = 18pF following the formula:

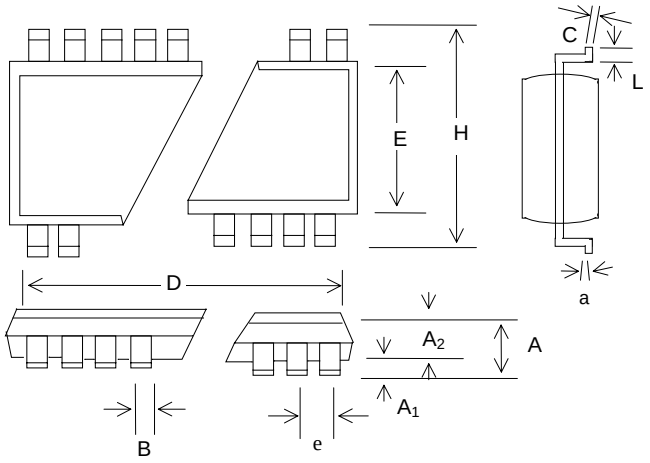
$$C_L = \frac{(C_{XINTRACE} + C_{XINDEVICE}) \times (C_{XOUTTRACE} + C_{XOUTDEVICE})}{(C_{XINTRACE} + C_{XINDEVICE}) + (C_{XOUTRACE} + C_{XOUTDEVICE})}$$

Then the board trace capacitance between Xin and the crystal should be no more than 4pF. (Same is applicable to the trace between Xout and the crystal)

In this case the total capacitance from the crystal to Xin will be 40pF. Similarly the total capacitance between the crystal and Xout will be 36pF. Hence using the above formula:

$$C_L = \frac{40 \times 40}{40 + 40} = 20 \text{ pF}$$

Package Drawing and Dimensions



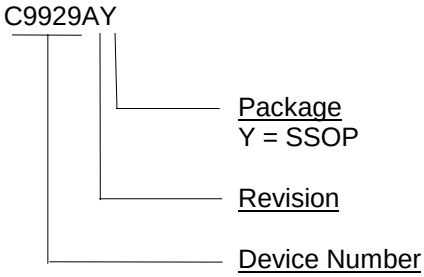
56 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.20	0.31	0.41
A2	0.088	0.090	0.092	2.24	2.29	2.34
B	0.008	0.010	0.0135	0.203	0.254	0.343
C	0.005	-	0.010	0.127	-	0.254
D	.720	.725	.730	18.29	18.42	18.54
E	0.292	0.296	0.299	7.39	7.49	7.60
e	0.025 BSC			0.635 BSC		
H	0.395	0.406	0.420	10.03	10.31	10.67
L	0.020	0.032	0.040	0.51	0.81	1.02
a	0°	5°	8°	0°	5°	8°

Ordering Information

Part Number	Package Type	Production Flow
C9929AY	56 PIN SSOP	Commercial, 0° to 70°C

Marking: Example: Cypress
C9929AY
Date Code, Lot #



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Document Title: C9929 Low EMI Clock Generator for Intel® 133MHz/3DIMM Chipset Systems **Document Number:** 38-07071				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107107	06/11/01	IKA	Convert from IMI to Cypress