Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (16K x 4-BIT)

IDT7188S
IDT7188L

FEATURES:

- High-speed (equal access and cycle times)
  - — Military: 20/25/35/45/55/70/85ns (max.)
  - — Commercial: 15/20/25/35ns (max.)
- Low power consumption
- Battery backup operation — 2V data retention (L version only)
- Available in high-density industry standard 22-pin, 300 mil ceramic and plastic DIP, 24-pin SOJ and CERPACK
- Produced with advanced CMOS technology
- Inputs/outputs TTL-compatible
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

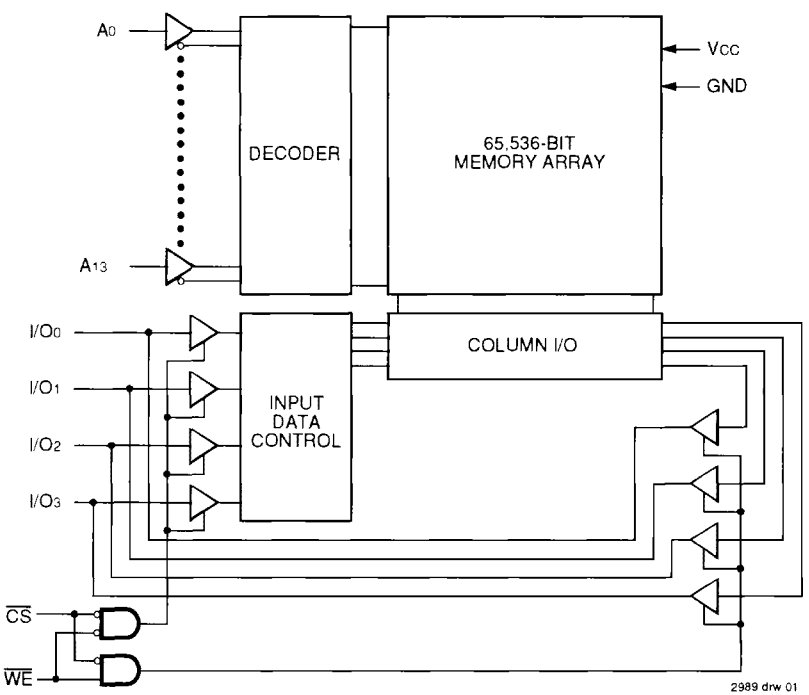
The IDT7188 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology — CMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

Access times as fast as 15ns are available. The IDT7188 offers a reduced power standby mode, I_{SB1}, which is activated when $\overline{CS}$ goes high. This capability significantly decreases power while enhancing system reliability. The low-power version (L) version also offers a battery backup data retention capability where the circuit typically consumes only 30µW operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5V supply. The IDT7188 is packaged in 22-pin, 300 mil ceramic and plastic DIPs, 24-pin SOJs and CERPACKs, providing excellent board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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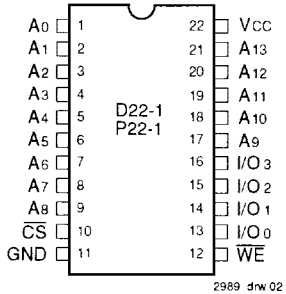
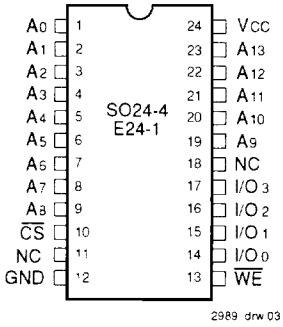
PIN CONFIGURATIONS



DIP
TOP VIEW



CERPACK/SOJ
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0–A13	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
I/O0-3	Data Input/Output
VCC	Power
GND	Ground

2989 tb 01

TRUTH TABLE[1]

Mode	$\overline{CS}$	$\overline{WE}$	I/O	Power
Standby	H	X	High Z	Standby
Read	L	H	DOUT	Active
Write	L	L	DIN	Active

NOTE:
1. H = VIH, L = VIL, X = don't care.

2989 tbl C2

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE:
2989 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz, VCC = 0v))

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	pF
COUT	Output Capacitance	VOUT = 0V	6	pF

NOTE:
2989 tb 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE:
2989 tbl 05

1. VIL (min.) = -3.0V for pulse width less than 20ns,once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2989 tbl 06

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT7188S Min.	IDT7188S Max.	IDT7188L Min.	IDT7188L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.			0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2989 tbl 07

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7188S15 7188L15 Com'l.	7188S15 7188L15 Mil.	7188S20 7188L20 Com'l.	7188S20 7188L20 Mil.	7188S25 7188L25 Com'l.	7188S25 7188L25 Mil.	7188S35 7188L35 Com'l.	7188S35 7188L35 Mil.	7188S45 7188L45 Com'l.	7188S45 7188L45 Mil.	7188S55/70 7188L55/70 Com'l.	7188S55/70 7188L55/70 Mil.	7188S85 7188L85 Com'l.	7188S85 7188L85 Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0(2)	S	100	—	100	105	100	105	100	105	—	105	—	105	—	105	mA
		L	75	—	70	80	70	80	70	80	—	80	—	80	—	80	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = f_{MAX}(2)	S	135	—	125	160	125	155	125	140	—	140	—	140	—	140	mA
		L	125	—	115	130	105	120	105	115	—	110	—	110	—	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	S	60	—	55	70	50	60	45	50	—	50	—	50	—	50	mA
		L	45	—	40	50	35	40	30	40	—	35	—	35	—	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC}=Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0(2)	S	20	—	15	25	15	20	15	20	—	20	—	20	—	20	mA
		L	1.5	—	0.5	1.5	0.5	1.5	0.5	1.5	—	1.5	—	1.5	—	1.5	

NOTES:

2989 tbl 06

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

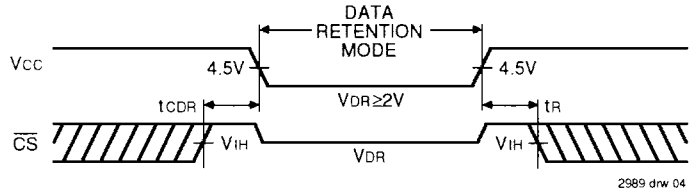
(L Version Only) $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Condition		Min.	Typ.[1] Vcc @ 2.0v	Typ.[1] Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	Vcc for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL.	—	10	15	600	900	µA
			COM'L.	—	10	15	150	225	
t_{CDR}[3]	Chip Deselect to Data Retention Time	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		0	—	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns
$\|I_{LI}\|$[3]	Input Leakage Current			—	—	—	2	2	µA

NOTES:
1. $T_A = +25°C$.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization but is not production tested.

2989 tbl 09

LOW Vcc DATA RETENTION WAVEFORM

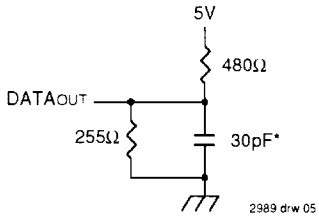


2989 drw 04

AC TEST CONDITIONS

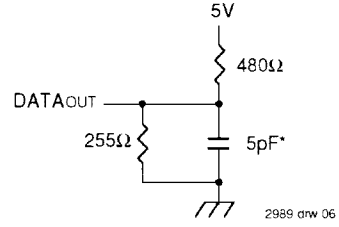
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2989 tbl 10



2989 drw 05

Figure 1. AC Test Load



2989 drw 06

Figure 2. AC Test Load (for t_{HZ}, t_{LZ}, t_{WZ}, t_{OHZ} and t_{OW})

*Includes scope and jig capacitances

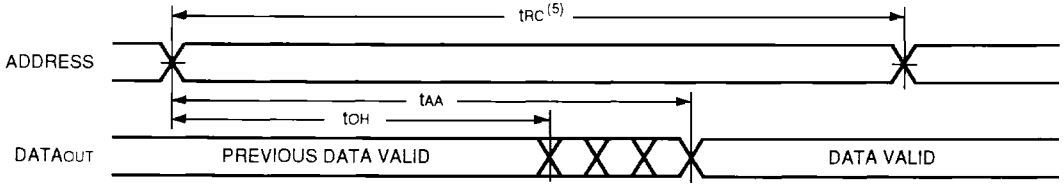
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7188S15[1] 7188L15[1] Min.	Max.	7188S20 7188L20 Min.	Max.	7188S25 7188L25 Min.	Max.	7188S35/45 7188L35/45 Min.	Max.	7188S55/70[2] 7188L55/70[2] Min.	Max.	7188S85[2] 7188L85[2] Min.	Max.	Unit
Read Cycle														
tRC	Read Cycle Time	15	—	20	—	25	—	35/45	—	55/70	—	85	—	ns
tAA	Address Access Time	—	15	—	20	—	25	—	35/45	—	55/70	—	85	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	—	35/45	—	55/70	—	85	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
tLZ	Output Selection to Output in Low Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns
tHZ	Chip Deselect to Output in High Z[3]	—	7	—	8	—	10	—	14	—	20/25	—	30	ns
tPU	Chip Select to Power Up Time[3]	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power Down Time[3]	—	15	—	20	—	25	—	35/45	—	55/70	—	85	ns

NOTES:
2989 tbl 11

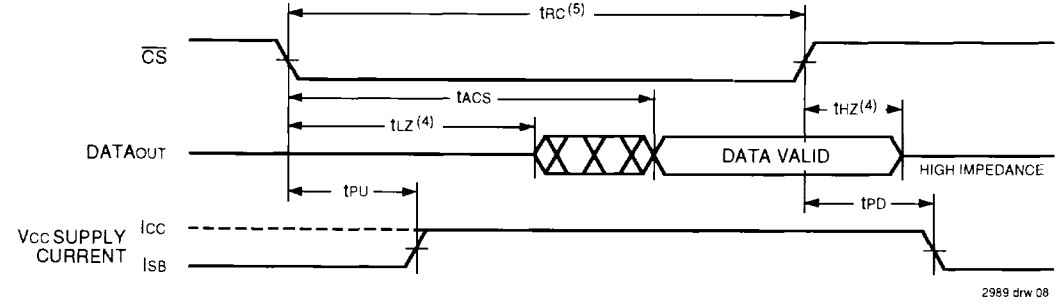
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed by device characterization but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1, 2]



2989 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2[1, 3]



2989 drw 08

NOTES:
1. WE is high for read cycle.
2. CS is low for READ cycle.
3. Address valid prior to or coincident with CS transition low.
4. Transition is measured ±200mV from steady state voltage.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

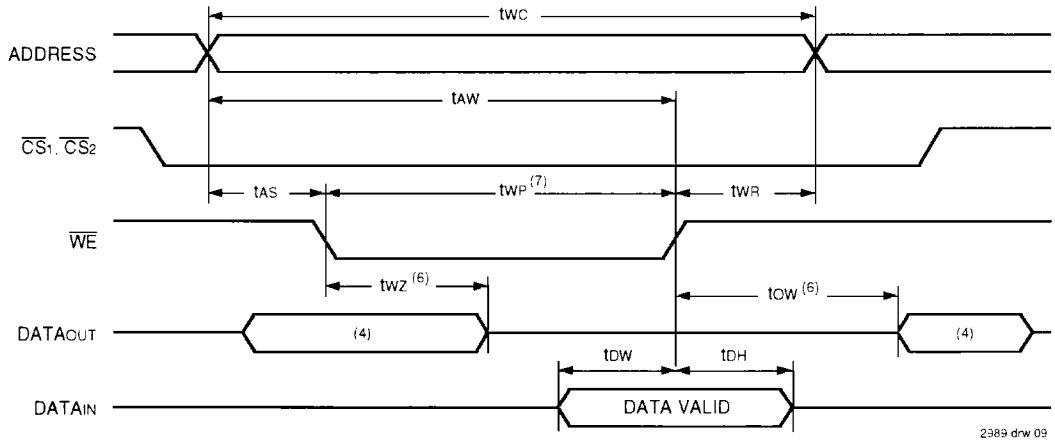
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7188S15[1] 7188L15[1]		7188S20 7188L20		7188S25 7188L25		7188S35/45[2] 7188L35/45[2]		7188S55/70[2] 7188L55/70[2]		7188S85[2] 7188L85[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle														
tWC	Write Cycle Time	14	—	17	—	20	—	30/40	—	50/60	—	75	—	ns
tCW	Chip Select to End of Write	14	—	17	—	20	—	25/35	—	50/60	—	75	—	ns
tAW	Address Valid to End of Write	14	—	17	—	20	—	25/35	—	50/60	—	75	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	14	—	17	—	20	—	25/35	—	50/60	—	75	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	10	—	10	—	13	—	15/20	—	25/30	—	35	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High Z[3]	—	5	—	6	—	7	—	10/15	—	25/30	—	40	ns
tOW	Output Active from End of Write[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns

NOTES:
2989 tbl 12

1. 0 to +70°C temperature range only.
2. −55°C to +125°C temperature range only.
3. This parameter is guaranteed by device characterization.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3]

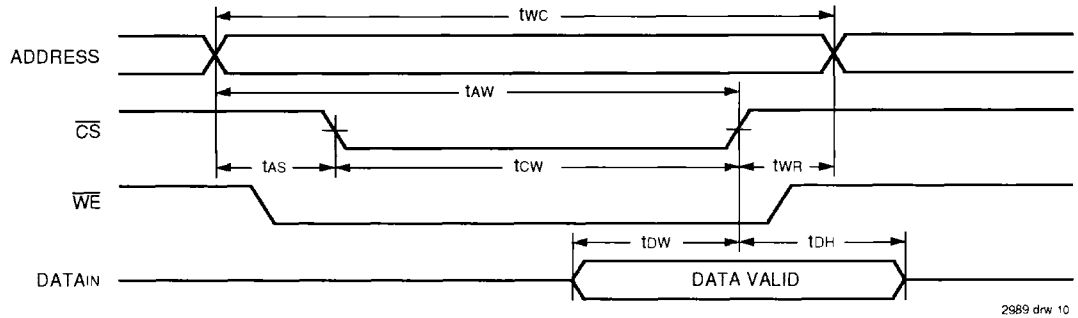


2989 drw 09

NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals should not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high-impedance state.
6. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,3,5)



NOTES:
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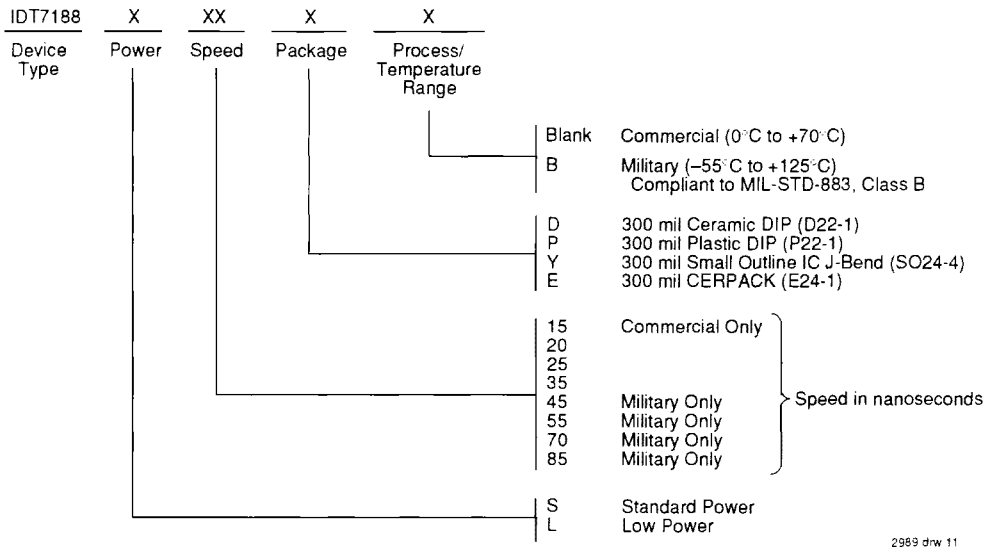
ORDERING INFORMATION



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