HI-REL DATA SHEET

HM 65791

16 k x 4
HIGH SPEED CMOS SRAM
SEPARATE I/O and TRANSPARENT WRITE

FEATURES

- **FAST ACCESS TIME : 25/35/45/55 ns**
- **LOW POWER CONSUMPTION**
  ACTIVE : 267 mW (typ)
  STANDBY : 75 mW (typ)
- **WIDE TEMPERATURE RANGE : - 55 TO + 125°C**
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**
- **SEPARATE INPUTS/OUTPUTS**
- **TRANSPARENT WRITE**
- **OUTPUT ENABLE**

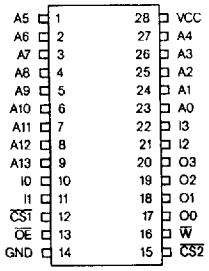
DESCRIPTION

The HM 65791 is a high speed CMOS static RAM organized as 16384 x 4 bits. It is manufactured using MHS's high performance CMOS technology.
Access times as fast as 25 ns are available with maximum power consumption of only 385 mW.
The HM 65791 features fully static operation requiring no external clocks or timing strobes.The automatic power-down feature reduces the power consumption by 60 % when the circuit is deselected.
Easy memory expansion is provided by an active low chip select ($\overline{CS1}$, $\overline{CS2}$), an active low output enable ($\overline{OE}$) and three state drivers.
All inputs and outputs of the HM 65791 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65791 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

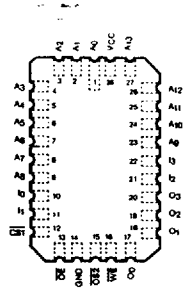
PACKAGES

Ceramic 300 mils, 28 pins, DIL. LCC, 28 pins.

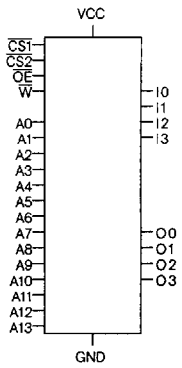
Pinout DIL 28 pins (top view)



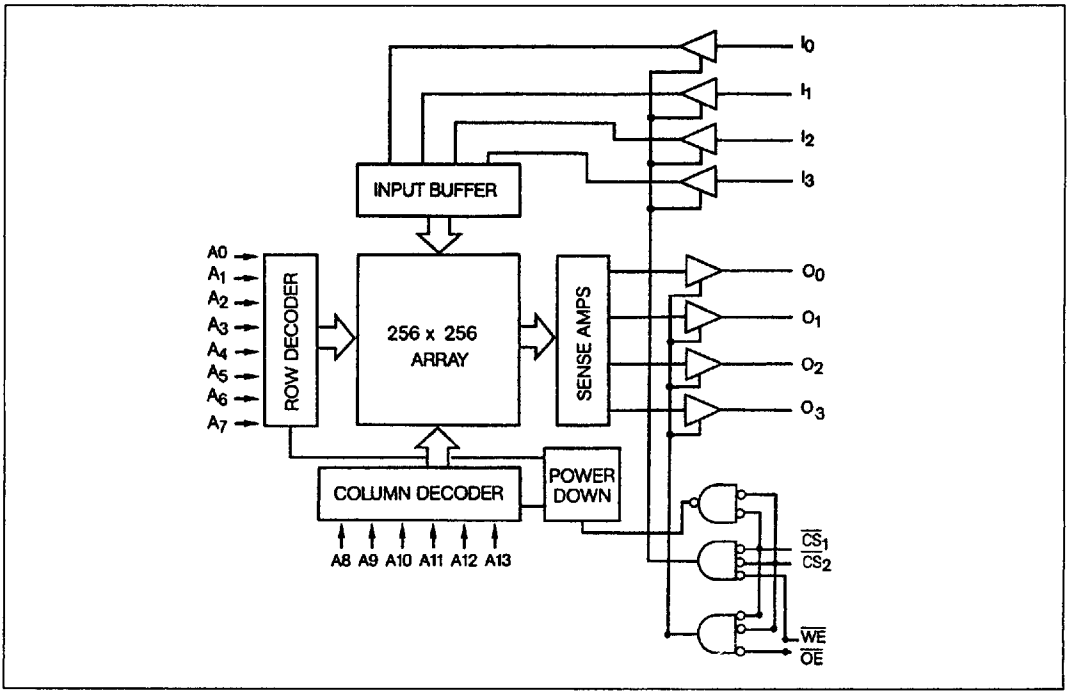
Pinout LCC 28 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



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PIN NAMES

A0-A13	: Address inputs	$\overline{CS1}$- $\overline{CS2}$	: Chip-Select
I0-I3	: Inputs	$\overline{OE}$	: Output enable
O0-O3	: Outputs	$\overline{W}$	: Write Enable
VCC	: Power	GND	: Ground

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	Z	Z	Deselect
L	L	H	Z	Valid	Read
L	H	L	Valid	Valid	Write
L	L	L	Valid	Valid	Write

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : - 0.5 V to + 7.0 V
DC input voltage : - 3.0 V to 7.0 V
DC output voltage in high Z state : - 0.5 V to + 7.0 V
Storage temperature : - 65°C to + 150°C

Output current into outputs (low) : 20 mA
Electro static discharge voltage : > 2001 V
(MIL STD 883C method 3015)

OPERATING RANGE	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	5 V ± 10 %	- 55°C to + 125°C
Industrial	5 V ± 10 %	- 40°C to + 85°C

ELECTRICAL CHARACTERISTICS
DC PARAMETERS : MIL STD 883C FOR GROUP A (Subgroups 1, 2, 3, 4)

Parameter	Description	65791 H	65791 K	65791 M	65791 N	Unit	Value	Note 6
ICCSB (1)	Standby supply current	20	20	20	20	mA	Max	M
ICCSB (1a)	Standby supply current	40	30	30	30	mA	Max	M
ICCOP (2)	Operating supply current	100	100	100	100	mA	Max	M
II (3)	Input leakage current	± 10	± 10	± 10	± 10	µA	Max	M
IOZ (3)	Output leakage current	± 10	± 10	± 10	± 10	µA	Max	M
VIL (4)	Input low voltage	0.8	0.8	0.8	0.8	V	Max	T
VIH (4)	Input high voltage	2.2	2.2	2.2	2.2	V	Min	T
VOL (5)	Output low voltage	0.4	0.4	0.4	0.4	V	Max	M
VOH (5)	Output high voltage	2.4	2.4	2.4	2.4	V	Min	M
C IN	Input capacitance	5	5	5	5	pF	Max	G
C OUT	Output capacitance	7	7	7	7	pF	Max	G

Notes : 1. $\overline{CS}$ > = Vcc - 0.3V , VIN > Vcc - 0.3V or < = 0.3V
1a. $\overline{CS}$ ≥ VIH Max Vcc, Min Duty cycle = 100 %
2. Vcc max, Output current = 0 mA, Minimum cycle
3. Vcc max, Vin = Gnd to Vcc
4. VIL min = - 3.0V, VIH max = Vcc
5. Vcc Min, IOL = 8 mA, IOH = - 4 mA
6. Including open/short test or inputs clamp voltage.
G - Guaranted - Not tested : Parameter measured at design validation and at any design change.
M - Measured : Parameter measured and data-log capability.
T - Tested : Parameter verification during testing.

AC TEST LOADS AND WAVEFORMS

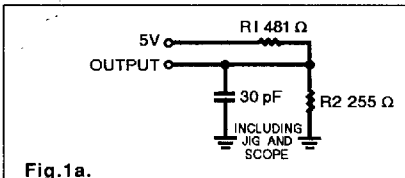


Fig.1a.

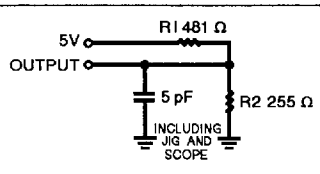
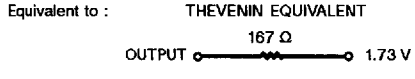


Fig.1b



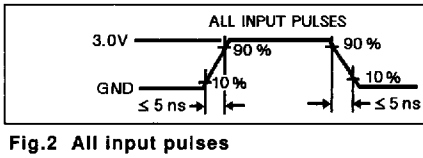


Fig.2 All input pulses

AC PARAMETERS : MIL STD 883C FOR GROUP A (SUBGROUPS 7, 8, 9, 10, 11)

Conditions :

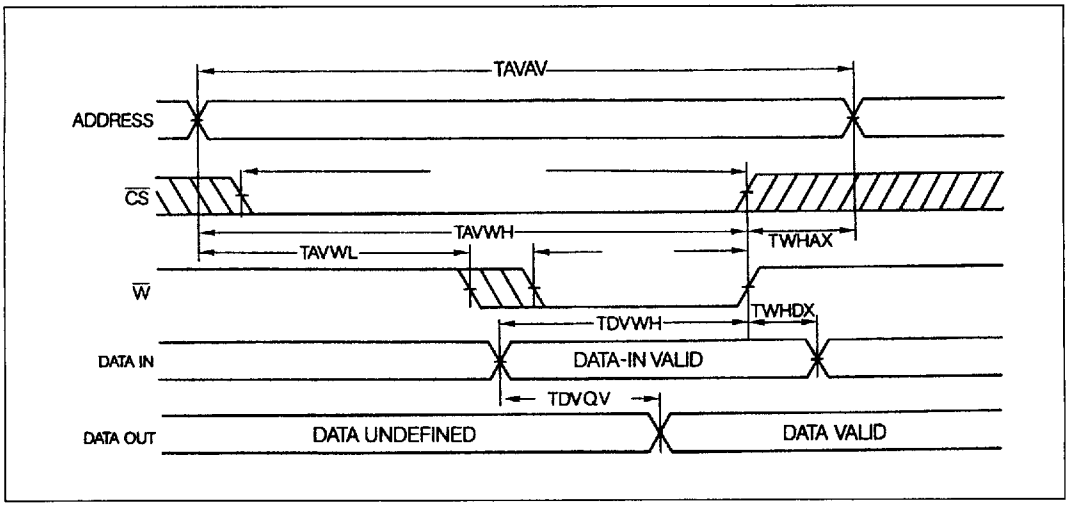
VCC	5V ± 10 %
Input pulse levels	Gnd to 3.0V
Input rise	5 ns
Input timing reference levels	1.5V
Output loading IOL / IOH	+ 30 pF
Operating temperature	- 55°C to + 125°C

WRITE CYCLE : Military specification

SYMBOL	PARAMETER (8)	65791 H	65791 K	65791 M	65791 N	UNIT	VALUE
TAVAV	Write cycle time	20	25	40	50	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	20	25	30	40	ns	min
TDVWH	Data set-up time	10	15	15	20	ns	min
TELWH	$\overline{CS}$ low to write end	20	25	30	40	ns	min
TWLQZ (7)	Write low to high Z	7	10	15	20	ns	max
TWLWH	Write pulse width	15	20	20	25	ns	min
TWHAX	Address hold to end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWLQV	$\overline{W}$ low to data valid	25	30	35	40	ns	max
TDVQV	Data valid to output valid	20	30	35	45	ns	max

Notes : 7. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. All parameters tested only.
All parameters are screened during full speed functional test.
For subgroups 7 and 8 (functional test).
Tested at 1 MHz with VIL = 0V and VIH = 3V.
HM 65791 is verified with differents patterns unit for basic function, latch-up, maximum rating, data-retention.

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



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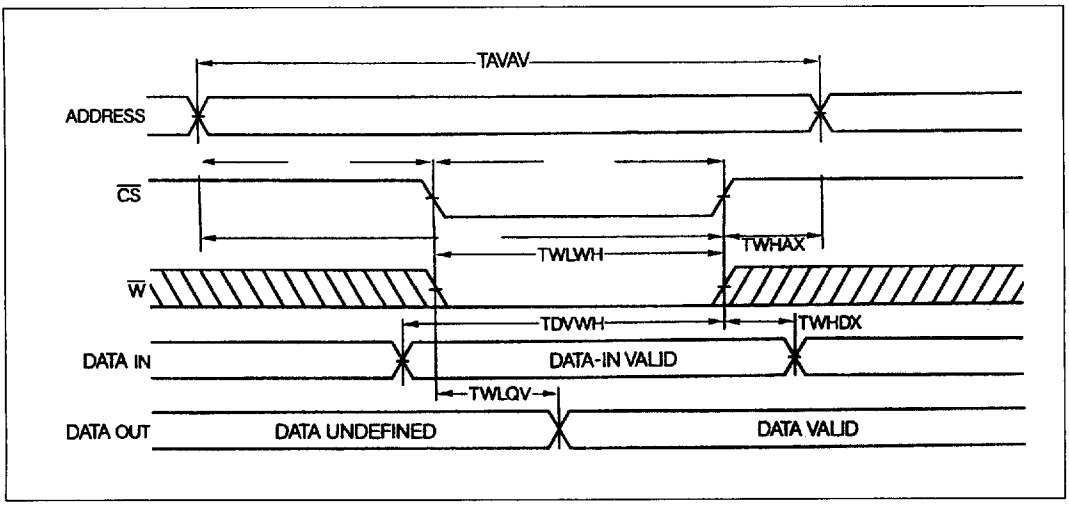
WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED)



READ CYCLE :

SYMBOL	PARAMETER (8)	65791 H	65791 K	65791 M	65791 N	UNIT	VALUE
TAVAV	Read cycle time	25	35	45	55	ns	min
TAVQW	Address access time	25	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	3	ns	min
TELQV	Chip-select access time	25	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	10	12	15	15	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	20	25	25	ns	max
TGLQV	Output enable access time	12	15	20	25	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	10	12	15	15	ns	max

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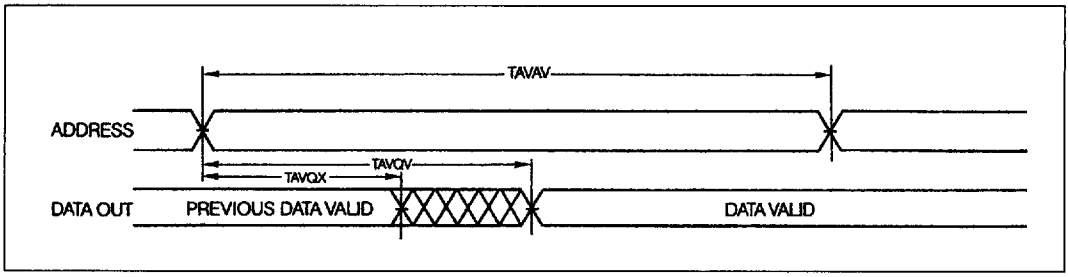
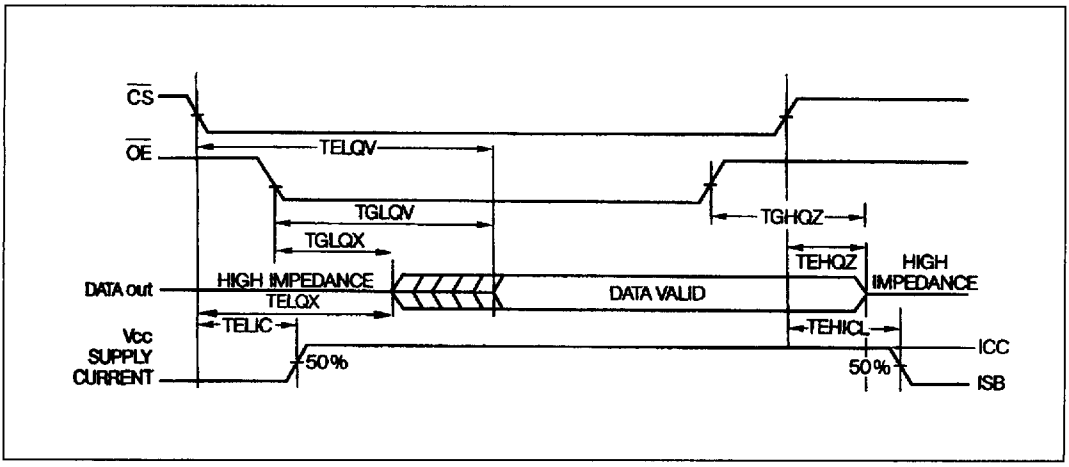
READ CYCLE nb 1



READ CYCLE nb 2



ORDERING INFORMATION

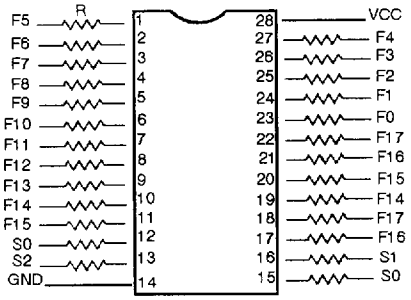
PROCESS FLOW

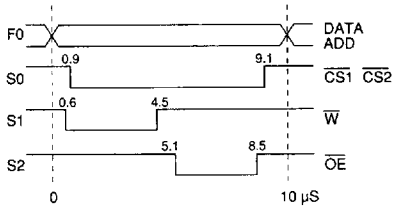
Package	Device Type	Grade	Type	Level/Class	Lot Acceptance Level
HM1	65791	K	S	B	2 *

- **Package**
  - 1 - Ceramic DIL 24
  - 4 - LCC 28 pins
  - 0 - Chip form
  - W - Wafer form
  - * only SCC 9000 specification
- **Device Type**
  - 16K x 4 high speed Static RAM with separate I/O and transparent write
- **Grade**
  - H : 25 ns
  - K : 35 ns
  - M : 45 ns
  - N : 55 ns
- **Type**
  - - 9 : Industrial
  - - 2 : Military
  - - 8 : Military Program
  - M : MIL STD 883C
  - S : SCC 9000
  - C : CECC 90000
  - D : Dice HI-REL
- **Level/Class**
  - Blank : MHS test method
  - B Class : MIL STD 883C
  - B Level : SCC 9000
  - C Level : SCC 9000
  - B Level : CECC 90000
- **Lot Acceptance Level**
  - 1 : LAT 1
  - 2 : LAT 2
  - 3 : LAT 3

	PACKAGED PRODUCT						DIE FORM	
SUFFIX →	- 2	- 8	MB	CB	SB	SC	- 2	DB
DESCRIPTION →	- 55°C TO + 125°C	MILITARY PROGRAM	MIL-STD 883C CLASS B	COMPLIANT WITH CECC 90000 LEVEL B	COMPLIANT WITH SCC 9000 LEVEL B	COMPLIANT WITH SCC 9000 LEVEL C	25°C AND 125°C PROBE	HI-REL FLOW

BURN IN SCHEMATICS





R = 1KΩ per pin
F0 = 50KHz ± 20 %
Fn = 1/2F n-1

S0, S1, S2, S3 : programmable signals for write/read cycle
VCC = 5.5 V

Drawings for reference only.

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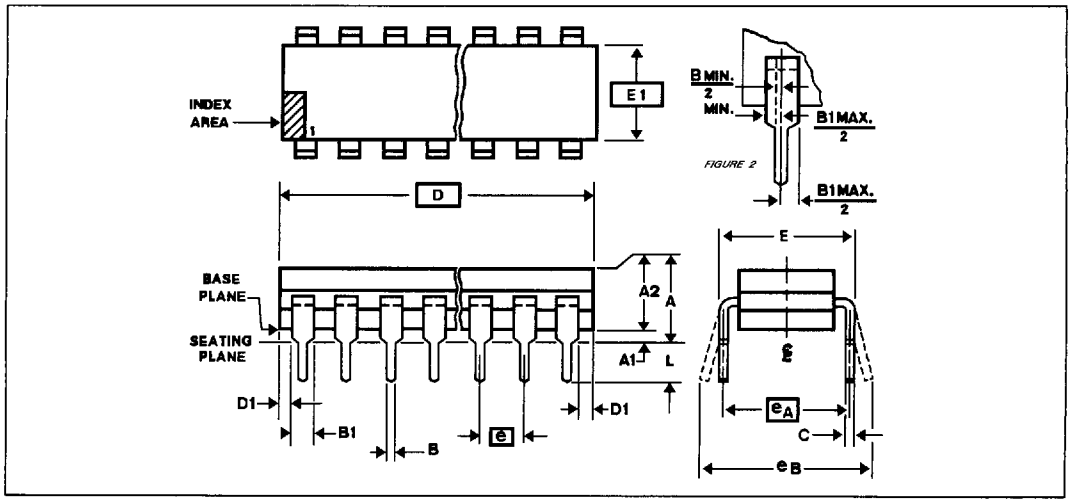
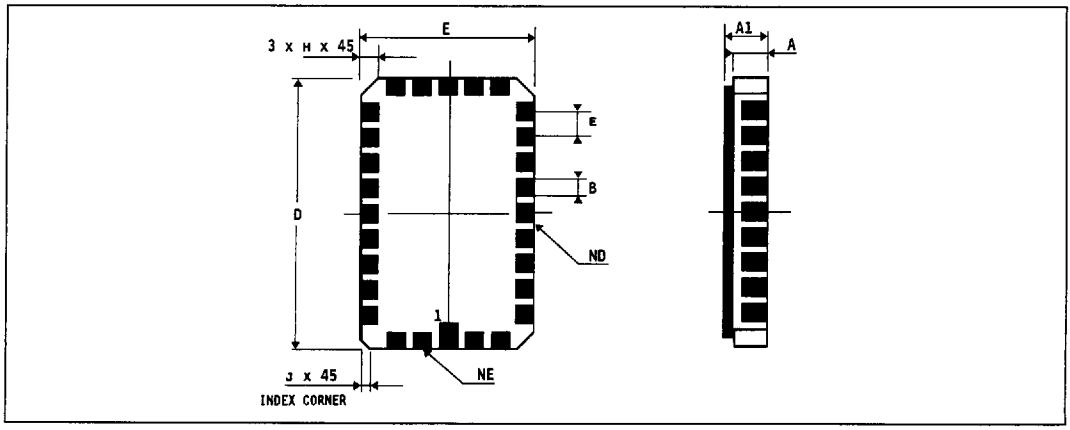
PACKAGE OUTLINES



28 PINS CERDIP .300

		A	A1	A2	B	B1	C	D	D1	E	E1	e	eA	eB	L
MM	MIN	—	0.38	2.92	0.36	1.14	0.20	36.58	0.13	7.62	6.10	2.54	7.62	—	3.05
	MAX	5.84	—	4.95	0.58	1.78	0.38	37.50	—	8.25	7.87	BSC	BSC	11.43	5.08
INCHES	MIN	—	.015	.115	.014	.045	.008	1.440	.005	.300	.240	.100	.300	—	.125
	MAX	.230	—	.195	.023	.070	.015	1.476	—	.325	.310	BSC	BSC	.450	.200



28 LDS .050 CENTER LEADLESS RECTANGULAR CHIP CARRIER

		A	A1	B	D	E	e	h	j	ND	NE
MM	MIN	1.37	1.62	0.56	13.81	8.74	1.27	0.64	0.38	9	5
	MAX	1.65	2.00	0.71	14.22	9.14	BSC	Ref	Ref		
INCHES	MIN	.054	.064	.022	.544	.344	.050	0.25	.015	9	5
	MAX	.065	.079	.028	.560	.360	BSC	Ref	Ref		