



FTG for Integrated Core Logic with 133-MHz FSB

Features

- Maximized EMI suppression using Cypress's Spread Spectrum technology
- Two copies of CPU clock at 66/100/133 MHz
- Thirteen copies of 100-MHz SDRAM clocks
- Two copies of PCI clock
- One copy of APIC clock at 33 MHz, synchronous to CPU clock
- Two copies of 48-MHz clock (non-spread spectrum) optimized for USB reference input and video dot clock
- Three copies of 3V 66-MHz fixed clock
- One copy of 14.31818-MHz reference clock
- Power down control
- SMBus interface for turning off unused clocks

Key Specifications

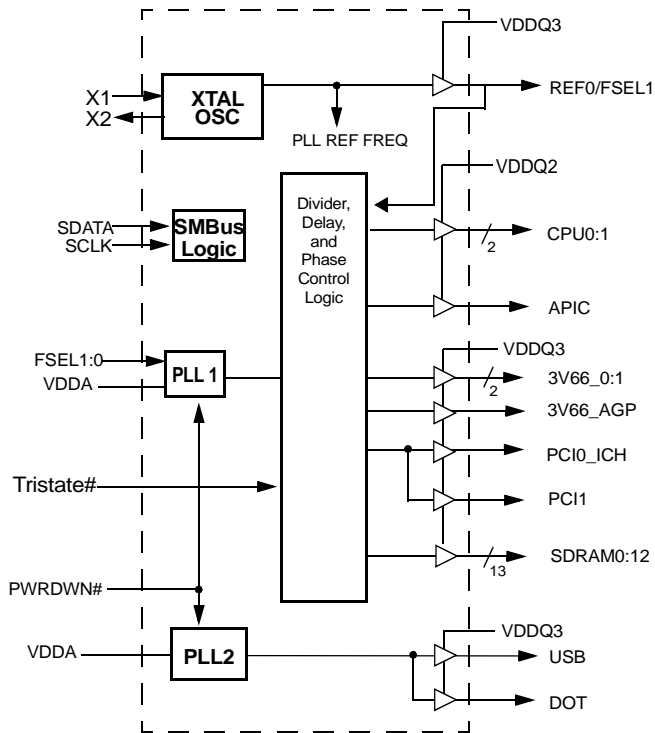
CPU, SDRAM Outputs Cycle-to-Cycle Jitter:..... 250 ps  
 APIC, 48-MHz, 3V66, PCI Outputs  
 Cycle-to-Cycle Jitter:..... 500 ps  
 APIC, SDRAM Output Skew:..... 250 ps

CPU, 3V66 Output Skew:..... 175 ps  
 PCI Output Skew:..... 500 ps  
 CPU to SDRAM Skew (@ 133 MHz):..... ±0.5 ns  
 CPU to SDRAM Skew (@ 100 MHz):..... 4.5 to 5.5 ns  
 CPU to 3V66 Skew (@ 66 MHz): ..... 7.0 to 8.0 ns  
 3V66 to PCI Skew (3V66 lead):..... 1.5 to 3.5 ns  
 PCI to APIC Skew: ..... ±0.5 ns

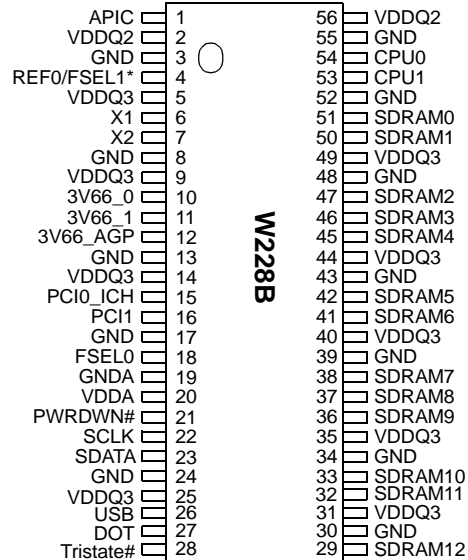
Table 1. Pin Selectable Functions

Tristate#	FSEL0	FSEL1	CPU	SDRAM
0	0	x	Three-state	Three-state
0	1	x	Test	Test
1	0	0	66 MHz	100 MHz
1	1	0	100 MHz	100 MHz
1	0	1	133 MHz	133 MHz
1	1	1	133 MHz	100 MHz

Block Diagram



Pin Configuration<sup>[1]</sup>



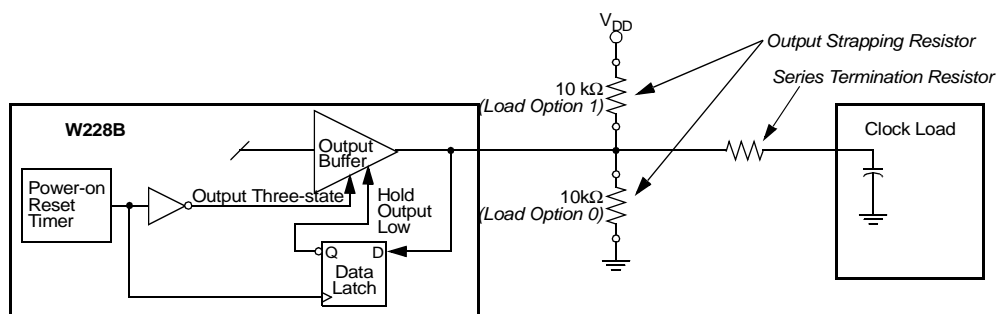
Note:

1. Internal pull-down resistors present on input marked with \*.  
 Design should not solely rely on internal pull-down resistor to set I/O pin LOW.

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**Pin Definitions**

Pin Name	Pin No.	Pin Type	Pin Description
REF0/FSEL1	4	I/O	<b>Reference Clock:</b> 3.3V 14.318-MHz clock output. This pin also serves as a strap option for CPU frequency selection. See <i>Table 1</i> for detailed descriptions.
X1	6	I	<b>Crystal Input:</b> This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.
X2	7	O	<b>Crystal Output:</b> A connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
PCI0_ICH, PCI1	15, 16	O	<b>PCI Clock 0 through 1:</b> 3.3V 33-MHz PCI clock outputs. PCI1 can be individually turned off via SMBus interface.
3V66_0:2, 3V66_AGP	10, 11, 12	O	<b>66-MHz Clock Output:</b> 3.3V fixed 66-MHz clock.
USB	26	O	<b>USB Clock Output:</b> 3.3V fixed 48-MHz, non-spread spectrum USB clock output.
DOT	27	O	<b>Dot Clock Output:</b> 3.3V 48-MHz, non-spread spectrum signal.
Tristate#, FSEL0	28, 18	I	<b>Clock Function Selection pins:</b> LVTTTL-compatible input to select device functions. See <i>Table 1</i> for detailed descriptions.
PWRDWN#	21	I	<b>Power-Down Control:</b> LVTTTL-compatible asynchronous input that places the device in power-down mode when held LOW.
CPU0:1	54, 53	O	<b>CPU Clock Outputs:</b> Clock outputs for the host bus interface and integrated test port. Output frequencies run at 66 MHz, 100 MHz, or 133 MHz depending on the configuration of SEL0:1 and SEL133. Voltage swing set by VDDQ2.
SDRAM0:12	51, 50, 47, 46, 45, 42, 41, 38, 37, 36, 33, 32, 29	O	<b>SDRAM Clock Outputs:</b> 3.3V outputs running at 100 MHz. SDRAM0:12 can be individually turned off via SMBus interface.
APIC	1	O	<b>Synchronous APIC Clock Outputs:</b> Clock outputs running synchronous with the PCI clock outputs (33 MHz). Voltage swing set by VDDQ2.
SDATA	23	I/O	Data pin for SMBus circuitry.
SCLK	22	I	Clock pin for SMBus circuitry.
VDDQ3	5, 9, 14, 25, 31, 35, 40, 44, 49	P	<b>3.3V Power Connection:</b> Power supply for SDRAM output buffers, PCI output buffers, 3V66 output buffers, reference output buffers, and 48-MHz output buffers. Connect to 3.3V.
VDDA	20	P	<b>3.3V Power Connection:</b> Power supply for core logic, PLL circuitry. Connect to 3.3V.
VDDQ2	2, 56	P	<b>2.5V Power Connection:</b> Power supply for IOAPIC and CPU output buffers. Connect to 2.5V or 3.3V.
GND	3, 8, 13, 17, 24, 30, 34, 39, 43, 48, 52, 55	G	<b>Ground Connections:</b> Connect all ground pins to the common system ground plane.
GNDA	19	G	<b>Ground Connections:</b> Connect all ground pins to the common system ground plane.



**Figure 1. Input Logic Selection Through Resistor Load Option**

## Overview

The W228B is a highly integrated frequency timing generator, supplying all the required clock sources for an Intel® architecture platform using graphics integrated core logic.

## Functional Description

### I/O Pin Operation

REF0/FSEL1 is a dual-purpose I/O pin. Upon power-up the pin acts as a logic input for FSEL1 selection (see *Table 1* and *Table 2*). If the pin is strapped to a HIGH state externally, CPU will be strapped LOW. CPU clock outputs will be determined by the status of SEL0:1 input pins. An external 10-kΩ strapping

resistor should be used. *Figure 1* shows a suggested method for strapping resistor connections.

After 2 ms, the pin becomes an output. Assuming the power supply has stabilized by then, the specified output frequency is delivered on the pins. If the power supply has not yet reached full value, output frequency initially may be below target but will increase to target once supply voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.

### Pin Selectable Functions

*Table 2* outlines the device functions selectable through Tristate# and FSEL0:1. Specific outputs available at each pin are detailed in *Table 2* below.

**Table 2. CK Whitney Truth Table**

Tristate#	FSEL0	FSEL1	CPU	SDRAM	3V66	PCI	48MHz	REF	APIC	Notes
0	0	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	2
0	1	X	TCLK/4	TCLK/4	TCLK/6	TCLK/12	TCLK/2	TCLK	TCLK/12	4, 5
1	0	0	66 MHz	100 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	33 MHz	3, 6, 7
1	1	0	100 MHz	100 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	33 MHz	3, 6, 7
1	0	1	133 MHz	133 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	33 MHz	3, 6, 7
1	1	1	133 MHz	100 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	33 MHz	3, 6, 7

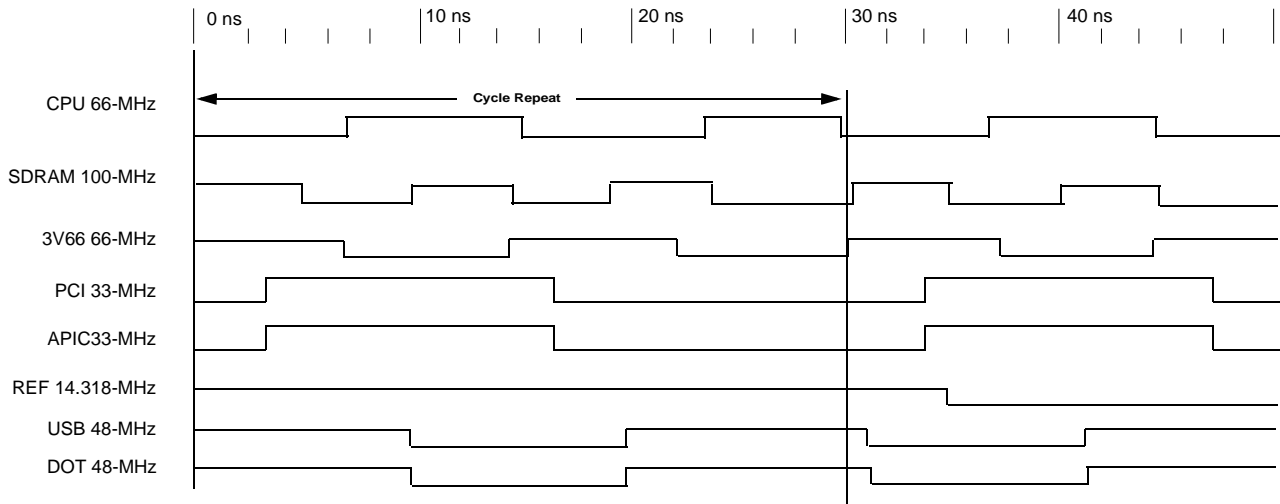
#### Notes:

2. Provided for board-level "bed of nails" testing.
3. "Normal" mode of operation.
4. TCLK is a test clock overdriven on the XTAL\_IN input during test mode.
5. Required for DC output impedance verification.
6. Range of reference frequency allowed is min. = 14.316 MHz, nominal = 14.31818 MHz, max. = 14.32 MHz.
7. Frequency accuracy of 48 MHz must be +167 PPM to match USB default.

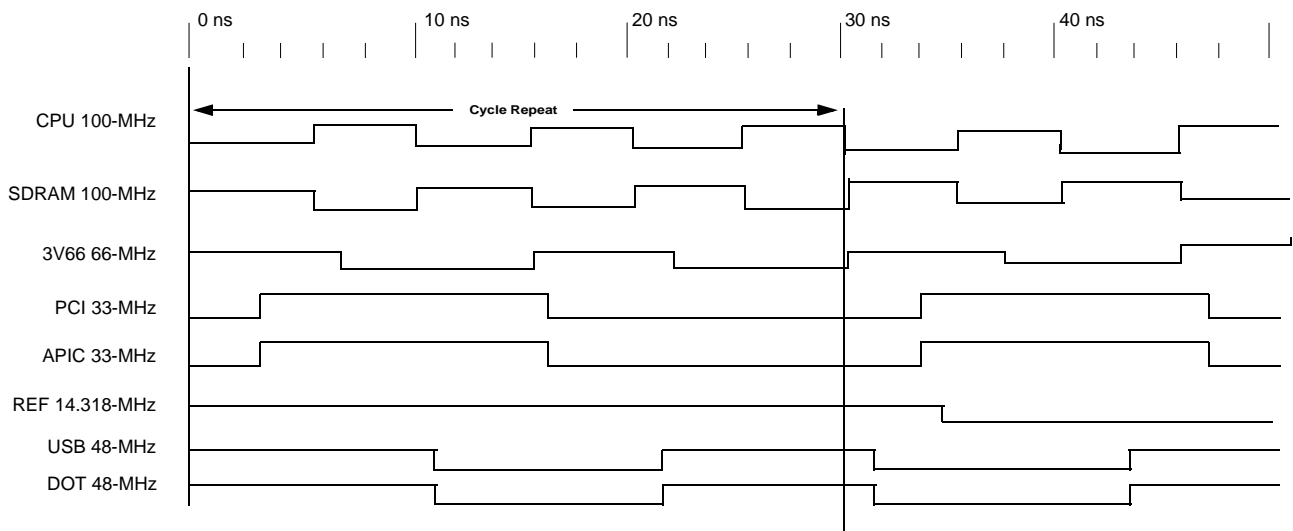
**Offsets Among Clock Signal Groups**

Figure 2 and Figure 3 represent the phase relationship among the different groups of clock outputs from W228B when it is providing a 66-MHz CPU clock and a 100-MHz CPU clock,

respectively. It should be noted that when the CPU clock is operating at 100 MHz, CPU clock output is 180 degrees out of phase with SDRAM clock outputs.



**Figure 2. Group Offset Waveforms (66-MHz CPU/100-MHz SDRAM Clock)**



**Figure 3. Group Offset Waveforms (100-MHz CPU/100-MHz SDRAM Clock)**

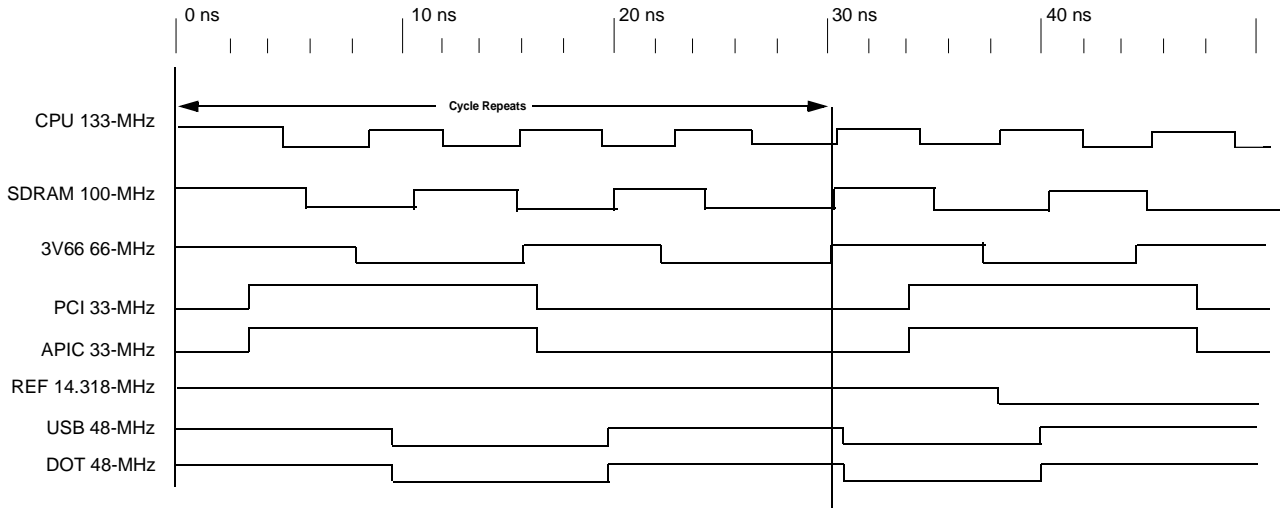


Figure 4. Group Offset Waveforms (133-MHz CPU/100-MHz SDRAM Clock)

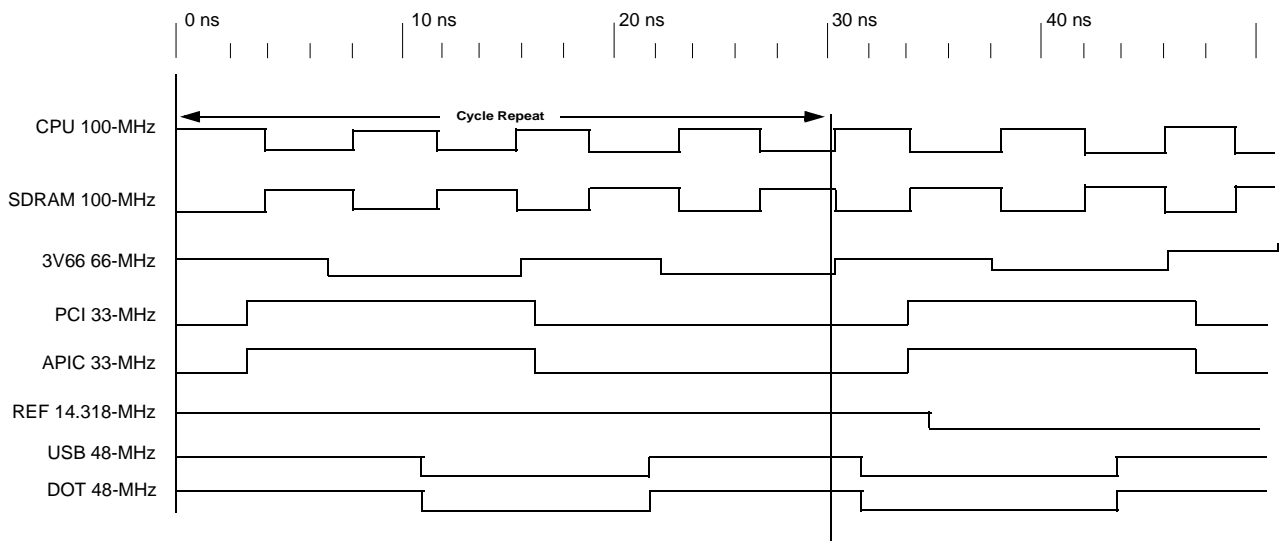


Figure 5. Group Offset Waveforms (133-MHz CPU/133-MHz SDRAM Clock)

**Power Down Control**

W228B provides one PWRDWN# signal to place the device in low-power mode. In low-power mode, the PLLs are turned off and all clock outputs are driven LOW.

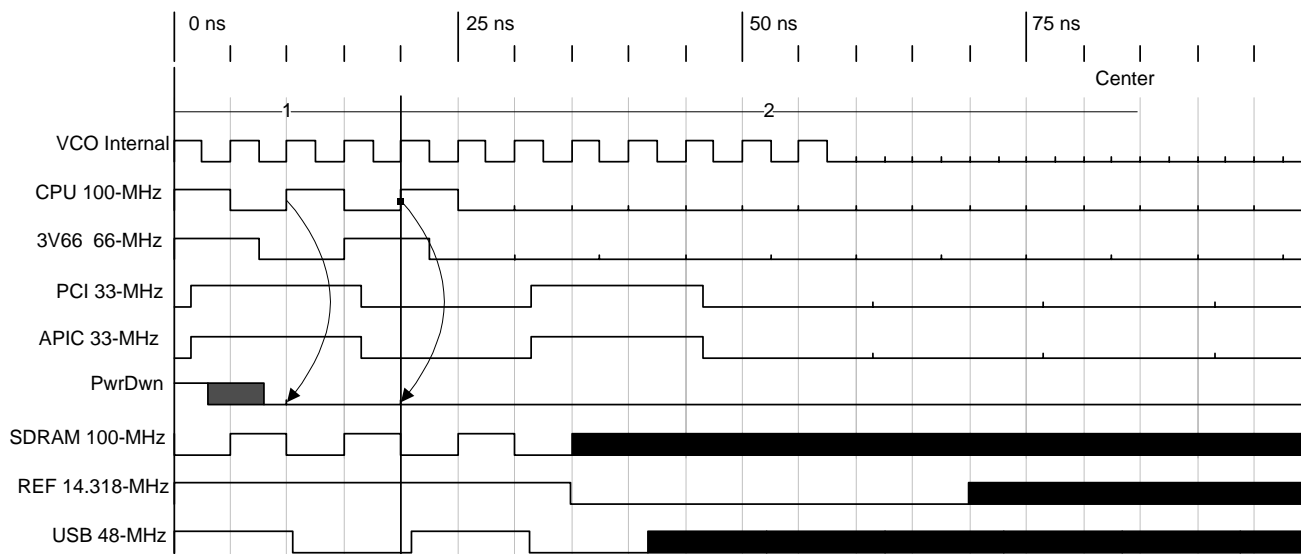


Figure 6. W228B PWRDWN# Timing Diagram<sup>[8, 9, 10, 11]</sup>

Table 3. W228B Maximum Allowed Current

W228B Condition	Max. 2.5V supply consumption Max. discrete cap loads, $V_{DDQ2} = 2.625V$ All static inputs = $V_{DDQ3}$ or $V_{SS}$	Max. 3.3V supply consumption Max. discrete cap loads $V_{DDQ3} = 3.465V$ All static inputs = $V_{DDQ3}$ or $V_{SS}$
Powerdown Mode (PWRDWN# = 0)	100 $\mu A$	500 $\mu A$
Full Active 66 MHz FSEL1:0 = 00 (PWRDWN# =1)	30 mA	280 mA
Full Active 100 MHz FSEL1:0 = 01 (PWRDWN# =1)	40 mA	280 mA
Full Active 133 MHz FSEL1:0 = 11 (PWRDWN# =1)	50 mA	400 mA

**Notes:**

8. Once the PWRDWN# signal is sampled LOW for two consecutive rising edges of CPU, clocks of interest will be held LOW on the next HIGH-to-LOW transition.
9. PWRDWN# is an asynchronous input and metastable conditions could exist. This signal is synchronized inside W228B.
10. The shaded sections on the SDRAM, REF, and USB clocks indicate "don't care" states.
11. Diagrams shown with respect to 100 MHz. Similar operation when CPU is 66 MHz.

### Spread Spectrum Frequency Timing Generator

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 7*.

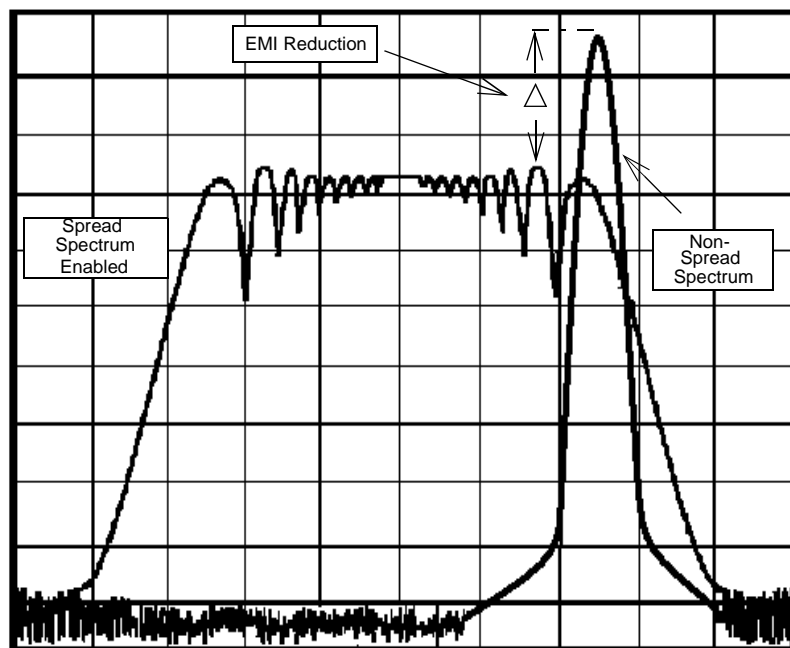
As shown in *Figure 7*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is:

$$dB = 6.5 + 9 \cdot \log_{10}(P) + 9 \cdot \log_{10}(F)$$

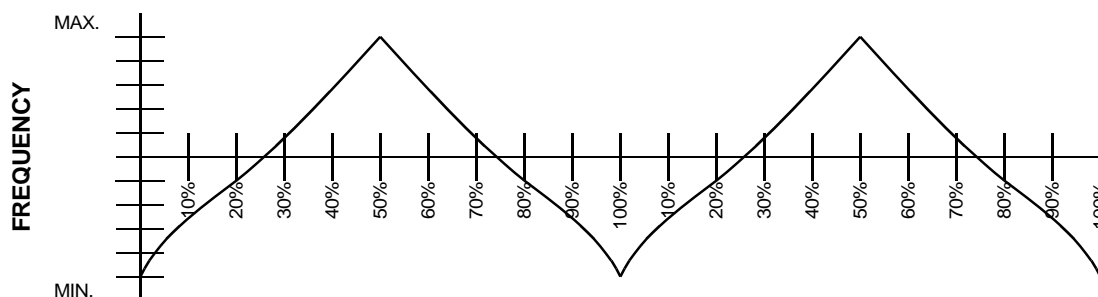
Where  $P$  is the percentage of deviation and  $F$  is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 8*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is  $-0.5\%$  of the selected frequency. *Figure 8* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

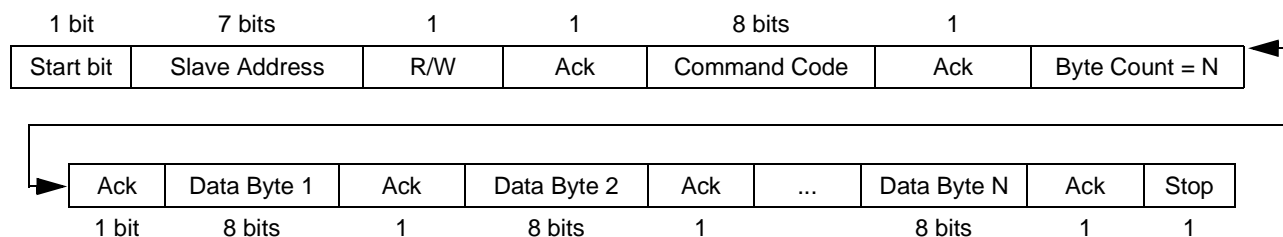
Spread Spectrum clocking is activated or deactivated by selecting the appropriate value for bit 3 in data byte 0 of the SMBus data stream. Refer to page 9 for more details.



**Figure 7. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation**



**Figure 8. Typical Modulation Profile**



**Figure 9. An Example of a Block Write<sup>[12]</sup>**

### Serial Data Interface

The W228B features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions.

### Data Protocol

The clock driver serial protocol accepts only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. Indexed bytes are not allowed.

A block write begins with a slave address and a write condition. After the command code the core logic issues a byte count which describes how many more bytes will follow in the message. If the host had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be 0. A block write command is allowed to

transfer a maximum of 32 data bytes. The slave receiver address for W228B is 11010010. *Figure 9* shows an example of a block write.

The command code and the byte count bytes are required as the first two bytes of any transfer. W228B expects a command code of 0000 0000. The byte count byte is the number of additional bytes required for the transfer, not counting the command code and byte count bytes. Additionally, the byte count byte is required to be a minimum of 1 byte and a maximum of 32 bytes to satisfy the above requirement. *Table 4* shows an example of a possible byte count value.

A transfer is considered valid after the acknowledge bit corresponding to the byte count is read by the controller. The command code and byte count bytes are ignored by the W228B. However, these bytes must be included in the data write sequence to maintain proper byte allocation.

**Table 4. Example of Possible Byte Count Value**

Byte Count Byte		Notes
MSB	LSB	
0000	0000	Not allowed. Must have at least one byte
0000	0001	Data for functional and frequency select register (currently byte 0 in spec)
0000	0010	Reads first two bytes of data (byte 0 then byte 1)
0000	0011	Reads first three bytes (byte 0, 1, 2 in order)
0000	0100	Reads first four bytes (byte 0, 1, 2, 3 in order)
0000	0101	Reads first five bytes (byte 0, 1, 2, 3, 4 in order) <sup>[13]</sup>
0000	0110	Reads first six bytes (byte 0, 1, 2, 3, 4, 5 in order) <sup>[13]</sup>
0000	0111	Reads first seven bytes (byte 0, 1, 2, 3, 4, 5, 6 in order)
0010	0000	Max. byte count supported = 32

**Table 5. Serial Data Interface Control Functions Summary**

Control Function	Description	Common Application
Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held LOW.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots.
Spread Spectrum Enabling	Enables or disables spread spectrum clocking.	For EMI reduction.
(Reserved)	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

**Notes:**

- 12. The acknowledgment bit is returned by the slave/receiver (W228B).
- 13. Data Bytes 3 to 7 are reserved.



**W228B Serial Configuration Map**

1. The serial bits will be read by the clock driver in the following order:

Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

2. All unused register bits (reserved and N/A) should be written to a "0" level.

3. All register bits labeled "Initialize to 0" must be written to zero during initialization. Failure to do so may result in higher than normal operating current.

4. Only Byte 0, 1, and 2 are defined in W228B. Byte 3 to Byte 7 are reserved and must be written to "zero."

**Byte 0: Control Register (1 = Enable, 0 = Disable)<sup>[14]</sup>**

Bit	Pin#	Name	Pin Description
Bit 7	-	Reserved	Reserved
Bit 6	-	Reserved	Reserved
Bit 5	-	Reserved	Reserved
Bit 4	-	Reserved	Reserved
Bit 3	-	Spread Spectrum (1 = On/0 = Off)	(Disabled/Enabled)
Bit 2	27	DOT	(Active/Inactive)
Bit 1	26	USB	(Active/Inactive)
Bit 0	--	Reserved	Reserved

**Byte 1: Control Register (1 = Enable, 0 = Disable)<sup>[14]</sup>**

Bit	Pin#	Name	Pin Description
Bit 7	38	SDRAM7	(Active/Inactive)
Bit 6	41	SDRAM6	(Active/Inactive)
Bit 5	42	SDRAM5	(Active/Inactive)
Bit 4	45	SDRAM4	(Active/Inactive)
Bit 3	46	SDRAM3	(Active/Inactive)
Bit 2	47	SDRAM2	(Active/Inactive)
Bit 1	50	SDRAM1	(Active/Inactive)
Bit 0	51	SDRAM0	(Active/Inactive)

**Byte 2: Control Register (1 = Enable, 0 = Disable)<sup>[14]</sup>**

Bit	Pin#	Name	Pin Description
Bit 7	12	3V66_AGP	(Active/Inactive)
Bit 6	29	SDRAM12	(Active/Inactive)
Bit 5	32	SDRAM11	(Active/Inactive)
Bit 4	33	SDRAM10	(Active/Inactive)
Bit 3	36	SDRAM9	(Active/Inactive)
Bit 2	37	SDRAM8	(Active/Inactive)
Bit 1	16	PCI1	(Active/Inactive)
Bit 0	-	(Reserved)	(Reserved)

**Note:**

14. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

**Byte 3: Reserved Register (1 = Enable, 0 = Disable)**

Bit	Pin#	Name	Pin Description
Bit 7	-	Reserved Drive to '0'	(Active/Inactive)
Bit 6	-	Reserved Drive to '0'	(Active/Inactive)
Bit 5	-	Reserved Drive to '0'	(Active/Inactive)
Bit 4	-	Reserved Drive to '0'	(Active/Inactive)
Bit 3	-	Reserved Drive to '0'	(Active/Inactive)
Bit 2	-	Reserved Drive to '0'	(Active/Inactive)
Bit 1		Reserved Drive to '0'	(Active/Inactive)
Bit 0	-	SDRAM 133-MHz Mode Enable Default is Disabled = '0', Enabled = '1'	(Disabled/Enabled)

**Byte 4: Reserved Register (1 = Enable, 0 = Disable)**

Bit	Pin#	Name	Pin Description
Bit 7	-	Reserved Drive to '0'	(Active/Inactive)
Bit 6	-	Reserved Drive to '0'	(Active/Inactive)
Bit 5	-	Reserved Drive to '0'	(Active/Inactive)
Bit 4	-	Reserved Drive to '0'	(Active/Inactive)
Bit 3	-	Reserved Drive to '0'	(Active/Inactive)
Bit 2	-	Reserved Drive to '0'	(Active/Inactive)
Bit 1		Reserved Drive to '0'	(Active/Inactive)
Bit 0	-	Reserved Drive to '0'	(Active/Inactive)

**DC Electrical Characteristics<sup>[15]</sup>**
**Absolute Maximum DC Power Supply**

Parameter	Description	Min.	Max.	Unit
V <sub>DD3</sub>	3.3V Core Supply Voltage	-0.5	4.6	V
V <sub>DDQ2</sub>	2.5V I/O Supply Voltage	-0.5	3.6	V
V <sub>DDQ3</sub>	3.3V Supply Voltage	-0.5	4.6	V
T <sub>S</sub>	Storage Temperature	-65	150	°C

**Absolute Maximum DC I/O**

Parameter	Description	Min.	Max.	Unit
V <sub>ih3</sub>	3.3V Input High Voltage	-0.5	4.6	V
V <sub>il3</sub>	3.3V Input Low Voltage	-0.5		V
ESD prot.	Input ESD Protection	2000		V

**DC Operating Requirements**

Parameter	Description	Condition	Min.	Max.	Unit
V <sub>DD3</sub>	3.3V Core Supply Voltage	3.3V±5%	3.135	3.465	V
V <sub>DDQ3</sub>	3.3V I/O Supply Voltage	3.3V±5%	3.135	3.465	V
V <sub>DDQ2</sub>	2.5V I/O Supply Voltage	2.5V±5%	2.375	2.625	V
V <sub>DD3</sub> = 3.3V±5%					
V <sub>ih3</sub>	3.3V Input High Voltage	V <sub>DD3</sub>	2.0	V <sub>DD</sub> + 0.3	V
V <sub>il3</sub>	3.3V Input Low Voltage		V <sub>SS</sub> - 0.3	0.8	V
I <sub>il</sub>	Input Leakage Current <sup>[16]</sup>	0 < V <sub>in</sub> < V <sub>DD3</sub>	-5	+5	µA
V <sub>DDQ2</sub> = 2.5V±5%					
V <sub>oh2</sub>	2.5V Output High Voltage	I <sub>oh</sub> = (-1 mA)	2.0		V
V <sub>ol2</sub>	2.5V Output Low Voltage	I <sub>ol</sub> = (1 mA)		0.4	V
V <sub>DDQ3</sub> = 3.3V±5%					
V <sub>oh3</sub>	3.3V Output High Voltage	I <sub>oh</sub> = (-1 mA)	2.4		V
V <sub>ol3</sub>	3.3V Output Low Voltage	I <sub>ol</sub> = (1 mA)		0.4	V
V <sub>DDQ3</sub> = 3.3V±5%					
V <sub>poh3</sub>	PCI Bus Output High Voltage	I <sub>oh</sub> = (-1 mA)	2.4		V
V <sub>pol3</sub>	PCI Bus Output Low Voltage	I <sub>ol</sub> = (1 mA)		0.55	V
C <sub>in</sub>	Input Pin Capacitance			5	pF
C <sub>xtal</sub>	Xtal Pin Capacitance		13.5	22.5	pF
C <sub>out</sub>	Output Pin Capacitance			6	pF
L <sub>pin</sub>	Pin Inductance		0	7	nH
T <sub>a</sub>	Ambient Temperature	No Airflow	0	70	°C

**Note:**

15. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.  
 16. Input Leakage Current does not include inputs with pull-up or pull-down resistors.

**AC Electrical Characteristics<sup>[15]</sup>**
 $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ ,  $V_{DDQ3} = 3.3\text{V}\pm 5\%$ ,  $V_{DDQ2} = 2.5\text{V}\pm 5\%$ 
 $f_{XTL} = 14.31818\text{ MHz}$ 

Spread Spectrum function turned off

 AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.<sup>[17]</sup>
**AC Electrical Characteristics**

Parameter	Description	66.6-MHz Host		100-MHz Host		133-MHz Host		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
$T_{\text{Period}}$	Host/CPUCLK Period	15.0	15.5	10.0	10.5	7.5	8.0	ns	17
$T_{\text{HIGH}}$	Host/CPUCLK High Time	5.2	N/A	3.0	N/A	1.87	N/A	ns	20
$T_{\text{LOW}}$	Host/CPUCLK Low Time	5.0	N/A	2.8	N/A	1.67	N/A	ns	
$T_{\text{RISE}}$	Host/CPUCLK Rise Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	21
$T_{\text{FALL}}$	Host/CPUCLK Fall Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	21
$T_{\text{Period}}$	SDRAM CLK Period (100-MHz)	10.0	10.5	10.0	10.5	10.0	10.5	ns	17
$T_{\text{HIGH}}$	SDRAM CLK High Time (100-MHz)	3.0	N/A	3.0	N/A	3.0	N/A	ns	20
$T_{\text{LOW}}$	SDRAM CLK Low Time (100-MHz)	2.8	N/A	2.8	N/A	2.8	N/A	ns	
$T_{\text{RISE}}$	SDRAM CLK Rise Time (100-MHz)	0.4	1.6	0.4	1.6	0.4	1.6	ns	21
$T_{\text{FALL}}$	SDRAM CLK Fall Time (100-MHz)	0.4	1.6	0.4	1.6	0.4	1.6	ns	21
$T_{\text{Period}}$	SDRAM CLK Period (133-MHz)	7.5	8.0	7.5	8.0	7.5	8.0	ns	17
$T_{\text{HIGH}}$	SDRAM CLK High Time (133-MHz)	1.87	N/A	1.87	N/A	1.87	N/A	ns	20
$T_{\text{LOW}}$	SDRAM CLK Low Time (133-MHz)	1.67	N/A	1.67	N/A	1.67	N/A	ns	
$T_{\text{RISE}}$	SDRAM CLK Rise Time (133-MHz)	0.4	1.6	0.4	1.6	0.4	1.6	ns	21
$T_{\text{FALL}}$	SDRAM CLK Fall Time (133-MHz)	0.4	1.6	0.4	1.6	0.4	1.6	ns	21
$T_{\text{Period}}$	APIC 33-MHz CLK Period	30.0	N/A	30.0	N/A	30.0	N/A	ns	17
$T_{\text{HIGH}}$	APIC 33-MHz CLK High Time	12.0	N/A	12.0	N/A	12.0	N/A	ns	20
$T_{\text{LOW}}$	APIC 33-MHz CLK Low Time	12.0	N/A	12.0	N/A	12.0	N/A	ns	
$T_{\text{RISE}}$	APIC CLK Rise Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	21
$T_{\text{FALL}}$	APIC CLK Fall Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	21
$T_{\text{Period}}$	3V66 CLK Period	15.0	16.0	15.0	16.0	15.0	16.0	ns	17, 19
$T_{\text{HIGH}}$	3V66 CLK High Time	5.25	N/A	5.25	N/A	5.25	N/A	ns	20
$T_{\text{LOW}}$	3V66 CLK Low Time	5.05	N/A	5.05	N/A	5.05	N/A	ns	
$T_{\text{RISE}}$	3V66 CLK Rise Time	0.5	2.0	0.5	2.0	0.5	2.0	ns	21
$T_{\text{FALL}}$	3V66 CLK Fall Time	0.5	2.0	0.5	2.0	0.5	2.0	ns	21
$T_{\text{Period}}$	PCI CLK Period	30.0	N/A	30.0	N/A	30.0	N/A	ns	17, 18
$T_{\text{HIGH}}$	PCI CLK High Time	12.0	N/A	12.0	N/A	12.0	N/A	ns	20
$T_{\text{LOW}}$	PCI CLK Low Time	12.0	N/A	12.0	N/A	12.0	N/A	ns	
$T_{\text{RISE}}$	PCI CLK Rise Time	0.5	2.0	0.5	2.0	0.5	2.0	ns	21
$T_{\text{FALL}}$	PCI CLK Fall Time	0.5	2.0	0.5	2.0	0.5	2.0	ns	21

**Notes:**

17. Period, jitter, offset, and skew measured on rising edge at 1.25 for 2.5V clocks and at 1.5V for 3.3V clocks.

 18.  $T_{\text{HIGH}}$  is measured at 2.0V for 2.5V outputs, 2.4V for 3.3V outputs.

 19.  $T_{\text{LOW}}$  is measured at 0.4V for all outputs.

 20. The time specified is measured from when  $V_{DDQ3}$  achieves its nominal operating level (typical condition  $V_{DDQ3} = 3.3\text{V}$ ) until the frequency output is stable and operating within specification.

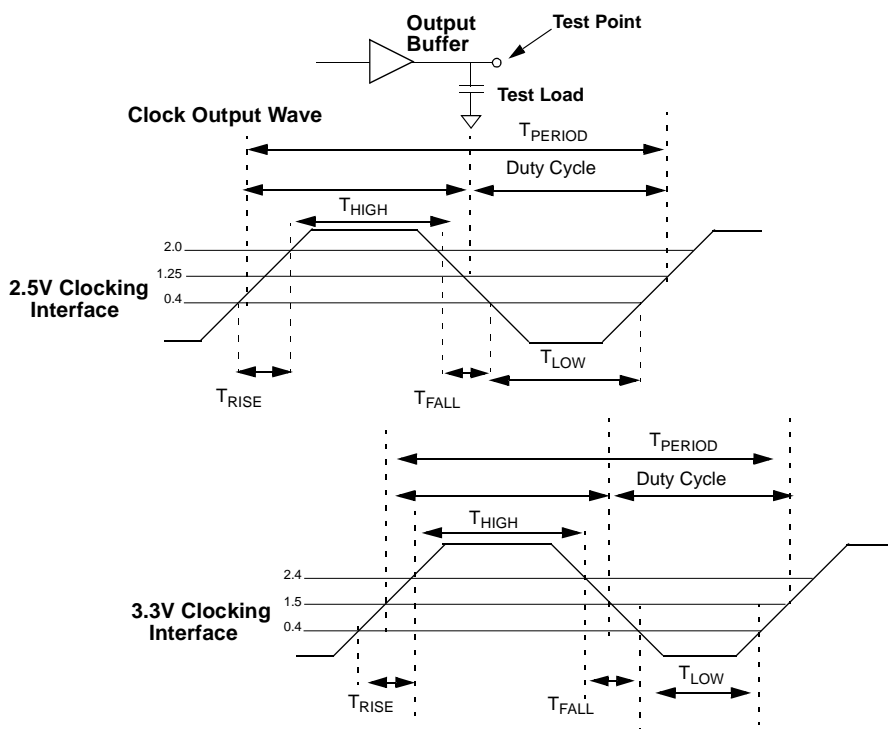
 21.  $T_{\text{RISE}}$  and  $T_{\text{FALL}}$  are measured as a transition through the threshold region  $V_{ol} = 0.4\text{V}$  and  $V_{oh} = 2.0\text{V}$  (1 mA) JEDEC specification for 2.5V outputs and  $V_{OL} = 0.4\text{V}$  and  $V_{OH} = 2.4\text{V}$  for 3.3V outputs.

**AC Electrical Characteristics** (continued)

Parameter	Description	66.6-MHz Host		100-MHz Host		133-MHz Host		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{pZL}, t_{pZH}$	Output Enable Delay (All outputs)	1.0	10.0	1.0	10.0	1.0	10.0	ns	
$t_{pLZ}, t_{pZH}$	Output Disable Delay (All outputs)	1.0	10.0	1.0	10.0	1.0	10.0	ns	
$t_{stable}$	All Clock Stabilization from Power-Up		3		3		3	ms	

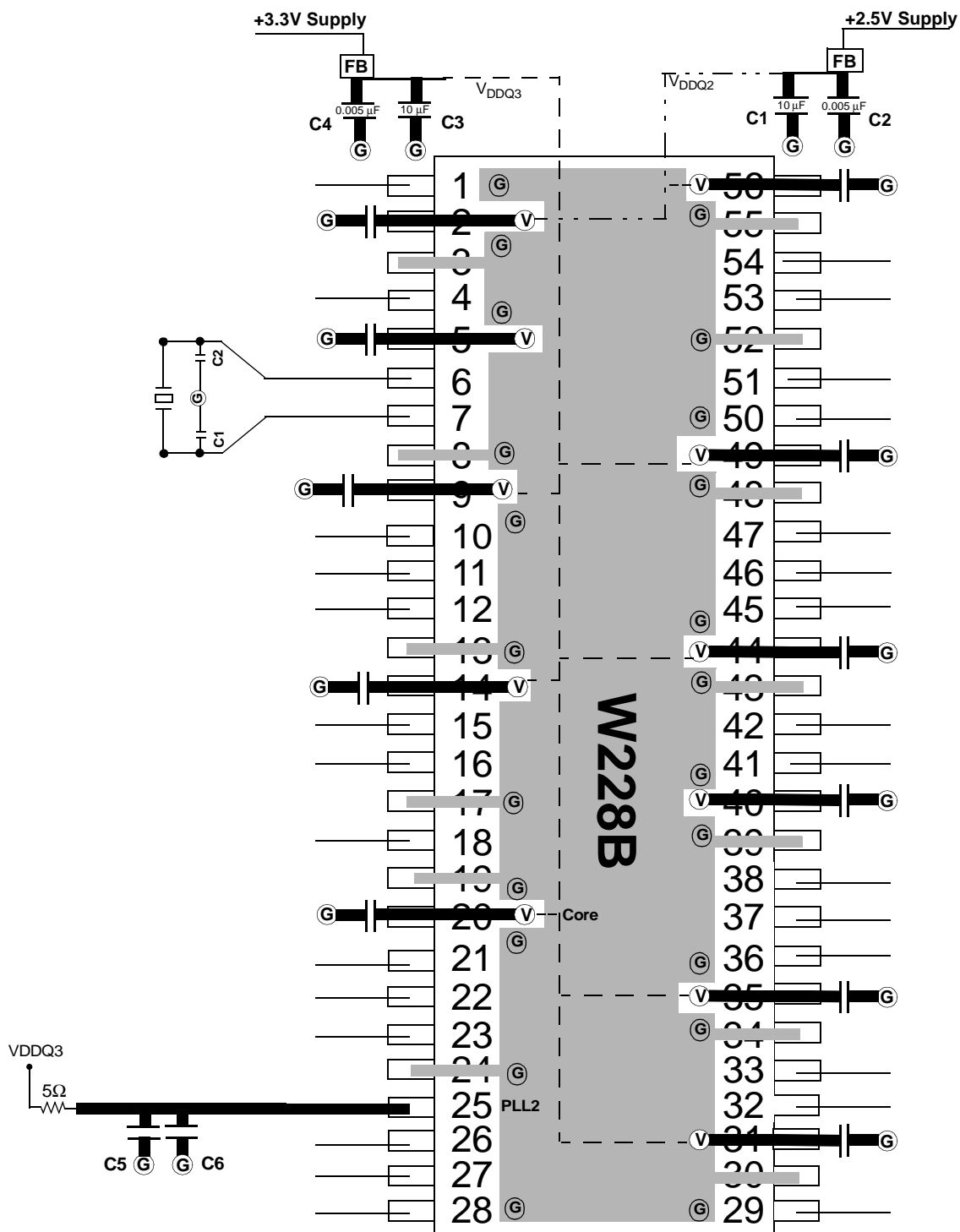
**Group Skew and Jitter Limits**

Output Group	Pin-Pin Skew Max.	Cycle-Cycle Jitter	Duty Cycle	Nom. V <sub>dd</sub>	Skew, Jitter Measure Point
CPU	175 ps	250 ps	45/55	2.5V	1.25V
SDRAM	250 ps	250 ps	45/55	3.3V	1.5V
APIC	250 ps	500 ps	45/55	2.5V	1.25V
48MHz	250 ps	500 ps	45/55	3.3V	1.5V
3V66	175 ps	500 ps	45/55	3.3V	1.5V
PCI	500 ps	500 ps	45/55	3.3V	1.5V
REF	N/A	1000 ps	45/55	3.3V	1.5V


**Figure 10. Output Buffer**
**Ordering Information**

Ordering Code	Package Name	Package Type
W228B	H	56-pin SSOP (300 mils)

Layout Diagram

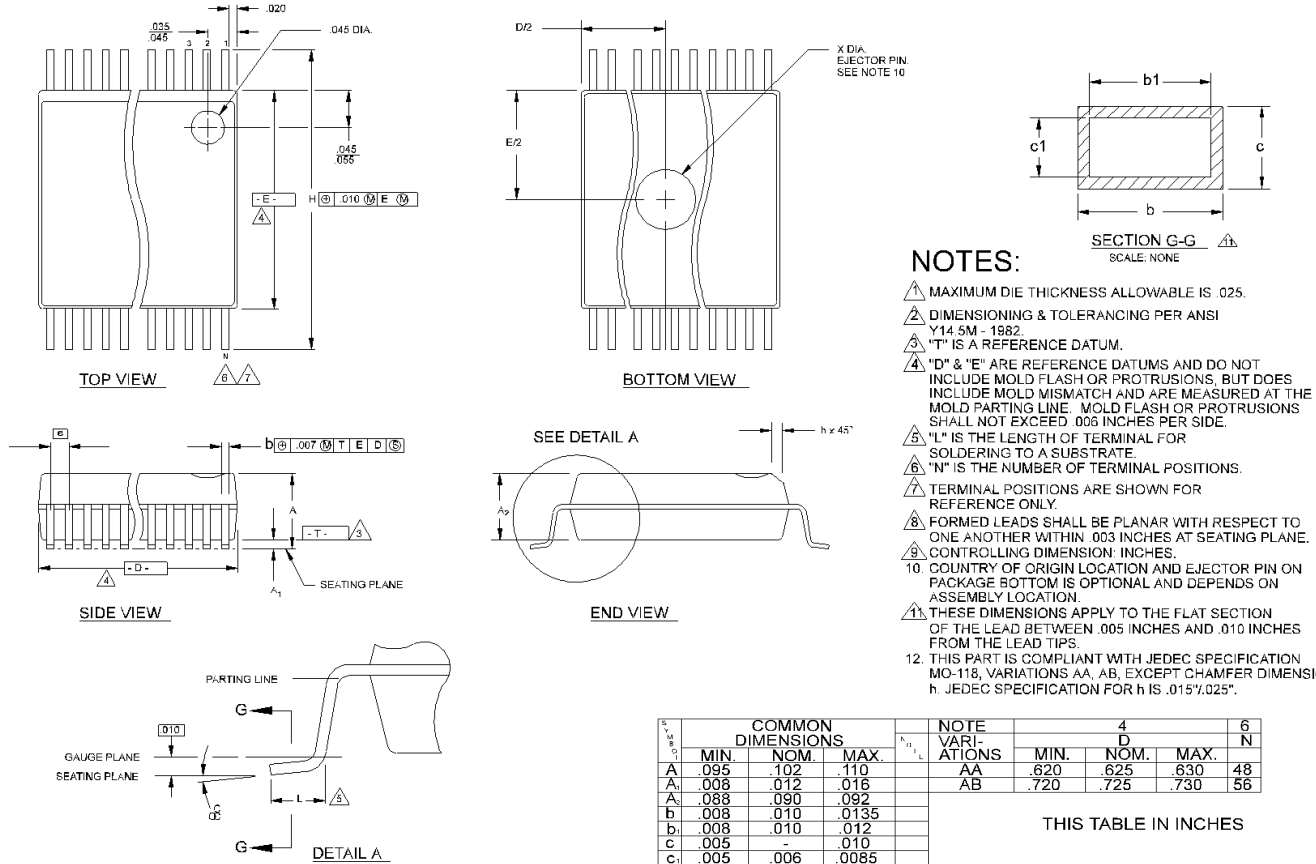


FB = Dale ILB1206 - 300 (300Ω @ 100 MHz)

C1 & C3 = 10–22 μF    C2 & C4 = 0.005 μF    C5 = 47 μF    C6 = 0.1 μF

Ⓞ = VIA to GND plane layer    Ⓟ = VIA to respective supply plane layer

**Note:** Each supply plane or strip should have a ferrite bead and capacitors  
All V<sub>DD</sub> Bypass = 0.1 μF

**Package Diagram**
**56-Pin Shrink Small Outline Package (SSOP, 300 mils)**

**Summary of nominal dimensions in inches:**

**Body Width: 0.296**  
**Lead Pitch: 0.025**  
**Body Length: 0.625**  
**Body Height: 0.102**

Symbol	COMMON DIMENSIONS			NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.102	.110	AA	.620	.625	.630	48
A <sub>1</sub>	.088	.090	.092	AB	.720	.725	.730	56
b	.008	.010	.0135					
b <sub>1</sub>	.008	.010	.012					
c	.005	-	.010					
c <sub>1</sub>	.005	.006	.0085					
D	SEE VARIATIONS			4				
E	.292	.296	.299					
e	.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	SEE VARIATIONS			6				
X	.085	.093	.100	10				
α	0°	5°	8°					

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Symbol	COMMON DIMENSIONS			NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	2.41	2.59	2.79	AA	15.75	15.88	16.00	48
A <sub>1</sub>	0.20	0.33	0.41	AB	18.29	18.42	18.54	56
b	0.203	0.254	0.343					
b <sub>1</sub>	0.203	0.254	0.305					
c	0.127	-	0.254					
c <sub>1</sub>	0.127	0.152	0.216					
D	SEE VARIATIONS			4				
E	7.42	7.52	7.59					
e	0.635 BSC							
H	10.16	10.31	10.41					
h	0.25	0.33	0.41					
L	0.61	0.81	1.02					
N	SEE VARIATIONS			6				
X	2.16	2.36	2.54	10				
α	0°	5°	8°					

THIS TABLE IN MILLIMETERS

**Revision History**

<b>Document Title: W228B FTG for Integrated Core Logic with 133-MHz FSB</b>				
<b>Document Number: 38-07180</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	111856	12/09/01	DSG	Change from Spec number: 38-00883 to 38-07180
*A	122820	12/22/02	RBI	Add Power up Requirements to Electrical Characteristics Information