128Kx32 SRAM MODULE *PRELIMINARY**

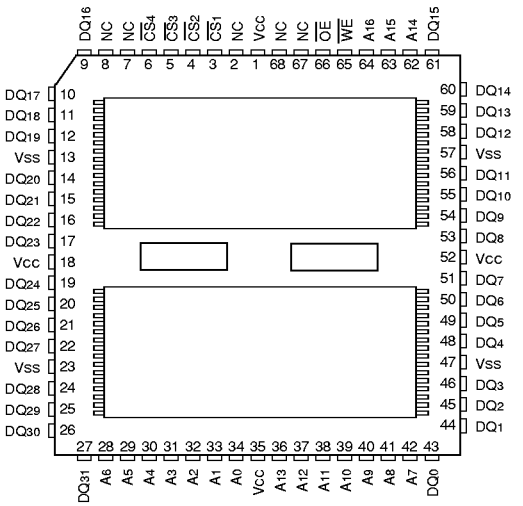
FEATURES

- Access Times of 15, 17, 20, 25, 35ns
- Packaging:
  - 68 Lead, Plastic PLCC, 24.71 mm (0.973 inch) square
- Organized as 128Kx32
- Commercial and Industrial Temperature Ranges
- TTL Compatible Inputs and CMOS Outputs
- PJ Pinout for Commercial Applications
- G2 Pinout for Upgrade Path to Military Grade Device
- 5 Volt Power Supply
- Low Power CMOS
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation

* *This data sheet describes a product under development, not fully characterized and is subject to change without notice.*

FIG. 1 PIN CONFIGURATION FOR WPS128K32P-XPJX, PJ pinout for Commercial Applications

TOP VIEW



NOTE: Pin-for-pin compatible with the molded PLCC modules.

PIN DESCRIPTION

DQ_{0-31}	Data Inputs/Outputs
A_{0-16}	Address Inputs
$\overline{WE}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	Not Connected

BLOCK DIAGRAM

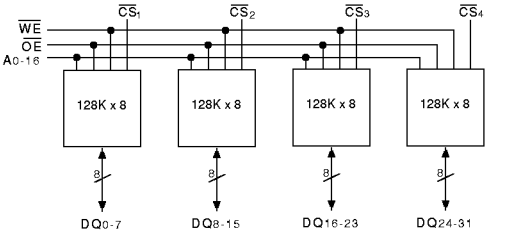
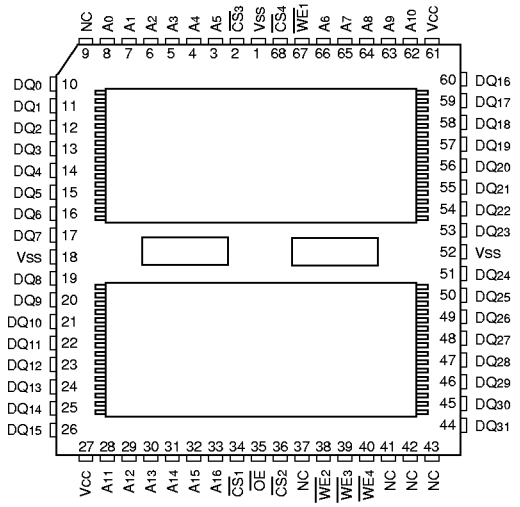


FIG. 2 PIN CONFIGURATION FOR WPS128K32G-XPJX, for upgrade to Military Grade Devices

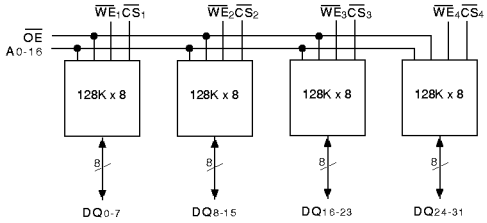
TOP VIEW



PIN DESCRIPTION

DQ0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
Vss	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature (Com.)	T_A	0	+70	°C
Operating Temperature (Ind.)	T_A	-40	+85	°C
Storage Temperature	T_{STG}	-55	+125	°C
Signal Voltage Relative to Vss	V_G	-0.5	Vcc + 0.5	V
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	Vcc + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp (Com.)	T_A	0	+70	°C
Operating Temp (Ind.)	T_A	-40	+85	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

CAPACITANCE

(@ T_A = +25°C)

Parameter		Symbol	Condition	Max	Unit
$\overline{OE}$ Capacitance		C_{OE}	V_{IN} = 0V, f = 1.0MHz	50	pF
$\overline{WE}$ Capacitance	G pinout	C_{WE}	V_{IN} = 0V, f = 1.0MHz	20	pF
	P pinout			20	
$\overline{CS}_{1-4}$ Capacitance		C_{CS}	V_{IN} = 0V, f = 1.0MHz	20	pF
DQ_{0-31} Capacitance		$C_{I/O}$	V_{IN} = 0V, f = 1.0MHz	20	pF
A_{0-16} Capacitance		C_{AD}	V_{IN} = 0V, f = 1.0MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -40 to +85°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = Vss to Vcc		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = Vss to Vcc		10	µA
Operating Supply Current x 32 Mode	I_{CC} x 32	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		450	mA
Standby Current	I_{SB}	$\overline{CS}$ = Vcc, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		50	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, Vcc = 4.5		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, Vcc = 4.5	2.4		V

NOTE: DC test conditions: V_{IL} = 0.3V, V_{IH} = Vcc -0.3V

AC CHARACTERISTICS

(VCC = 5.0V, TA = -40 to +85°C)

Parameter Read Cycle	Symbol	-15		-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		25		35		ns
Address Access Time	t_{AA}		15		17		20		25		35	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		0		ns
Chip Select Access Time	t_{ACS}		15		17		20		25		35	ns
Output Enable to Output Valid	t_{OE}		8		9		10		12		20	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	3		3		3		3		3		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		7		8		8		10		20	ns
Output Disable to Output in High Z	t_{OHZ}[1]		7		8		8		10		20	ns

1. This parameter is guaranteed by design but not tested.

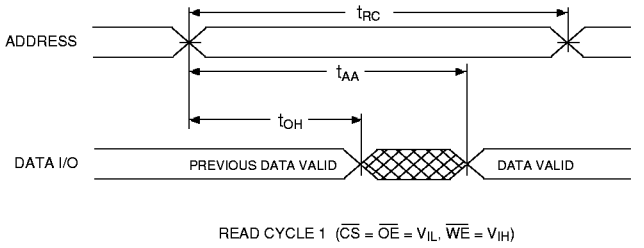
AC CHARACTERISTICS

(VCC = 5.0V, TA = -40 to +85°C)

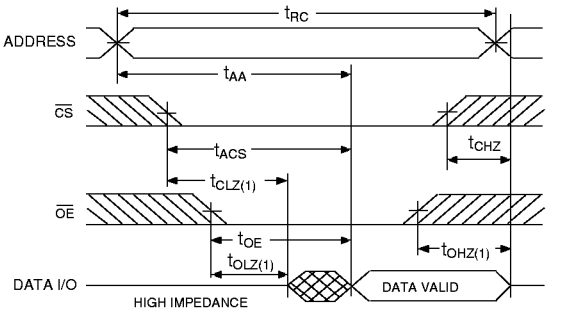
Parameter Write Cycle	Symbol	-15		-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max			
Write Cycle Time	t_{WC}	15		17		20		25		35		ns
Chip Select to End of Write	t_{CW}	11		12		13		15		25		ns
Address Valid to End of Write	t_{AW}	11		12		13		15		25		ns
Data Valid to End of Write	t_{DW}	9		10		10		10		20		ns
Write Pulse Width	t_{WP}	11		12		13		15		25		ns
Address Setup Time	t_{AS}	0		0		0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		0		0		ns
Output Active from End of Write	t_{OW}[1]	3		3		3		3		4		ns
Write Enable to Output in High Z	t_{WHZ}[1]		8		10		10		11		15	ns
Data Hold Time	t_{DH}	3		3		3		3		3		ns

1. This parameter is guaranteed by design but not tested.

FIG. 3
TIMING WAVEFORM - READ CYCLE



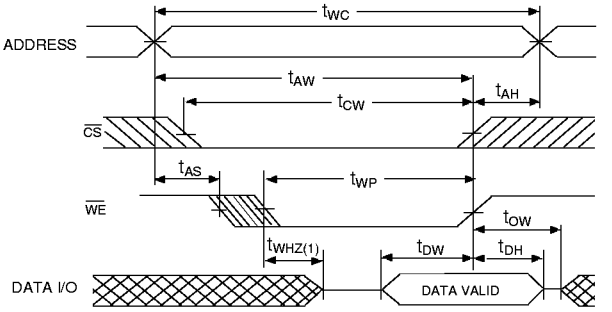
READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



READ CYCLE 2 ($\overline{WE}$ = V_{IH})

(1) GUARANTEED BY DESIGN BUT NOT TESTED

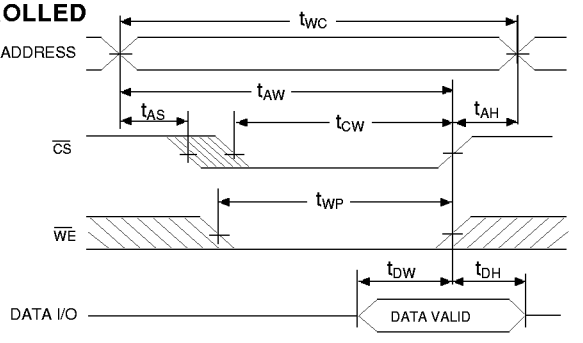
FIG. 4
WRITE CYCLE - $\overline{WE}$ CONTROLLED ($\overline{OE}$ IS INACTIVE - HIGH)



WRITE CYCLE 1 $\overline{WE}$ CONTROLLED ($\overline{OE}$ = V_{IH})

(1) GUARANTEED BY DESIGN BUT NOT TESTED

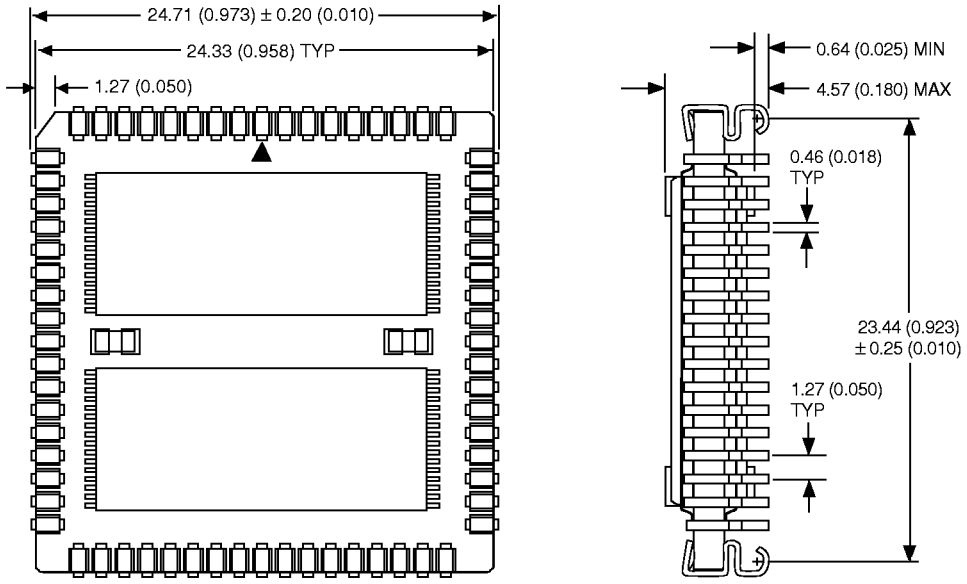
FIG. 5
WRITE CYCLE - $\overline{CS}$ CONTROLLED



WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

PACKAGE 708: 68 LEAD PLCC



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W P S 128K 32 X - XX PJ X

DEVICE GRADE:
C = Commercial 0°C to +70°C
I = Industrial -40°C to +85°C

PACKAGE TYPE:
PJ = 68 Lead Plastic PLCC

ACCESS TIME (ns)

IMPROVEMENT MARK
G = G2 pinout for upgrade path to military grade device
P = PJ pinout for commercial applications

ORGANIZATION, 128K x 32

SRAM

Plastic Multichip Module

WHITE MICROELECTRONICS