P4C163/P4C163L
ULTRA HIGH SPEED 8K x 9
STATIC CMOS RAMS (SCRAMS)

FEATURES

- **Full CMOS, 6T Cell**
- **High Speed (Equal Access and Cycle Times)**
  - **25/35ns (Commercial)**
  - **25/35/45ns (Military)**
- **Low Power Operation (Commercial/Military)**
  - **690/800 mW Active – 25**
  - **193/220 mW Standby (TTL Input)**
  - **5.5 mW Standby (CMOS Input) P4C163L**
- **Output Enable and Dual Chip Enable Control Functions**
- **Single 5V±10% Power Supply**
- **Data Retention with 2.0V Supply, 10 µA Typical Current (P4C163L Military)**
- **Common I/O**
- **Fully TTL Compatible Inputs and Outputs**
- **Produced with PACE II Technology™**
- **Standard Pinout (JEDEC Approved)**
  - **28-Pin 300 mil DIP, SOJ**
  - **28-Pin 350 x 550 mil LCC**

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DESCRIPTION

The P4C163 and P4C163L are 73,728-bit ultra high-speed static RAMs organized as 8K x 9. The CMOS memories require no clocks or refreshing and have equal access and cycle times. Inputs are fully TTL-compatible. The RAMs operate from a single 5V±10% tolerance power supply. With battery backup, data integrity is maintained for supply voltages down to 2.0V. Current drain is 10 µA from a 2.0V supply.

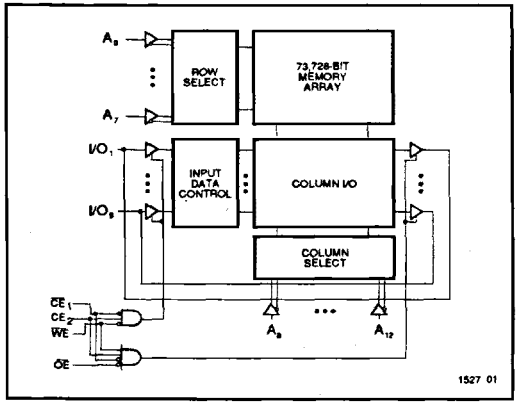
Access times as fast as 25 nanoseconds are available, permitting greatly enhanced system operating speeds. CMOS is used to reduce power consumption in both active and standby modes. The P4C163 and P4C163L are members of a family of PACE RAM™ products offering super fast access times never before available at these complexity levels in TTL-compatible bipolar or CMOS technologies.

The P4C163 and P4C163L are manufactured with PACE II Technology which is Performance Advanced CMOS Engineering to use 0.7 micron effective channel lengths giving 400 picosecond loaded* internal gate delays. PACE II Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, this technology features latch-up protection and single-event-upset protection, and is supported by a Class 1 facility for volume production.

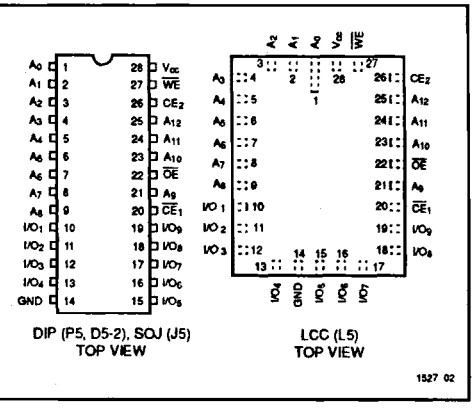
The P4C163 and P4C163L are available in 28-pin 300 mil DIP and SOJ and 28-pin 350 x 550 mil LCC packages providing excellent board level densities.

*For a fan-in/fan-out of 4 at 85°C junction temperature and 5.0 V supply.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	–0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–55 to +125	°C

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Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

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RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade[2]	Ambient Temperature	GND	V_{CC}
Military	–55 to +125°C	0V	5.0V ± 10%

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Grade[2]	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage[2]

Symbol	Parameter	Test Conditions		P4C163		P4C163L		Unit
				Min	Max	Min	Max	
V_{IH}	Input High Voltage			2.2	V_{CC}+0.5	2.2	V_{CC}+0.5	V
V_{IL}	Input Low Voltage			–0.5[3]	0.8	–0.5[3]	0.8	V
V_{HC}	CMOS Input High Voltage			V_{CC}–0.2	V_{CC}+0.5	V_{CC}–0.2	V_{CC}+0.5	V
V_{LC}	CMOS Input Low Voltage			–0.5[3]	0.2	–0.5[3]	0.2	V
V_{CD}	Input Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–1.2		–1.2	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +8 mA, V_{CC} = Min.			0.4		0.4	V
V_{OLC}	Output Low Voltage (CMOS Load)	I_{OLC} = +100 µA, V_{CC} = Min.			0.2		0.2	V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = –4 mA, V_{CC} = Min.		2.4		2.4		V
V_{OHC}	Output High Voltage (CMOS Load)	I_{OHC} = –100 µA, V_{CC} = Min.		V_{CC}–0.2		V_{CC}–0.2		V
I_{LI}	Input Leakage Current	V_{CC} = Max. V_{IN} = GND to V_{CC}	Mil. Com'l.	–10 –5	+10 +5	–5 N/A	+5 N/A	µA
I_{LO}	Output Leakage Current	V_{CC} = Max., $\overline{CE}$ = V_{IH}, V_{OUT}= GND to V_{CC}	Mil. Com'l.	–10 –5	+10 +5	–5 N/A	+5 N/A	µA

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CAPACITANCES[4]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF

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Symbol	Parameter	Conditions	Typ.	Unit
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

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Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20 ns.
4. This parameter is sampled and not 100% tested.

POWER DISSIPATION CHARACTERISTICS

Over recommended operating temperature and supply voltage[2]

Symbol	Parameter	Test Conditions		P4C163 Min	P4C163 Max	P4C163L Min	P4C163L Max	Unit
I_{CC}	Dynamic Operating Current – 25	V_{CC} = Max., f = Max., Outputs Open	Mil.	—	145	—	145	mA
			Com'l.	—	125	—	N/A	
I_{CC}	Dynamic Operating Current – 35, 45	V_{CC} = Max., f = Max., Outputs Open	Mil.	—	120	—	120	mA
			Com'l.	—	95	—	N/A	
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$, V_{CC} = Max., f = Max., Outputs Open	Mil.	—	40	—	40	mA
			Com'l.	—	35	—	N/A	
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE}_1 \geq V_{HC}$ or $CE_2 \leq V_{LC}$, V_{CC} = Max., f = 0, Outputs Open, $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	Mil.	—	20	—	1	mA
			Com'l.	—	18	—	N/A	

n/a = Not Applicable

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DATA RETENTION CHARACTERISTICS (P4C163L, Military Temperature Only)

Symbol	Parameter	Test Condition	Min	Typ.* V_{CC}= 2.0V	Typ.* V_{CC}= 3.0V	Max V_{CC}= 2.0V	Max V_{CC}= 3.0V	Unit
V_{DR}	V_{CC} for Data Retention		2.0					V
I_{CCDR}	Data Retention Current	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		10	15	200	300	µA
t_{CDR}	Chip Deselect to Data Retention Time		0					ns
t_R†	Operation Recovery Time		t_{RC}§					ns

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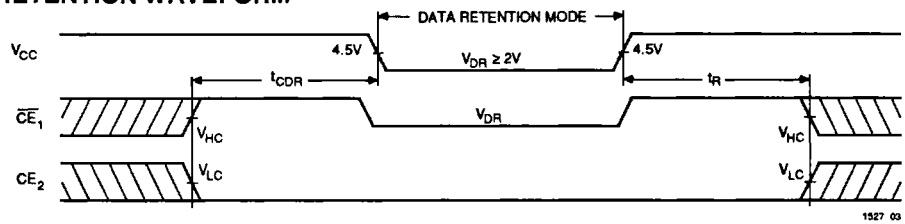
*T_A = +25°C

§t_{RC} = Read Cycle Time

†This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



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AC ELECTRICAL CHARACTERISTICS—READ CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Symbol	Parameter	-25		-35		-45		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address Access Time		25		35		45	ns
t_{AC}	Chip Enable Access Time		25		35		45	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{LZ}	Chip Enable to Output in Low Z	3		3		3		ns
t_{HZ}	Chip Disable to Output in High Z		10		15		20	ns
t_{OE}	Output Enable Low to Data Valid		13		18		20	ns
t_{OLZ}	Output Enable Low to Low Z	3		3		3		ns
t_{OHZ}	Output Enable High to High Z		12		15		20	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		ns
t_{PD}	Chip Disable to Power Down Time		20		20		25	ns

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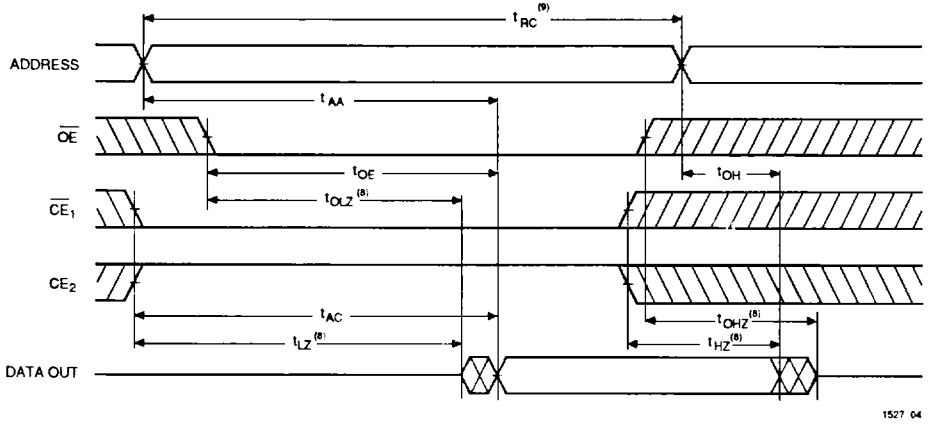
READ CYCLE NO. 1 ($\overline{OE}$ CONTROLLED) [5]



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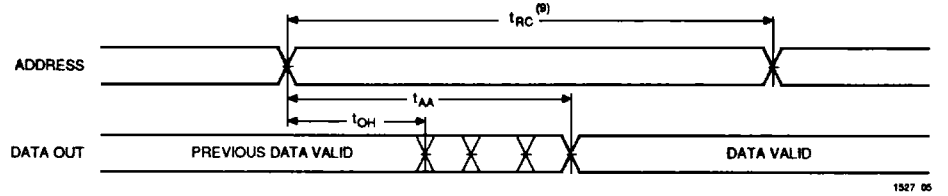
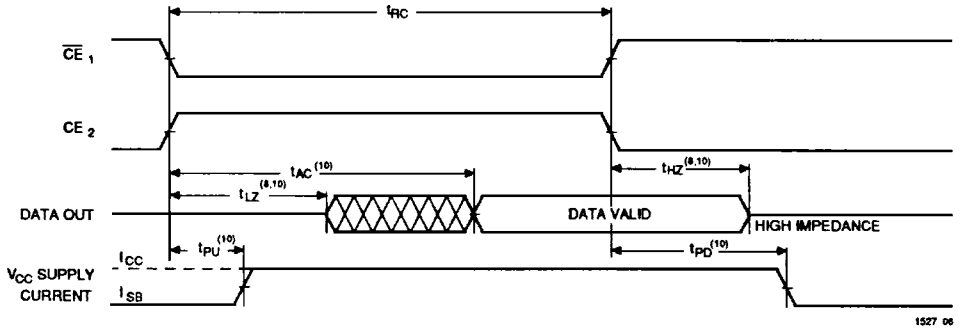
Notes:

5. $\overline{WE}$ is HIGH for READ cycle.
6. $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{OE}$ is LOW for READ cycle.
7. ADDRESS must be valid prior to, or coincident with $\overline{CE}_1$ transition low and CE_2 transition HIGH.
8. Transition is measured ± 200mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.

READ CYCLE NO. 2 (ADDRESS CONTROLLED) [5,6]



READ CYCLE NO. 3 ($\overline{CE}_1$, CE_2 CONTROLLED) [5,7,10]



Notes:

9. READ Cycle Time is measured from the last valid address to the first transitioning address.
10. Transitions caused by a chip enable control have similar delays irrespective of whether $\overline{CE}_1$ or CE_2 causes them.

AC CHARACTERISTICS—WRITE CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Symbol	Parameter	-25		-35		-45		Unit
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	25		35		45		ns
t_{CW}	Chip Enable Time to End of Write	18		25		33		ns
t_{AW}	Address Valid to End of Write	18		25		33		ns
t_{AS}	Address Set-up Time	0		0		0		ns
t_{WP}	Write Pulse Width	18		20		25		ns
t_{AH}	Address Hold Time	0		0		0		ns
t_{DW}	Data Valid to End of Write	13		15		20		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		10		14		18	ns
t_{OW}	Output Active from End of Write	3		5		5		ns

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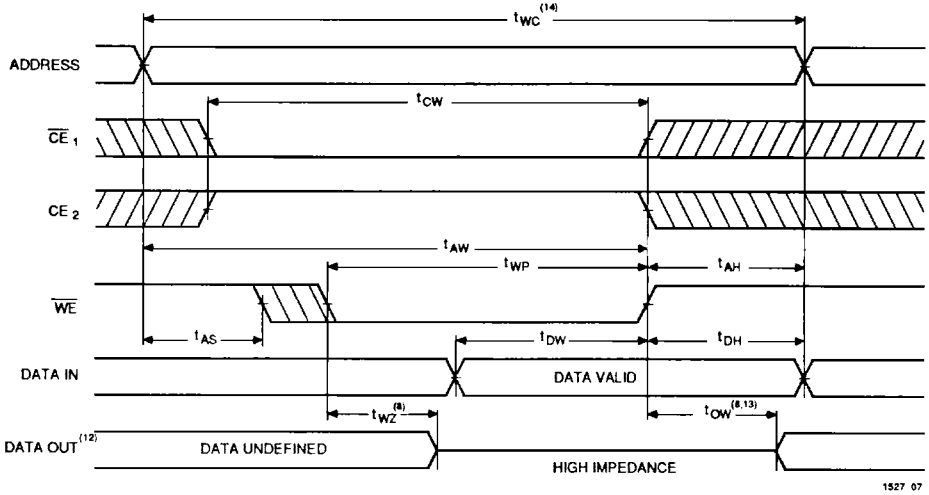
WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) [11]



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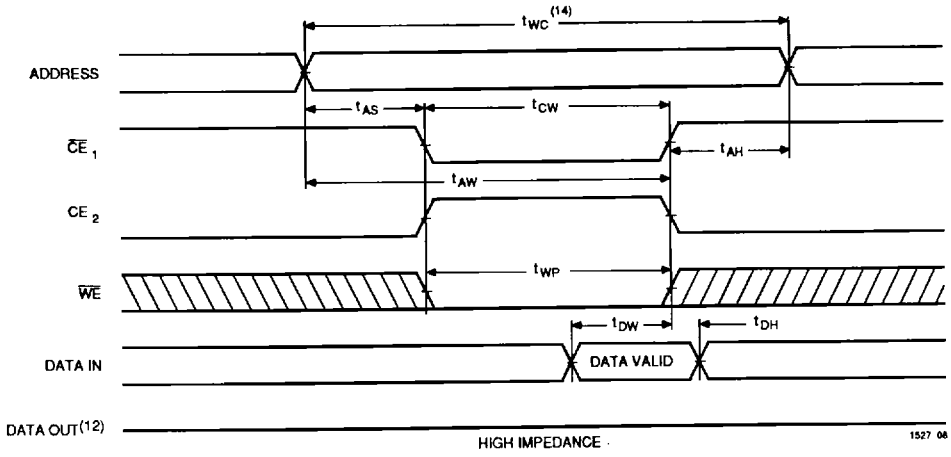
Notes:

11. $\overline{CE}$ and $\overline{WE}$ must be LOW, and CE_2 HIGH for WRITE cycle.
12. $\overline{OE}$ is LOW for this WRITE cycle to show t_{WZ} and t_{OW}.
13. If $\overline{CE}$ goes HIGH, or CE_2 goes LOW, simultaneously with $\overline{WE}$ HIGH, the output remains in a low impedance state.
14. Write Cycle Time is measured from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED) (11)



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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

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TRUTH TABLE

Mode	$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	L	X	X	High Z	Standby
D_{OUT} Disabled	L	H	H	H	High Z	Active
Read	L	H	L	H	D_{OUT}	Active
Write	L	H	X	L	High Z	Active

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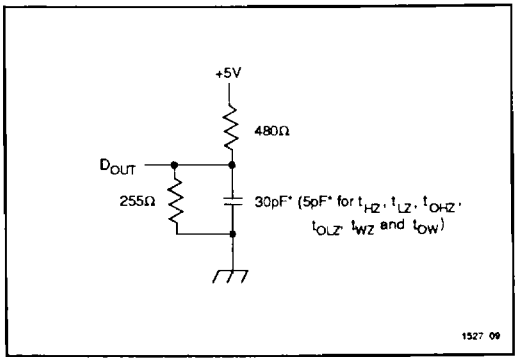


Figure 1. Output Load

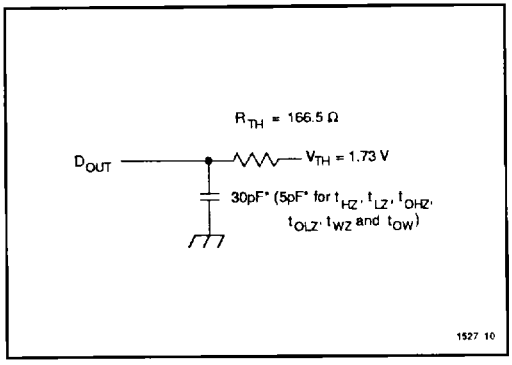


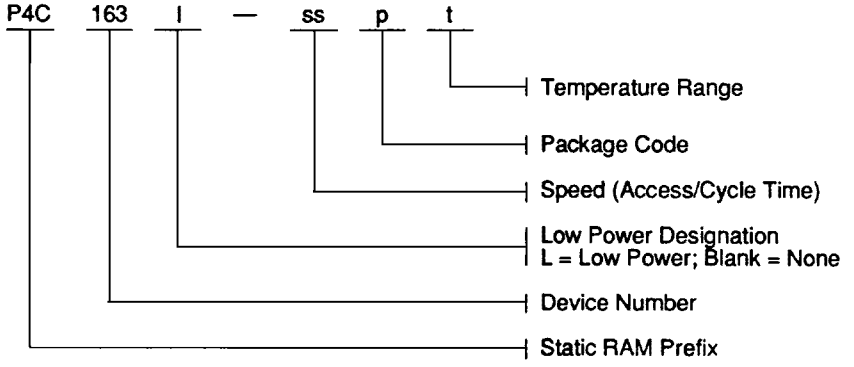
Figure 2. Thevenin Equivalent

* including scope and test fixture.

Note:
Because of the ultra-high speed of the P4C163/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{cc} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{cc} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

ORDERING INFORMATION

Performance Semiconductor's part numbering scheme is as follows.



I = Ultra-low standby power designator L, if available.
ss = Speed (access/cycle time in ns), e.g., 25, 35, 45.
p = Package code, i.e., P, J, D, L.
t = Temperature range, i.e., C, M, MB.

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PACKAGE SUFFIX

Package Suffix	Description
P	Plastic DIP, 300 mil wide standard
J	Plastic SOJ, 300 mil wide standard
C	Sidebrazed DIP, 300 mil wide
L	Leadless Chip Carrier (ceramic)
D	CERDIP, 300 mil wide standard

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TEMPERATURE RANGE SUFFIX

Temperature Range Suffix	Description
C	Commercial Temperature Range, 0°C to +70°C.
M	Military Temperature Range, −55°C to +125°C.
MB	Mil. Temp. with MIL-STD-883D Class B compliance

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SELECTION GUIDE

The P4C163/L is available in the following temperature, speed and package options. The P4C163L is only available in military temperature range with access times of 25 ns and slower. The P4C163L is available to Standardized Military Drawing 5962-88683. Check Mil-Bul-103 for current listing of part types.

Temp. Range	Package \ Speed	25	35	45
Com'l	Plastic DIP	−25PC	−35PC	N/A
	Plastic SOJ	−25JC	−35JC	N/A
	CER DIP	−25DC	−35DC	N/A
	LCC	−25LC	−35LC	N/A
Mil. Temp.	CERDIP	−25DM	−35DM	−45DM
	LCC	−25LM	−35LM	−45LM
Military Proc'd*	CERDIP	−25DMB	−35DMB	−45DMB
	LCC	−25LMB	−35LMB	−45LMB

* Military temperature range with MIL-STD-883 Revision D, Class B processing.
N/A = Not available

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