# 54ACT11240, 74ACT11240

## *Octal Buffers and Line Drivers With 3-State Outputs*

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices provide inverting outputs and symmetrical $\overline{G}$ (active-low output control) inputs. These devices feature high fan-out and improved fan-in.

The 54ACT11240 is characterized for operation over the full military temperature range of -55°C to 125°C while the 74ACT11240 is characterized for operation from -40°C to 85°C.

### Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

### Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

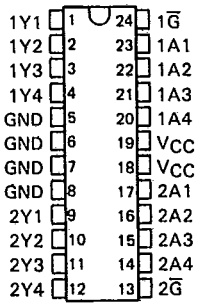
# 54ACT11240, 74ACT11240
# OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

T-52-07-00

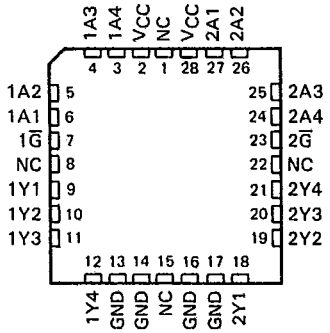
TI0072—D3410, MAY 1987—REVISED MARCH 1990

- Inputs are TTL-Voltage Compatible
- Flow-Through Architecture to Optimize PCB Layout
- Center-Pin $V_{CC}$ and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

**54ACT11240 ... JT PACKAGE**
**74ACT11240 ... DW OR NT PACKAGE**
**(TOP VIEW)**




**54ACT11240 ... FK PACKAGE**
**(TOP VIEW)**




NC—No internal connection

## description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices provide inverting outputs and symmetrical $\overline{G}$ (active-low output control) inputs. These devices feature high fan-out and improved fan-in.

The 54ACT11240 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11240 is characterized for operation from −40°C to 85°C.

**FUNCTION TABLE**
**(each gate)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{G}$ | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

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# OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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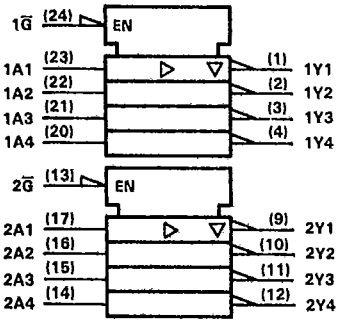
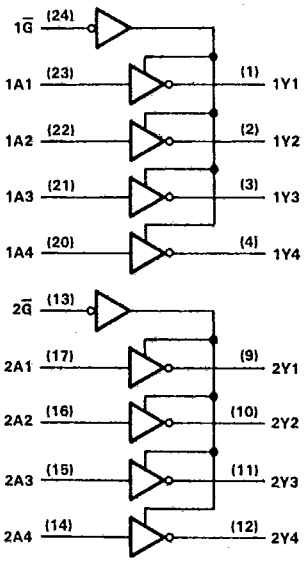
TI0072—D3410, MAY 1987—REVISED MARCH 1990

## logic symbol†




† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Note 1) ..... −0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CC}$) ..... ±20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±50 mA
Continuous current through $V_{CC}$ or GND pins ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## recommended operating conditions

| | | 54ACT11240 | | | 74ACT11240 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input voltage | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | | −24 | | | −24 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | | | 24 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | | 10 | 0 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | −55 | | 125 | −40 | | 85 | °C |

# 54ACT11240, 74ACT11240
# OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | 54ACT11240 | | 74ACT11240 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = −50 μA | 4.5 V | 4.4 | | | 4.4 | | 4.4 | | V |
| | | 5.5 V | 5.4 | | | 5.4 | | 5.4 | | |
| | $I_{OH}$ = −24 mA | 4.5 V | 3.94 | | | 3.7 | | 3.8 | | |
| | | 5.5 V | 4.94 | | | 4.7 | | 4.8 | | |
| | $I_{OH}$ = −50 mA† | 5.5 V | | | | 3.85 | | | | |
| | $I_{OH}$ = −75 mA† | 5.5 V | | | | | | 3.85 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 5.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 24 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | 5.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 50 mA† | 5.5 V | | | | | 1.65 | | | |
| | $I_{OL}$ = 75 mA† | 5.5 V | | | | | | | 1.65 | |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.5 | | ±10 | | ±5 | μA |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 8 | | 160 | | 80 | μA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at GND or $V_{CC}$ | 5.5 V | | | 0.9 | | 1 | | 1 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | | | | | | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | 5 V | | 10 | | | | | | pF |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## switching characteristics, $V_{CC}$ = 5 V ± 0.5 V (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | | 54ACT11240 | | 74ACT11240 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | 1.5 | 6.5 | 9.9 | 1.5 | 11.1 | 1.5 | 10.6 | ns |
| $t_{PHL}$ | | | 1.5 | 6 | 8 | 1.5 | 9.2 | 1.5 | 8.7 | |
| $t_{PZH}$ | $\overline{G}$ | Y | 1.5 | 7.5 | 11.7 | 1.5 | 13.1 | 1.5 | 12.5 | ns |
| $t_{PZL}$ | | | 1.5 | 7.3 | 11.5 | 1.5 | 12.8 | 1.5 | 12.3 | |
| $t_{PHZ}$ | $\overline{G}$ | Y | 1.5 | 7.3 | 9.4 | 1.5 | 10.3 | 1.5 | 10 | ns |
| $t_{PLZ}$ | | | 1.5 | 7.9 | 10.3 | 1.5 | 11.2 | 1.5 | 10.8 | |

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per gate | Outputs enabled | $C_L$ = 50 pF, f = 1 MHz | 47 | pF |
| | | Outputs disabled | | 13 | |



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## PARAMETER MEASUREMENT INFORMATION

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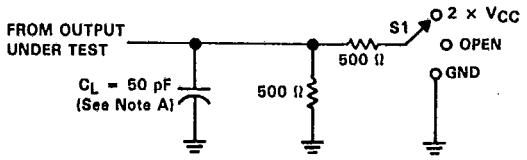
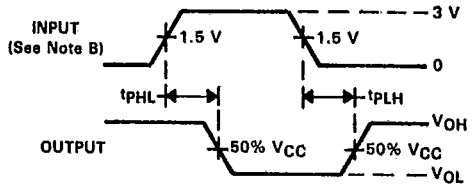
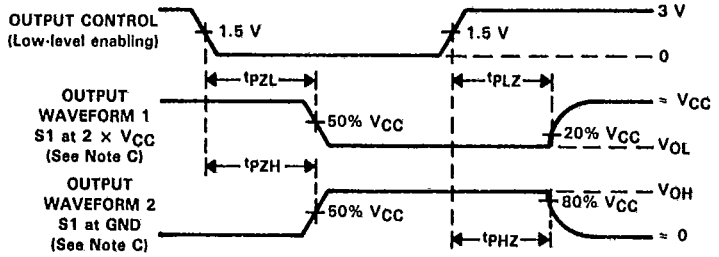



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | OPEN |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

LOAD CIRCUIT




PROPAGATION DELAY TIMES




ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

**FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS**