HARRIS

# HMM-11510

## GaAs MMIC Amplifier 7.5 – 15 GHz

**PRODUCT DATA SHEET** **June 1991**

### Features

- **On-Chip Source Resistor Network for Easy Bias Point Selection**
- **Directly Cascadable without Interstage Matching**
- **DC Blocking of Both RF Input and Output**
- **Ti/Pt/Au Metallization and Large Gate Cross Section for Enhanced Reliability**
- **Dielectric Scratch/Short Circuit Protection Improves Durability**
- **Individual Die Serialization Provides the *Ultimate* in Traceability**

### Description

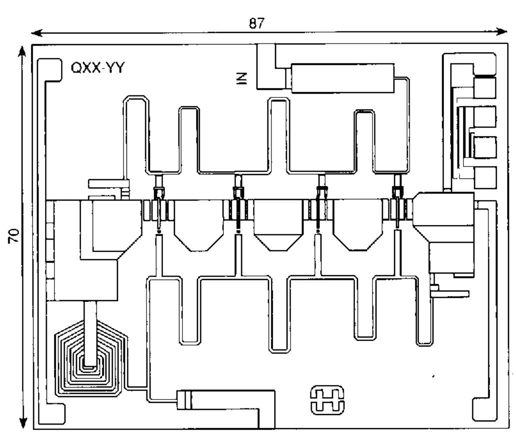
The HMM-11510 is a cascadable, broadband gain block designed for *gain* and *driver* circuit applications. A completely integrated amplifier, the HMM-11510 includes DC blocking of the RF input and output and an on-chip source bias resistor network.

A distributed amplifier design, the HMM-11510 is designed to replace MIC hybrids, while its small size and ruggedness offer distinct advantages in demanding military applications or, wherever space is at a premium.

Produced using the same mask set as the HMM-11810, HMM-11510 dice carry the 'HMM-11810' marking; but are distinguished from the HMM-11810 by separate RF qualification in addition to separate labels on the Gel-Pak shipping containers.

Standard wafer qualification includes 100 percent on-wafer DC probe, and visual inspection, as well as RF evaluation on a sample test basis.

### Device Outline

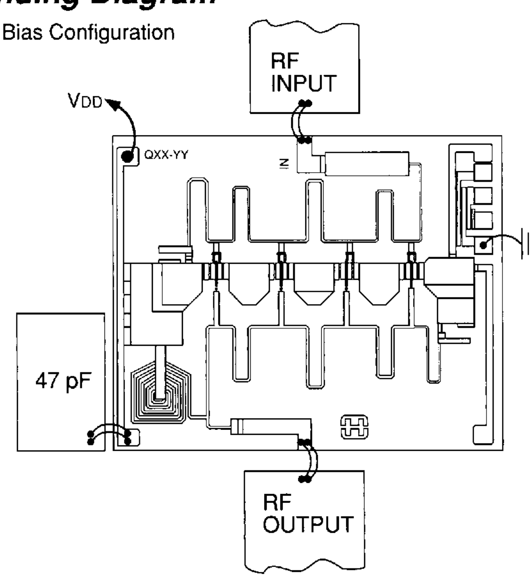



DIMENSIONS IN MILS

CHIP THICKNESS 5 MILS
Au BACKSIDE METALLIZATION

### Bonding Diagram

Gain Bias Configuration




# NEW PRODUCT INFORMATION

## Electrical Specifications at $T_A = 25°C$

| SYMBOL | PARAMETER | UNITS | MIN | TYP | MAX |
|---|---|---|---|---|---|
| Freq. | Operating Frequency Range | GHz | 7.5 | | 15 |
| $S_{21}$ | Small Signal Gain | dB | 4.5 | 6.0 | |
| ΔG | Gain Flatness (over full bandwidth) | dB | | ± 0.5 | ± 1.0 |
| $P_{1dB}$ | Output Power at 1dB Gain Compression | dBm | 15.0 | 16.0 | |
| VSWR | Input VSWR | | | 1.5:1 | 2.5:1 |
| VSWR | Output VSWR | | | 1.5:1 | 2.5:1 |
| NF | Noise Figure | dB | | 6.0 | |
| Conditions for above: $V_{DD}$ = 7.0 V, $I_{DD}$ = 100 mA (typical), Gain Bias Configuration | | | | | |
| $I_{DD}$ | Drain Current, $V_{DD}$ = 3.0 V, $R_S$ = 0 Ω | mA | 125 | 200 | 275 |

NOTES: 1. Typical RF performance and minimum limits are based on testing of sample units from each wafer on 50 Ω test carriers and do not include correction for tuner/fixture losses. DC min/max limits are guaranteed by 100% on-wafer probe testing.
2. Max $I_{DD}$ is the terminal current with $R_S$ = 0 Ω. This is the saturated source drain current ($I_{DSS}$) for the parallel combination of FETs in the circuit.

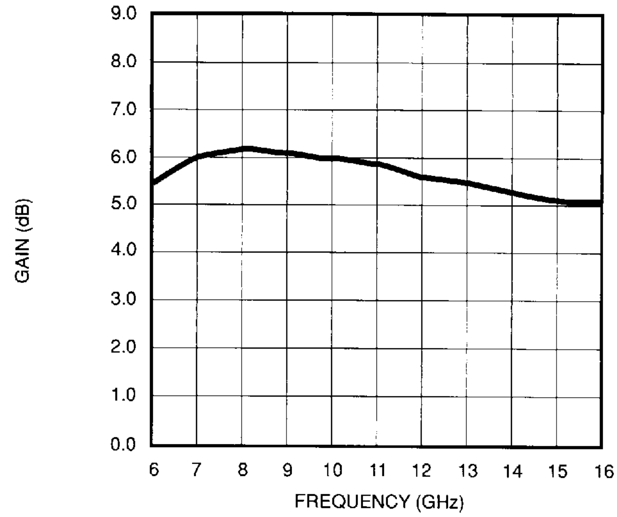
## Product Ratings

| SYMBOL | PARAMETER | MAXIMUM OPERATING CONDITIONS | |
|---|---|---|---|
| | | RECOMMENDED | ABSOLUTE |
| $V_{DD}$ | Supply Voltage | +8 V | +10 V |
| $T_{CH}$ | Channel Temperature, Operating | +180°C | +250°C |
| $T_{STG}$ | Storage Temperature | –65°C to +180°C | –65°C to +250°C |

NOTE: Permanent damage may result from operation at conditions beyond absolute maximum ratings.

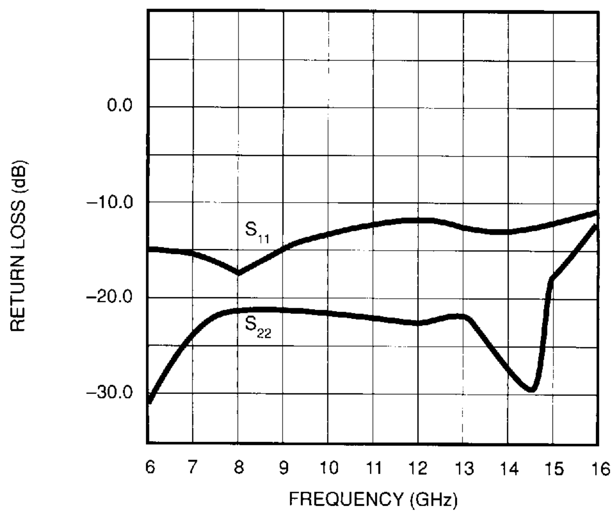
*Refer to Application Note 201 for die attachment and wire-bonding recommendations.*

## Gain Performance



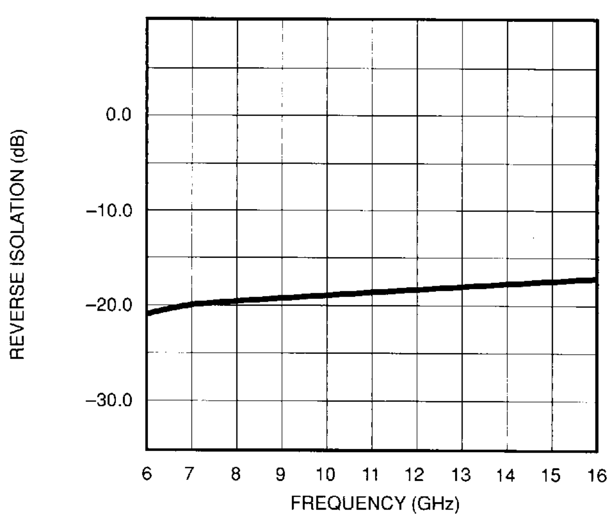

Gain ($S_{21}$) vs. Frequency. $V_{DD}$ = 7.0 V, Gain Bias.

## Return Loss



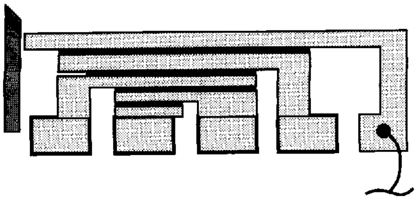

Input Return Loss ($S_{11}$) and Output Return Loss ($S_{22}$) vs. Frequency. $V_{DD}$ = 7.0 V, Gain Bias.

## Reverse Isolation

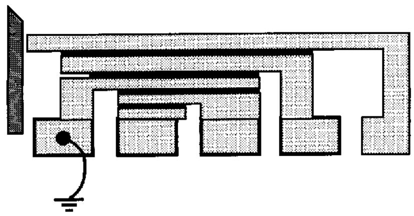



Reverse Isolation ($S_{12}$) vs. Frequency. $V_{DD}$ = 7.0 V, Gain Bias.

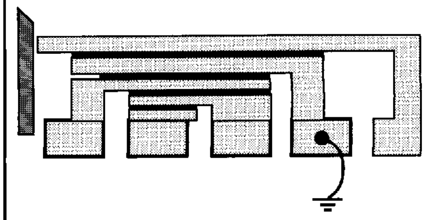
## Off-Chip Resistor



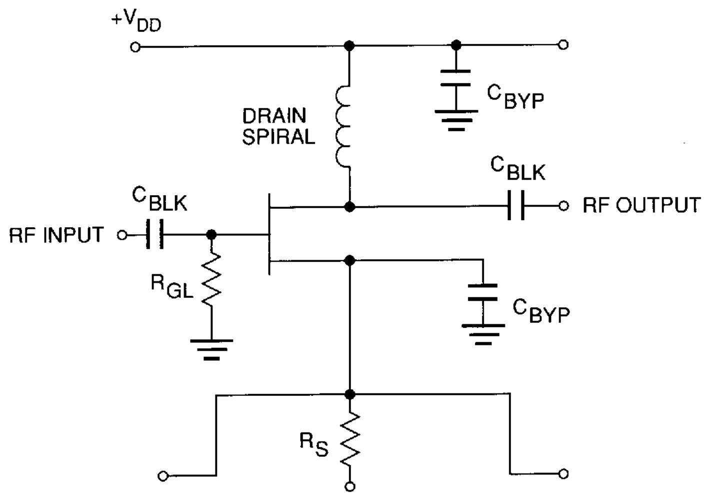
## Gain Bias



## Linear Power Bias



## Device Schematic




## Typical S-Parameters, $V_{DS}$ = 7.0 V, $I_{DD}$ = 100 mA (Gain Bias Configuration)

| FREQ (GHz) | $S_{11}$ | | $S_{21}$ | | $S_{12}$ | | $S_{22}$ | |
|---|---|---|---|---|---|---|---|---|
| | MAG | ANG | MAG | ANG | MAG | ANG | MAG | ANG |
| 4.0 | .103 | –86.6 | 1.691 | 138.8 | .046 | 52.5 | .260 | –170.6 |
| 5.0 | .193 | –120.1 | 1.811 | 105.8 | .047 | 29.1 | .122 | –167.7 |
| 6.0 | .179 | –138.9 | 1.908 | 71.9 | .077 | –6.2 | .075 | –150.0 |
| 6.5 | .182 | –137.3 | 1.973 | 58.6 | .073 | –20.5 | .065 | –112.5 |
| 7.0 | .170 | –153.8 | 2.032 | 42.8 | .080 | –32.5 | .090 | –108.8 |
| 7.5 | .144 | –178.6 | 2.043 | 26.2 | .086 | –45.9 | .100 | –111.7 |
| 8.0 | .127 | 149.6 | 2.049 | 10.3 | .090 | –58.5 | .102 | –115.3 |
| 8.5 | .167 | 135.0 | 2.008 | –2.1 | .110 | –70.9 | .113 | –124.1 |
| 9.0 | .200 | 96.1 | 2.059 | –18.1 | .108 | –88.8 | .092 | –132.4 |
| 9.5 | .217 | 72.6 | 2.025 | –32.6 | .112 | –100.8 | .080 | –135.0 |
| 10.0 | .232 | 49.9 | 2.034 | –47.3 | .115 | –111.8 | .070 | –136.0 |
| 11.0 | .256 | 0.6 | 1.996 | –77.8 | .121 | –132.9 | .061 | –126.0 |
| 12.0 | .253 | –46.0 | 1.945 | –106.0 | .131 | –156.9 | .059 | –108.3 |
| 13.0 | .226 | –104.3 | 1.964 | –136.3 | .144 | 175.6 | .056 | –111.1 |
| 14.0 | .211 | –179.6 | 1.863 | –168.6 | .156 | 146.8 | .035 | –116.2 |
| 15.0 | .219 | 112.3 | 1.840 | 161.0 | .159 | 113.6 | .032 | –86.8 |
| 16.0 | .256 | 42.4 | 1.847 | 124.9 | .165 | 76.4 | .066 | –70.7 |

NOTE: S-Parameters include bond wire inductances and are measured in a 50 Ω microstrip fixture.