Integrated Circuit Systems, Inc.

ICS91857

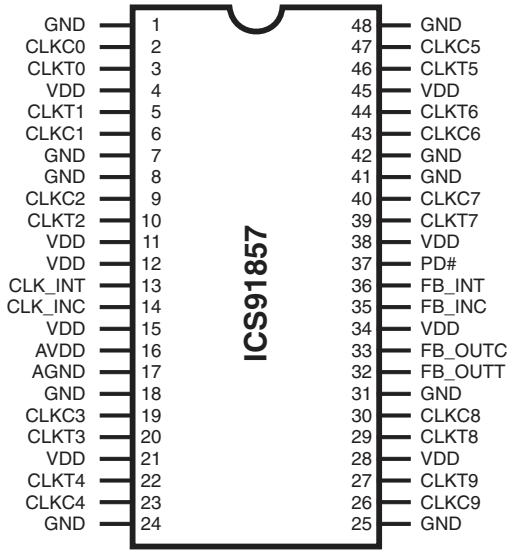
Value SSTL_2 Clock Driver (60MHz - 220MHz)

Recommended Application:
Zero delay board fan-out memory modules

Product Description/Features:
- Meets PC3200 specification for DDRI-400 support
- Low skew, low jitter PLL clock driver
- 1 to 10 differential clock distribution (SSTL_2)
- Feedback pins for input to output synchronization
- PD# for power management
- Spread Spectrum tolerant inputs
- Auto PD when input signal removed

Switching Characteristics:
- CYCLE - CYCLE jitter (>100MHz):<75ps
- OUTPUT - OUTPUT skew: <100ps

Pin Configuration

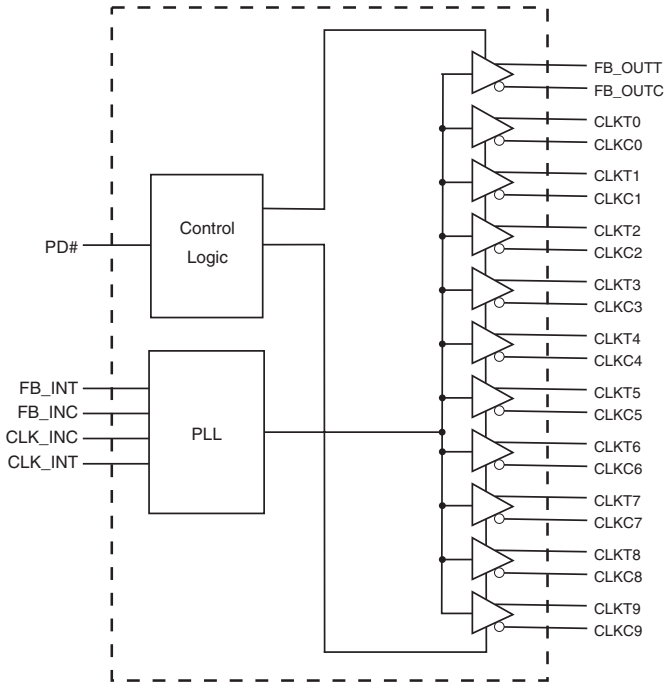


48-Pin TSSOP
6.10 mm. Body, 0.50 mm. pitch TSSOP

Functionality

INPUTS				OUTPUTS				PLL State
AVDD	PD#	CLK_INT	CLK_INC	CLKT	CLKC	FB_OUTT	FB_OUTC	
GND	H	L	H	L	H	L	H	Bypassed/off
GND	H	H	L	H	L	H	L	Bypassed/off
2.5V (nom)	L	L	H	Z	Z	Z	Z	off
2.5V (nom)	L	H	L	Z	Z	Z	Z	off
2.5V (nom)	H	L	H	L	H	L	H	on
2.5V (nom)	H	H	L	H	L	H	L	on
2.5V (nom)	X	<20MHz)(1)		Z	Z	Z	Z	off

Block Diagram



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
4, 11, 12, 15, 21, 28, 34, 38, 45,	VDD	PWR	Power supply 2.5V up to DDR 333. Power supply 2.6V for DDR-I at 400MHz.
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	GND	PWR	Ground
16	AVDD	PWR	Analog power supply, 2.5V up to DDR 333. Power supply 2.6V for DDR-I at 400MHz.
17	AGND	PWR	Analog ground.
27, 29, 39, 44, 46, 22, 20, 10, 5, 3	CLKT(9:0)	OUT	"True" Clock of differential pair outputs.
26, 30, 40, 43, 47, 23, 19, 9, 6, 2	CLKC(9:0)	OUT	"Complementary" clocks of differential pair outputs.
14	CLK_INC	IN	"Complementary" reference clock input
13	CLK_INT	IN	"True" reference clock input
33	FB_OUTC	OUT	"Complementary" Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INC.
32	FB_OUTT	OUT	"True" Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT.
36	FB_INT	IN	"True" Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error.
35	FB_INC	IN	"Complementary" Feedback input, provides signal to the internal PLL for synchronization with CLK_INC to eliminate phase error.
37	PD#	IN	Power Down. LVCMOS input

This PLL Clock Buffer is designed for a V_{DD} of 2.5V, an AV_{DD} of 2.5V and differential data input and output levels.

ICS91857 is a zero delay buffer that distributes a differential clock input pair (CLK_INC, CLK_INT) to ten differential pair of clock outputs (CLKT[0:9], CLKC[0:9]) and one differential pair feedback clock output (FB_OUT, FB_OUTC). The clock outputs are controlled by the input clocks (CLK_INC, CLK_INT), the feedback clocks (FB_INT, FB_INC) the 2.5-V LVCMOS input (PD#) and the Analog Power input (AV_{DD}). When input (PD#) is low while power is applied, the receivers are disabled, the PLL is turned off and the differential clock outputs are Tri-Stated. When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

When the input frequency is less than the operating frequency of the PLL, appproximately 20MHz, the device will enter a low power mode. An input frequency detection circuit on the differential inputs, independent from the input buffers, will detect the low frequency condition and perform the same low power features as when the (PD#) input is low. When the input frequency increases to greater than approximately 20 MHz, the PLL will be turned back on, the inputs and outputs will be enabled and PLL will obtain phase lock between the feedback clock pair (FB_INT, FB_INC) and the input clock pair (CLK_INC, CLK_INT).

The PLL in the **ICS91857** clock driver uses the input clocks (CLK_INC, CLK_INT) and the feedback clocks (FB_INT, FB_INC) provide high-performance, low-skew, low-jitter output differential clocks (CLKT [0:9], CLKC [0:9]). The ICS91857 is also able to track Spread Spectrum Clock (SSC) for reduced EMI.

ICS91857 is characterized for operation from 0°C to 70°C and will meet JEDEC Standard 82-1 and 82-1A for Registered DDR Clock Driver.

0494C—08/15/05

Absolute Maximum Ratings

Supply Voltage (VDD & AVDD) . . . . . -0.5V to 4.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} + 0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics for DDR200/266/333 - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage A_{VDD}, V_{DD} = 2.5V ± 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	$V_I = V_{DD}$ or GND	5			µA
Input Low Current	I_{IL}	$V_I = V_{DD}$ or GND			5	µA
Operating Supply Current	$I_{DD2.5}$	C_L = 0pf @ 200MHz		260		mA
	I_{DDPD}	C_L = 0pf			100	mA
Output High Current	I_{OH}	V_{DD} = 2.3V, V_{OUT} = 1V	-18	-32		mA
Output Low Current	I_{OL}	V_{DD} = 2.3V, V_{OUT} = 1.2V	26	35		mA
High Impedance Output Current	I_{OZ}	V_{DD}=2.7V, Vout=V_{DD} or GND			±10	mA
Input Clamp Voltage	V_{IK}	V_{DDQ} = 2.3V Iin = -18mA			-1.2	V
High-level output voltage	V_{OH}	V_{DD} = min to max, I_{OH} = -1 mA	V_{DDQ} - 0.1			V
		V_{DDQ} = 2.3V, I_{OH} = -12 mA	1.7			V
Low-level output voltage	V_{OL}	V_{DD} = min to max I_{OL}=1 mA			0.1	V
		V_{DDQ} = 2.3V I_{OH}=12 mA			0.6	V
Input Capacitance[1]	C_{IN}	V_I = GND or V_{DD}		3		pF
Output Capacitance[1]	C_{OUT}	V_{OUT} = GND or V_{DD}		3		pF

[1]Guaranteed by design at 170MHz, not 100% tested in production.

Electrical Characteristics for DDRI-400 - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage A_{VDD}, V_{DD} = 2.6V ± 0.1V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	$V_I = V_{DD}$ or GND	5			µA
Input Low Current	I_{IL}	$V_I = V_{DD}$ or GND			5	µA
Operating Supply Current	$I_{DD2.5}$	C_L = 0pf @ 200MHz		260		mA
	I_{DDPD}	C_L = 0pf			100	mA
Output High Current	I_{OH}	V_{DD} = 2.3V, V_{OUT} = 1V	-18	-32		mA
Output Low Current	I_{OL}	V_{DD} = 2.3V, V_{OUT} = 1.2V	26	35		mA
High Impedance Output Current	I_{OZ}	V_{DD}=2.7V, Vout=V_{DD} or GND			±10	mA
Input Clamp Voltage	V_{IK}	V_{DDQ} = 2.3V Iin = -18mA			-1.2	V
High-level output voltage	V_{OH}	V_{DD} = min to max, I_{OH} = -1 mA	V_{DDQ} - 0.1			V
		V_{DDQ} = 2.3V, I_{OH} = -12 mA	1.7			V
Low-level output voltage	V_{OL}	V_{DD} = min to max I_{OL}=1 mA			0.1	V
		V_{DDQ} = 2.3V I_{OH}=12 mA			0.6	V
Input Capacitance[1]	C_{IN}	V_I = GND or V_{DD}		3		pF
Output Capacitance[1]	C_{OUT}	V_{OUT} = GND or V_{DD}		3		pF

[1]Guaranteed by design at 220MHz, not 100% tested in production.

Recommended Operating Condition for DDR200/266/333 (see note1)

T_A = 0 - 85°C; Supply Voltage AVDD, VDD = 2.5V ± 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DDQ}, A_{VDD}		2.3		2.7	V
Low level input voltage	V_{IL}	CLKT, CLKC, FB_INC			V_{DDQ}/2 - 0.18	V
		PD#	-0.3		0.7	V
High level input voltage	V_{IH}	CLKT, CLKC, FB_INC	V_{DDQ}/2 + 0.18			V
		PD#	1.7		V_{DDQ} + 0.6	V
DC input signal voltage (note 2)			-0.3		V_{DDQ}	V
Differential input signal voltage (note 3)	V_{ID}	DC - CLKT, FB_INT	0.36		V_{DDQ} + 0.6	V
		AC - CLKT, FB_INT	0.7		V_{DDQ} + 0.6	V
Output differential cross-voltage (note 4)	V_{OX}		V_{DDQ}/2 - 0.15		V_{DDQ}/2 + 0.15	V
Input differential cross-voltage (note 4)	V_{IX}		V_{DDQ}/2 - 0.2		V_{DDQ}/2 + 0.2	V
High level output current	I_{OH}				0.12	mA
Low level output current	I_{OL}				12	mA
Input slew rate	S_R		1		4	V/ns
Operating free-air temperature	T_A		0		70	°C

Notes:

1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC execution of differential input.
3. Differential inputs signal voltages specifies the differential voltage [VTR-VCP] required for switching, where VT is the true input level and VCP is the complementary input level.
4. Differential cross-point voltage is expected to track variations of V_{CC} and is the voltage at which the differential signal must be crossing.

Recommended Operating Condition for DDRI-400 (see note1)

T_A = 0 - 70°C; Supply Voltage AVDD, VDD = 2.6V ± 0.1V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DDQ}, A_{VDD}		2.5	2.6	2.7	V
Low level input voltage	V_{IL}	CLKT, CLKC, FB_INC			V_{DDQ}/2 - 0.18	V
		PD#	-0.3		0.7	V
High level input voltage	V_{IH}	CLKT, CLKC, FB_INC	V_{DDQ}/2 + 0.18			V
		PD#	1.7		V_{DDQ} + 0.3	V
DC input signal voltage (note 2)			-0.3		V_{DDQ}	V
Differential input signal voltage (note 3)	V_{ID}	DC - CLKT, FB_INT	0.36		V_{DDQ} + 0.6	V
		AC - CLKT, FB_INT	0.7		V_{DDQ} + 0.6	V
Output differential cross-voltage (note 4)	V_{OX}		V_{DDQ}/2 - 0.15		V_{DDQ}/2 + 0.15	V
Input differential cross-voltage (note 4)	V_{IX}		V_{DDQ}/2 - 0.2		V_{DDQ}/2 + 0.2	V
High level output current	I_{OH}				12	mA
Low level output current	I_{OL}				-12	mA
Input slew rate	S_R		1		4	V/ns
Operating free-air temperature	T_A		0		70	°C

Notes:
1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC execution of differential input.
3. Differential inputs signal voltages specifies the differential voltage [VTR-VCP] required for switching, where VT is the true input level and VCP is the complementary input level.
4. Differential cross-point voltage is expected to track variations of V_{CC} and is the voltage at which the differential signal must be crossing.

Timing Requirements for DDR200/266/333

T_A = 0 - 70°C; Supply Voltage A_{VDD}, V_{DD} = 2.5V ± 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Max clock frequency	$freq_{op}$	2.5V ± 0.2V @ 25°C	60	170	MHz
Application Frequency Range	$freq_{App}$	2.5V ± 0.2V @ 25°C	95	170	MHz
Input clock duty cycle	d_{tin}		40	60	%
CLK stabilization	T_{STAB}			100	µs

Timing Requirements for DDRI-400

T_A = 0 - 70°C; Supply Voltage A_{VDD}, V_{DD} = 2.6V ± 0.1V

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Max clock frequency	$freq_{op}$	2.6V ± 0.1V	60	230	MHz
Application Frequency Range	$freq_{App}$	2.6V ± 0.1V	95	220	MHz
Input clock duty cycle	d_{tin}		40	60	%
CLK stabilization	T_{STAB}			100	µs

Switching Characteristics for DDR200/266/333

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Low-to high level propagation delay time	t_{PLH}[1]	CLK_IN to any output		3.5		ns
High-to low level propagation delay time	t_{PLL}[1]	CLK_IN to any output		3.5		ns
Output enable time	t_{EN}	PD# to any output		3		ns
Output disable time	t_{dis}	PD# to any output		3		ns
Period jitter	$T_{jit\ (per)}$	100 - 200 MHz	-75		75	ps
Half-period jitter	$t_{(jit\_hper)}$	100 - 200 MHz	-75		75	
Input clock slew rate	$t_{(sir\_I)}$		1		4	V/ns
Output clock slew rate	$t_{(sl\_o)}$		1		2	V/ns
Cycle to Cycle Jitter[1]	T_{cyc}-T_{cyc}	100 - 200 MHz	-75		75	ps
Static Phase Offset	$t_{(spo)}$[3]		-50	0	50	ps
Output to Output Skew	T_{skew}				100	ps
Pulse skew	T_{skewp}				100	ps

Notes:

1. Refers to transition on noninverting output in PLL bypass mode.
2. Switching characteristics guaranteed for application frequency range.
3. Static phase offset shifted by design.

Switching Characteristics for DDRI-400

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Low-to high level propagation delay time	t_{PLH}[1]	CLK_IN to any output		3.5		ns
High-to low level propagation delay time	t_{PLL}[1]	CLK_IN to any output		3.5		ns
Output enable time	t_{EN}	PD# to any output		3		ns
Output disable time	t_{dis}	PD# to any output		3		ns
Period jitter	$T_{jit\ (per)}$	100 - 200 MHz	-50		50	ps
Half-period jitter	$t_{(jit\_hper)}$	100 - 200 MHz	-75		75	
Input clock slew rate	$t_{(sir\_I)}$		1		4	V/ns
Output clock slew rate	$t_{(sl\_o)}$		1		2	V/ns
Cycle to Cycle Jitter[1]	T_{cyc}-T_{cyc}	100 - 200 MHz	-75		75	ps
Static Phase Offset	$t_{(spo)}$[3]		-50	0	50	ps
Output to Output Skew	T_{skew}				75	ps
Pulse skew	T_{skewp}				100	ps

Notes:
1. Refers to transition on noninverting output in PLL bypass mode.
2. Switching characteristics guaranteed for application frequency range.
3. Static phase offset shifted by design.

Parameter Measurement Information

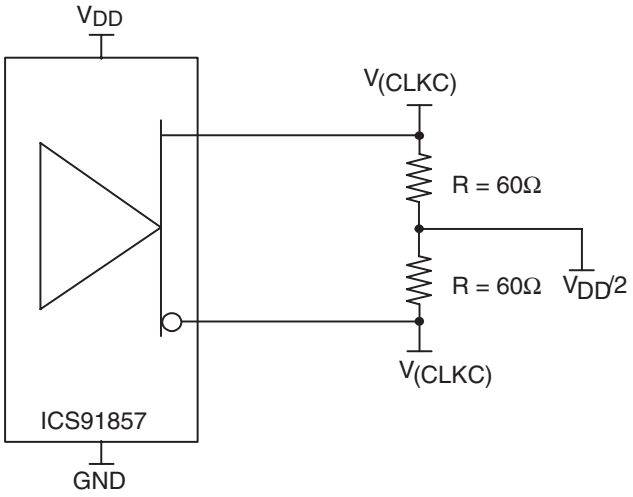
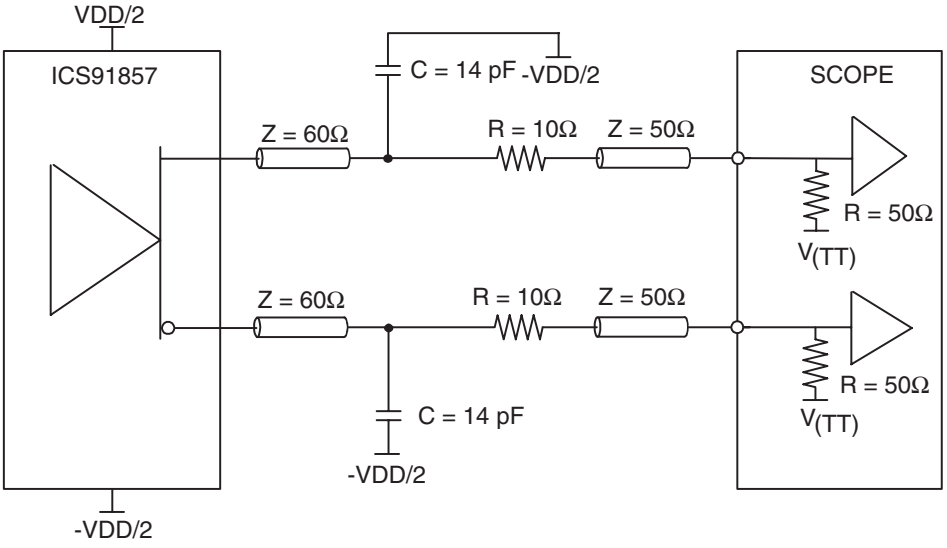
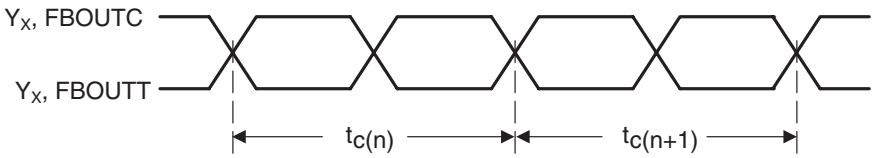


Figure 1. IBIS Model Output Load



NOTE: $V_{(TT)} = GND$

Figure 2. Output Load Test Circuit



$$t_{jit(cc)} = t_{c(n)} \pm t_{c(n+1)}$$

Figure 3. Cycle-to-Cycle Jitter

Parameter Measurement Information

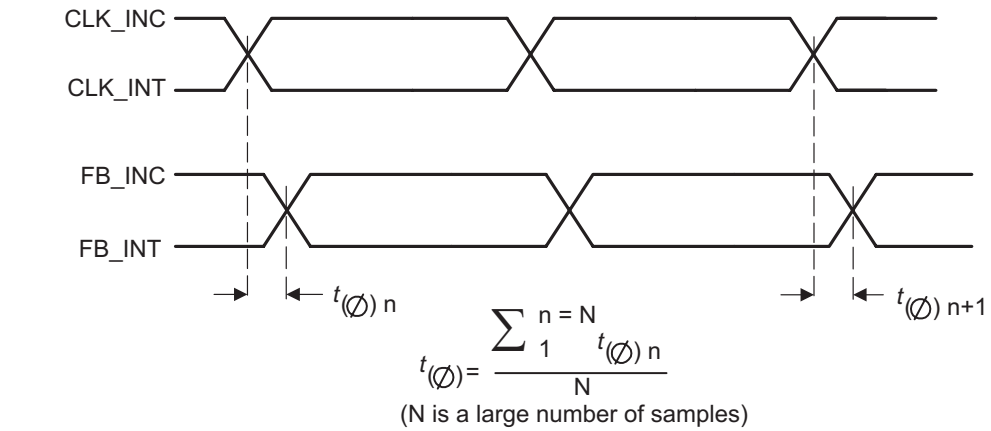


Figure 4. Static Phase Offset

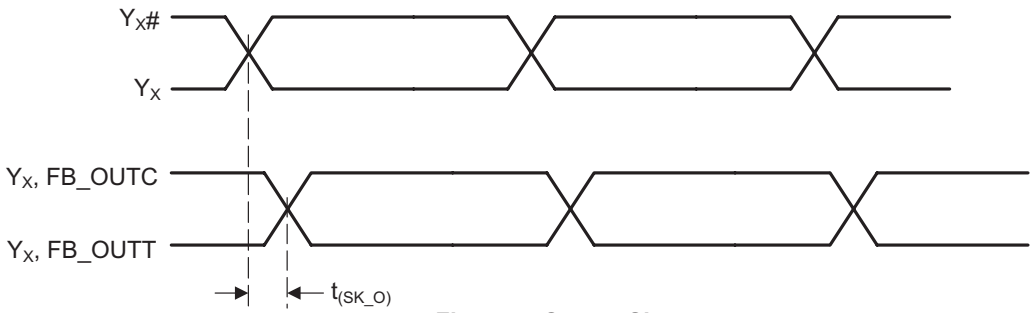


Figure 5. Output Skew

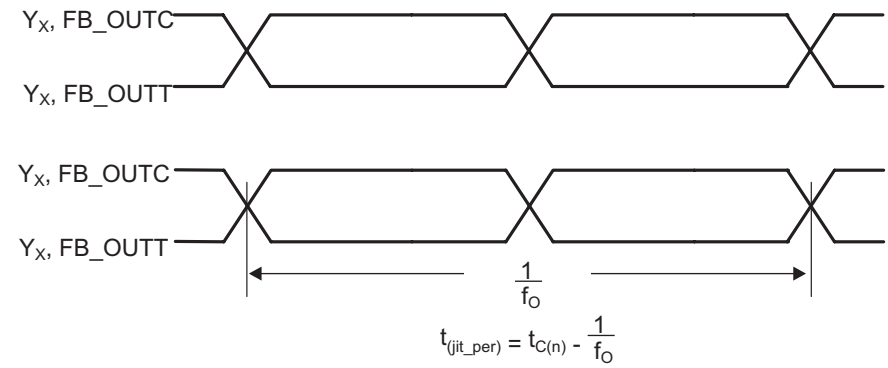


Figure 6. Period Jitter

Parameter Measurement Information

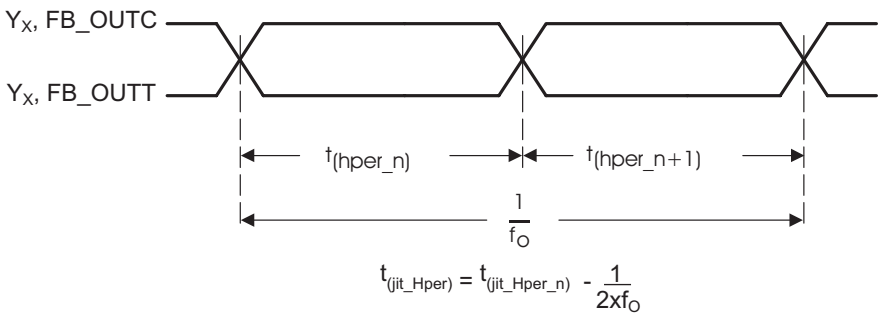


Figure 7. Half-Period Jitter

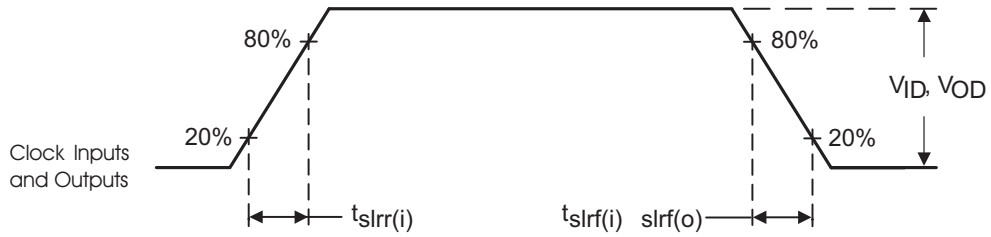
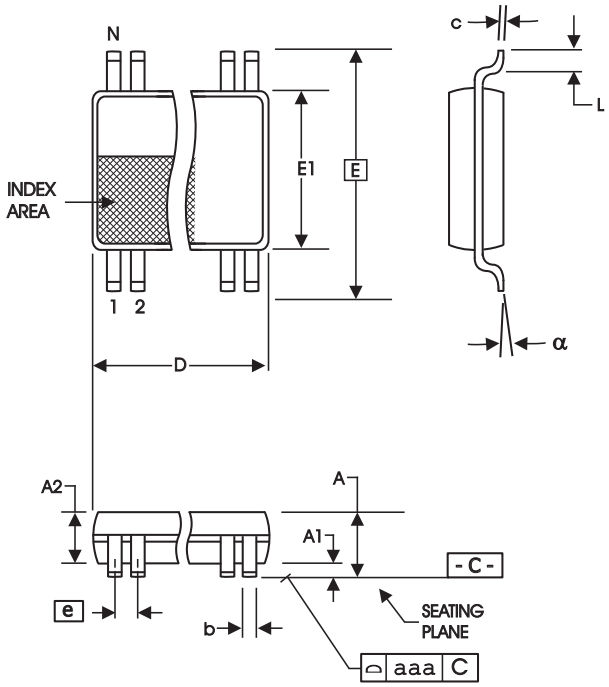


Figure 8. Input and Output Slew Rates



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

6.10 mm. Body, 0.50 mm. pitch TSSOP

(240 mil) (20 mil)

Ordering Information

ICS91857yGLFT

Example:

ICS XXXX y G - PPP - LF - T

Designation for tape and reel packaging

RoHS Compliant (Optional)

Pattern Number

Package Type
G = TSSOP

Revision Designator (will not correlate with datasheet revision)

Device Type

Prefix
ICS = Standard Device

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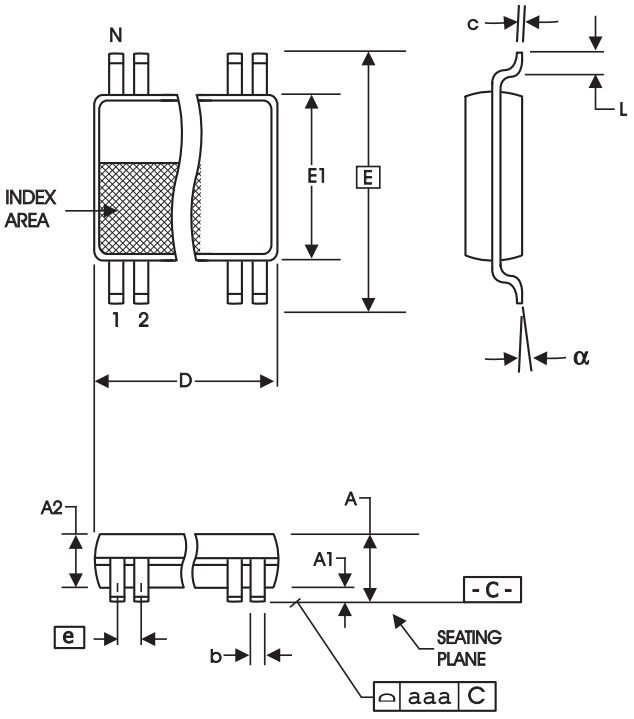

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.13	0.23	.005	.009
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.40 BASIC		0.016 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.08	--	.003

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	9.60	9.80	.378	.386

Reference Doc.: JEDEC Publication 95, MO-153

10-0037

4.40 mm. Body, 0.40 mm. pitch TSSOP (TVSOP)

(173 mil) (16 mil)

Ordering Information

ICS91857yLLFT

Example:

ICS XXXX y L - PPP - LF -T

Designation for tape and reel packaging

RoHS Compliant (Optional)

Pattern Number

Package Type
L = TSSOP (TVSOP)

Revision Designator (will not correlate with datasheet revision)

Device Type

Prefix
ICS = Standard Device

0494C—08/15/05

Revision History

Rev.	Issue Date	Description	Page #
C	8/15/2005	Added LF Ordering Information.	12-13

91857A (DDR PLL)

Description
2.5 Wide Range Frequency Clock Driver
Market Group
DIMM
Additional Info
• Meets PC3200 specification for DDRI-400 support • Low skew, low jitter PLL clock driver • 1 to 10 differential clock distribution (SSTL_2) • Feedback pins for input to output synchronization • PD# for power management • Spread Spectrum tolerant inputs • Auto PD when input signal removed

Related Orderable Parts

Attributes	91857AG	91857AGLF	91857AGLFT	91857AGT	91857AL	91857ALT
Package	TSSOP 48 (PA48)	TSSOP 48 (PAG48)	TSSOP 48 (PAG48)	TSSOP 48 (PA48)	TVSOP 48 (PF48)	TVSOP 48 (PF48)
Speed	NA	NA	NA	NA	NA	NA
Temperature	C	C	C	C	C	C
Voltage	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
Status	Active	Active	Active	Active	Active	Active
Sample	No	No	No	No	No	No
Minimum Order Quantity	380	380	1000	1000	384	1000
Factory Order Increment	38	38	1000	1000	48	1000

Related Documents

Type	Title	Size	Revision Date
Datasheet	91857A	134 KB	03/22/2006
Product Change Notice	PCN#: TB-0510-05 New Shipping Tube for TSSOP/TVSOP/TSSOP Exposed	202 KB	12/13/2005

Node: www.idt.com