# TC74LCX138F/FN/FS

TENTATIVE DATA

## LOW VOLTAGE 3-TO-8 LINE DECODER WITH 5V TOLERANT INPUTS AND OUTPUTS

The TC74LCX138 is a high performance CMOS 3-to-8 DECODER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3V) $V_{CC}$ applications, but it could be used to interface to 5V supply environment for inputs.

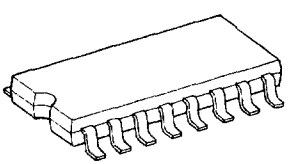
When the device is enabled, 3 Binary Select inputs (A, B and C) determine which one of the outputs ($\overline{Y}0$-$\overline{Y}7$) will go low.

When enable input G1 is held low or either $\overline{G}2A$ or $\overline{G}2B$ is held high, decoding function is inhibited and all outputs go high.

G1, $\overline{G}2A$, and $\overline{G}2B$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

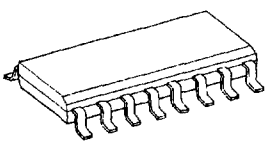
All inputs are equipped with protection circuits against static discharge.

TC74LCX138F



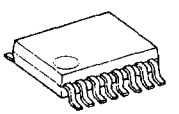
SOP16-P-300

TC74LCX138FN



SOL16-P-150

TC74LCX138FS



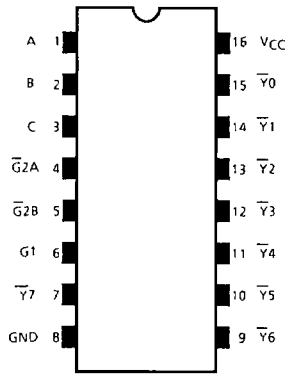
SSOP16-P-225B

Weight SOP16-P-300 : 0.18g (Typ.)
SOL16-P-150 : 0.12g (Typ.)
SSOP16-P-225B : 0.07g (Typ.)

### FEATURES

- Low voltage operation : $V_{CC} = 2.0 \sim 3.6V$
- High speed operation : $t_{pd} = 6.0ns$ (Max.) ($V_{CC} = 3.0 \sim 3.6V$)
- Output current : $|I_{OH}| / I_{OL} = 24mA$ (Min.) ($V_{CC} = 3.0V$)
- Latch-up performance : $\pm 500mA$
- Available in JEDEC SOP, EIAJ SOP and SSOP
- Power down protection is provided on all inputs and outputs.
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 138 type.

PIN ASSIGNMENT



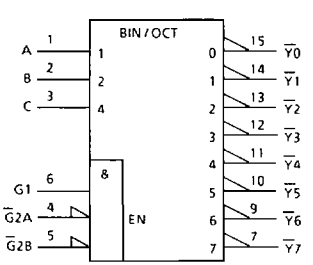

(TOP VIEW)

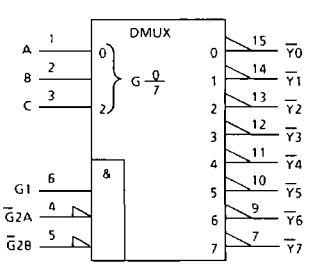
TRUTH TABLE

| INPUTS | | | | | | OUTPUTS | | | | | | | | SELECTED OUTPUT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ENABLE | | | SELECT | | | | | | | | | | | |
| G1 | $\overline{G2A}$ | $\overline{G2B}$ | C | B | A | $\overline{Y0}$ | $\overline{Y1}$ | $\overline{Y2}$ | $\overline{Y3}$ | $\overline{Y4}$ | $\overline{Y5}$ | $\overline{Y6}$ | $\overline{Y7}$ | |
| L | X | X | X | X | X | H | H | H | H | H | H | H | H | NONE |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H | NONE |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H | NONE |
| H | L | L | L | L | L | L | H | H | H | H | H | H | H | $\overline{Y0}$ |
| H | L | L | L | L | H | H | L | H | H | H | H | H | H | $\overline{Y1}$ |
| H | L | L | L | H | L | H | H | L | H | H | H | H | H | $\overline{Y2}$ |
| H | L | L | L | H | H | H | H | H | L | H | H | H | H | $\overline{Y3}$ |
| H | L | L | H | L | L | H | H | H | H | L | H | H | H | $\overline{Y4}$ |
| H | L | L | H | L | H | H | H | H | H | H | L | H | H | $\overline{Y5}$ |
| H | L | L | H | H | L | H | H | H | H | H | H | L | H | $\overline{Y6}$ |
| H | L | L | H | H | H | H | H | H | H | H | H | H | L | $\overline{Y7}$ |

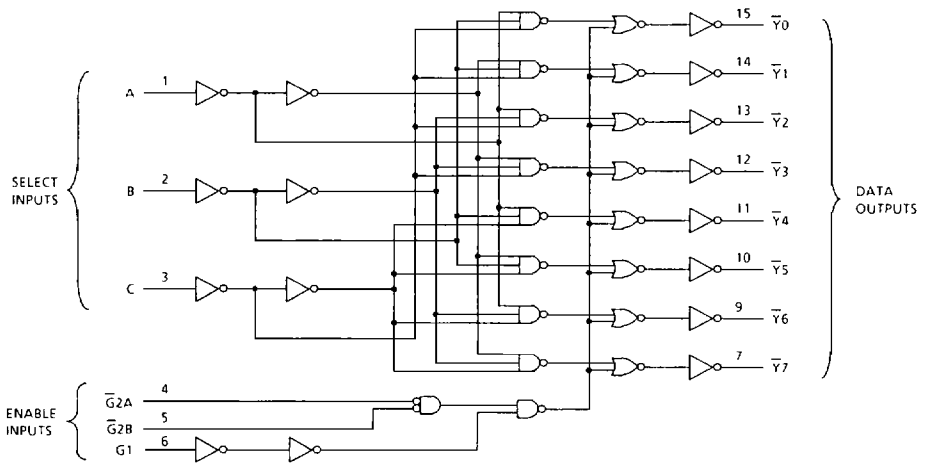
X : Don't Care

IEC LOGIC SYMBOL



SYSTEM DIAGRAM




MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Supply Voltage Range | $V_{CC}$ | −0.5~7.0 | V |
| DC Input Voltage | $V_{IN}$ | −0.5~7.0 | V |
| DC Output Voltage | $V_{OUT}$ | −0.5~7.0 (Note 1) | V |
| | | −0.5~$V_{CC}$ + 0.5 (Note 2) | |
| Input Diode Current | $I_{IK}$ | −50 | mA |
| Output Diode Current | $I_{OK}$ | ±50 (Note 3) | mA |
| DC Output Current | $I_{OUT}$ | ±50 | mA |
| Power Dissipation | $P_D$ | 180 | mW |
| DC $V_{CC}$/Ground Current | $I_{CC}$ / $I_{GND}$ | ±100 | mA |
| Storage Temperature | $T_{stg}$ | −65~150 | °C |

(Note 1) VCC = 0V
(Note 2) High or Low State. $I_{OUT}$ absolute maximum rating must be observed.
(Note 3) $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 2.0~3.6 | V |
| | | 1.5~3.6 (Note 4) | |
| Input Voltage | $V_{IN}$ | 0~5.5 | V |
| Output Voltage | $V_{OUT}$ | 0~5.5 (Note 5) | V |
| | | 0~ $V_{CC}$ (Note 6) | |
| Output Current | $I_{OH}$ / $I_{OL}$ | ± 24 (Note 7) | mA |
| | | ± 12 (Note 8) | |
| Operating Temperature | $T_{opr}$ | − 40~85 | °C |
| Input Rise And Fall Time | dt / dv | 0~10 (Note 9) | ns / V |

(Note 4) Data Retention Only
(Note 5) VCC = 0V
(Note 6) High or Low State
(Note 7) $V_{CC}$ = 3.0~3.6V
(Note 8) $V_{CC}$ = 2.7~3.0V
(Note 9) $V_{IN}$ = 0.8~2.0V, $V_{CC}$ = 3.0V

ELECTRICAL CHARACTERISTICS
DC characteristics (Ta = − 40~85°C)

| PARAMETER | | SYMBOL | TEST CONDITION | | $V_{CC}$ (V) | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| Input Voltage | "H" Level | $V_{IH}$ | | | 2.7~3.6 | 2.0 | — | V |
| | "L" Level | $V_{IL}$ | | | 2.7~3.6 | — | 0.8 | |
| Output Voltage | "H" Level | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = − 100μA | 2.7~3.6 | $V_{CC}$ − 0.2 | — | V |
| | | | | $I_{OH}$ = − 12mA | 2.7 | 2.2 | — | |
| | | | | $I_{OH}$ = − 18mA | 3.0 | 2.4 | — | |
| | | | | $I_{OH}$ = − 24mA | 3.0 | 2.2 | — | |
| | "L" Level | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 100μA | 2.7~3.6 | — | 0.2 | |
| | | | | $I_{OL}$ = 12mA | 2.7 | — | 0.4 | |
| | | | | $I_{OL}$ = 16mA | 3.0 | — | 0.4 | |
| | | | | $I_{OL}$ = 24mA | 3.0 | — | 0.55 | |
| Input Leakage Current | | $I_{IN}$ | $V_{IN}$ = 0~5.5V | | 2.7~3.6 | — | ± 5.0 | μA |
| Power Off Leakage Cuurent | | $I_{OFF}$ | $V_{IN}$ / $V_{OUT}$ = 5.5V | | 0 | — | 10.0 | μA |
| Quiescent Supply Current | | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 2.7~3.6 | — | 10.0 | μA |
| | | | $V_{IN}$ / $V_{OUT}$ = 3.6~5.5V | | 2.7~3.6 | — | ± 10.0 | |
| Increase In $I_{CC}$ Per Input | | $\Delta I_{CC}$ | $V_{IH}$ = $V_{CC}$ − 0.6V | | 2.7~3.6 | — | 500 | μA |

AC characteristics (Ta = −40~85°C)

| PARAMETER | SYMBOL | TEST CONDITION | $V_{CC}$ (V) | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Propagation Delay Time (A, B, C-$\overline{Y}$) | $t_{pLH}$ $t_{pHL}$ | (Fig.1, 2) | 2.7 | — | 7.0 | ns |
| | | | 3.3 ± 0.3 | 1.5 | 6.0 | |
| Propagation Delay Time (G1-$\overline{Y}$) | $t_{pLH}$ $t_{pHL}$ | (Fig.1, 2) | 2.7 | — | 7.5 | ns |
| | | | 3.3 ± 0.3 | 1.5 | 6.5 | |
| Propagation Delay Time ($\overline{G2}$-$\overline{Y}$) | $t_{pLH}$ $t_{pHL}$ | (Fig.1, 2) | 2.7 | — | 7.0 | ns |
| | | | 3.3 ± 0.3 | 1.5 | 6.0 | |
| Output To Output Skew | $t_{osLH}$ $t_{osHL}$ | (Note 10) | 2.7 | — | — | ns |
| | | | 3.3 ± 0.3 | — | 1.0 | |

(Note 10) Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

**CAPACITIVE CHARACTERISTICS** (Ta = 25°C)

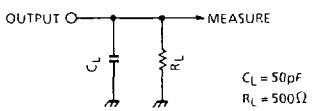
| PARAMETER | SYMBOL | TEST CONDITION | $V_{CC}$ (V) | TYP. | UNIT |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | — | 3.3 | TBD | pF |
| Power Dissipation Capacitance | $C_{PD}$ | $f_{IN}$ = 10MHz (Note 11) | 3.3 | TBD | pF |

(Note 11) $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :

$$I_{CC (opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TEST CIRCUIT

Fig.1




AC WAVEFORM

Fig.2 $t_{pLH}$, $t_{pHL}$