

54ABT/74ABT273C

Octal D-Type Flip-Flop

General Description

The 'ABT273C has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the \overline{MR} input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

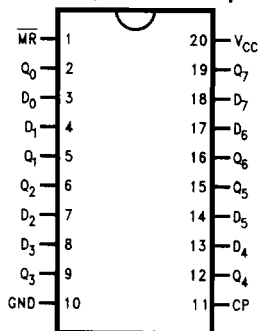
Features

- Eight edge-triggered D flip-flops
- Buffered common clock
- Buffered, asynchronous Master Reset
- See 'ABT377C for clock enable version
- See 'ABT373C for transparent latch version
- See 'ABT374C for TRI-STATE® version
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed 2000V minimum ESD protection
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Disable time less than enable time to avoid bus contention

Ordering Code: See Section 10

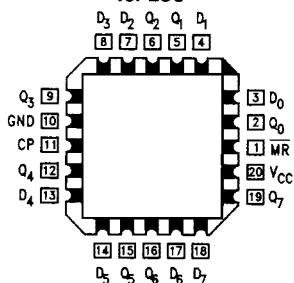
Connection Diagrams

**Pin Assignment for
DIP, SOIC, SSOP and Flatpak**



TL/F/11549-1

**Pin Assignment
for LCC**



TL/F/11549-2

Pin Names	Description
D ₀ -D ₇	Data Inputs
\overline{MR}	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
Q ₀ -Q ₇	Data Outputs

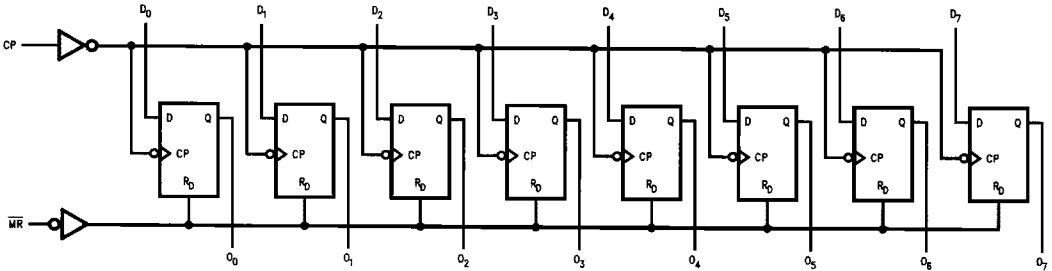
Truth Table

Mode Select-Function Table

Operating Mode	Inputs			Output
	MR	CP	D _n	Q _n
Reset (Clear)	L	X	X	L
Load "1"	H	↗	h	H
Load "0"	H	↗	l	L

H = HIGH Voltage Level steady state
 h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
 L = LOW Voltage Level steady state
 l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
 X = Immaterial
 ↗ = LOW-to-HIGH clock transition

Logic Diagram



TL/F/11549-3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State in the HIGH State	-0.5V to +4.75V -0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

ESD Last Passing Voltage (Min)	2000V
DC Latchup Source Current	-500 mA
Over Voltage Latchup	V _{CC} + 4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	-40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT273C			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54ABT/74ABT 54ABT 74ABT	2.5 2.0 2.0		V	Min	I _{OH} = -3 mA I _{OH} = -24 mA I _{OH} = -32 mA
V _{OL}	Output LOW Voltage	54ABT 74ABT		0.55 0.55	V	Min	I _{OL} = 48 mA I _{OL} = 64 mA
I _{IH}	Input HIGH Current			5 5	μA	Max	V _{IN} = 2.7V (Note 2) V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current			-5 -5	μA	Max	V _{IN} = 0.5V (Note 2) V _{IN} = 0.0V
V _{ID}	Input Leakage Test		4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OS}	Output Short-Circuit Current		-100	-275	mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output High Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
I _{CCH}	Power Supply Current			50	μA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current			30	mA	Max	All Outputs LOW
I _{CCT}	Maximum I _{CC} /Input	Outputs Enabled		2.5	mA	Max	V _I = V _{CC} - 2.1V Data Input V _I = V _{CC} - 2.1V All Others at V _{CC} or GND
I _{CCD}	Dynamic I _{CC}	No Load		0.1	mA/ MHz	Max	Outputs Open (Note 1) One Bit Toggling, 50% Duty Cycle

Note 1: For 8 bits toggling, I_{CCD} < 0.5 mA/MHz.

Note 2: Guaranteed but not tested.

AC Electrical Characteristics: See Section 2 (SOIC package, contact factory for DIP or SSOP)

Symbol	Parameter	74ABTC			54ABTC		74ABTC		Units	Fig. No.	
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$				
		Min	Typ	Max	Min	Max	Min	Max			
f_{max}	Max Clock Frequency								MHz		
t_{PLH} t_{PHL}	Propagation Delay CP to O_n	2.2 3.1		6.2 7.1				2.2 3.1	6.2 7.1	ns	2-3, 5
t_{PHL}	Propagation Delay $\overline{\text{MR}}$ to O_n	2.4 2.4		6.7 6.7				2.4 2.4	6.7 6.7	ns	2-3, 5

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ABTC		54ABTC		74ABTC		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW D_n to CP	1.0 1.5				1.0 1.5		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW D_n to CP	2.0 2.0				2.0 2.0		ns	2-6
$t_w(\text{H})$ $t_w(\text{L})$	Pulse Width, CP, HIGH or LOW	3.3 3.3				3.3 3.3		ns	2-3
$t_w(\text{L})$	Master Reset Pulse Width, LOW							ns	2-3
t_{REC}	Recovery Time $\overline{\text{MR}}$ to CP							ns	2-6

Capacitance (SOIC package, contact factory for DIP or SSOP)

Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ\text{C}$
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0\text{V}$
C_{OUT} (Note 1)	Output Capacitance	9	pF	$V_{CC} = 5.0\text{V}$

Note 1: C_{OUT} is measured at frequency $f = 1\text{ MHz}$, per MIL-STD-833B, Method 3012.