Integrated Circuit Systems, Inc.

ICS9248-105

Preliminary Product Preview

Frequency Generator & Integrated Buffers for Celeron & PII/III™

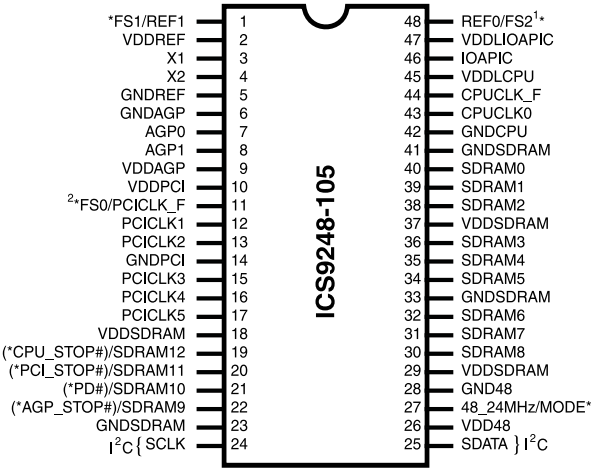
Recommended Application:
ALI 1641 PII/PIII chip set.

Output Features:
- 2- CPUs @2.5V, up to 146.22MHz
- 2 - AGPCLK @ 3.3V
- 13 - SDRAM @ 3.3V, up to166MHz
- 6- PCICLK @3.3V
- 1- IOAPIC @ 2.5V
- 1- 48MHz (Could be 24MHz via I^2C) @ 3.3V
- 2- REF @3.3V, 14.318MHz

Features:
- Up to 146.22MHz frequency support
- Support power management: CPU, PCI, AGP stop and Power down Mode form I^2C programming.
- Spread spectrum for EMI control (0 to -0.5%, ± 0.25%)
- Uses external 14.318MHz crystal

Skew Specifications:
- CPU – CPU: <175ps
- SDRAM - SDRAM: < 400ps
- AGP-AGP: <250ps
- PCI – PCI: <500ps
- CPU-SDRAM<500ps
- CPU(early)-PCI: MIN=1.0ns,TYP=2.0,MAX=3.0
- CPU-AGP<500ps

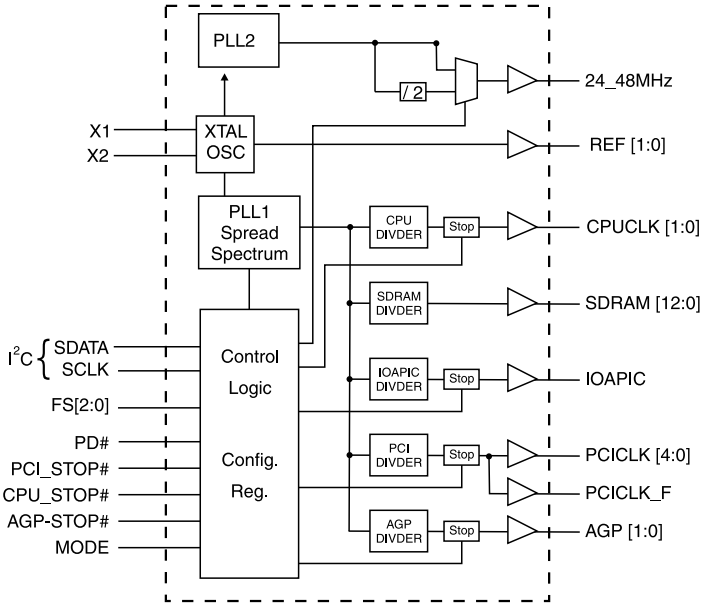
Pin Configuration



48-Pin 300mil SSOP

*: These inputs have a 120K pull-up to VDD on indicated inputs.
1: These are double strength.
2. Strong output

Block Diagram



Functionality

FS2	FS1	FS0	CPU	SDRAM	AGP	PCI
0	0	0	66.82	100.23	66.8	33.40
0	0	1	100.23	100.23	66.8	33.40
0	1	0	66.82	66.82	66.8	33.40
0	1	1	133.64	100.23	66.8	33.40
1	0	0	66.82	133.64	66.8	33.40
1	0	1	100.23	133.64	66.67	33.34
1	1	0	100.23	66.82	66.8	33.40
1	1	1	133.64	133.64	66.8	33.40

ICS9248-105

Preliminary Product Preview

General Description

The **ICS9248-105** is the single chip clock solution for Desktop/Notebook designs using the ALI 1641 PII/PIII style chipset. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9248-105 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I^2C interface allows changing functions, stop clock programming and frequency selection.

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	FS1	IN	Frequency select pin.
	REF1	OUT	14.318 MHz reference clock.
2, 9, 10, 18, 26, 29, 37	VDD	PWR	3.3V Power supply for SDRAM, AGP, PCI, reference output buffers and 48MHz output
3	X1	IN	Crystal input,nominally 14.318MHz.
4	X2	OUT	Crystal output, nominally 14.318MHz.
5, 6, 14, 23, 28, 42, 33, 41	GND	PWR	Ground pin for 3V outputs.
8, 7	AGP [1:0]	OUT	AGP outputs defined as 2X PCI.
11	FS0	IN	Frequency select pin.
	PCICLK_F	OUT	Free running PCI clock not affected by PCI_STOP# .
17, 16, 15, 13, 12	PCICLK [4:0]	OUT	PCI clock outputs.
19	CPU_STOP#	IN	Stops all CPUCLKs [1:0] besides the CPUCLK_F clocks at logic 0 level, when input low
	SDRAM12	OUT	SDRAM clock output
20	PCI_STOP#	IN	Stops all PCICLKs [5:1] besides the CPUCLK_F clocks at logic 0 level, when input low
	SDRAM11	OUT	SDRAM clock output
21	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
	SDRAM10	OUT	SDRAM clock output
22	AGP_STOP#	IN	Stops all AGP clocks [0:1] at logic 0 level, when input low
	SDRAM9	OUT	SDRAM clock output
24	SCLK	IN	Clock input of I2C input, 5V tolerant input
25	SDATA	IN	Data input for I2C serial input, 5V tolerant input
27	MODE	IN	Function select pin, 1=Desktop Mode, 0=Mobile Mode.
	48_24MHz	OUT	Selectable 48 or 24MHz output, default is 48MHz
30, 31, 32, 34, 35, 36, 38, 39, 40,	SDRAM[8:0]	OUT	SDRAM clock outputs
43	CPUCLK0	OUT	CPU clock output
44	CPUCLK_F	OUT	Free running CPU clock. Not affected by the CPU_STOP#.
45	VDDLCPU	PWR	Supply for CPU clocks, either 2.5V or 3.3V nominal
46	IOAPIC	OUT	2.5V clock output
47	VDDLAPIC	PWR	Power pin for the IOAPIC outputs. 2.5V.
48	FS2	IN	Frequency select pin.
	REF0	OUT	14.318 MHz reference clock.

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D2(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D3(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description								PWD
Bit (7:4)	Bit				CPU	SDRAM	AGP	PCI	0000 Note 1
	7	6	5	4					
	0	0	0	0	66.82	100.23	66.8	33.40	
	0	0	0	1	100.23	100.23	66.8	33.40	
	0	0	1	0	66.82	66.82	66.8	33.40	
	0	0	1	1	133.64	100.23	66.8	33.40	
	0	1	0	0	66.82	133.64	66.8	33.40	
	0	1	0	1	100.23	133.64	66.67	33.34	
	0	1	1	0	100.23	66.82	66.8	33.40	
	0	1	1	1	133.64	133.64	66.8	33.40	
	1	0	0	0	90.03	90.03	60.02	30.01	
	1	0	0	1	95.02	126.35	63.35	31.67	
	1	0	1	0	105.00	139.71	70.00	35.00	
	1	0	1	1	109.99	109.99	73.33	36.66	
	1	1	0	0	119.75	119.75	59.88	29.94	
	1	1	0	1	126.35	95.02	63.18	31.59	
	1	1	1	0	139.71	105.00	69.86	34.93	
	1	1	1	1	146.22	146.22	73.11	36.56	
Bit3	0-Frequency is selected by hardware select, latched inputs 1-Frequency is selected by Bit 7:4								0
Bit2	00- ±0.25% Center Spread Spectrum 01- Down Spread Spectrum 0 to -0.5% 10- Spread spectrum off 11- Tristate all outputs								00
Bit1									
Bit0	1- 48_24#MHz = 48 MHz 0- 48_24#MHz = 24 MHz								1

Note 1. Default at Power-up will be for latched logic inputs to define frequency.

Note: PWD = Power-Up Default

I^2C is a trademark of Philips Corporation

Byte 1: CPU, 48MHz Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	48-24MHz
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	-	1	(Reserved)
Bit 2	-	1	(Reserved)
Bit 1	43	1	CPUCLK 0
Bit 0	44	1	CPUCLK_F

Byte 2: PCI Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	11	1	PCICLK_F
Bit 6	-	1	(Reserved)
Bit 5	17	1	PCICLK5
Bit 4	16	1	PCICLK4
Bit 3	15	1	PCICLK3
Bit 2	13	1	PCICLK2
Bit 1	12	1	PCICLK1
Bit 0	-	1	(Reserved)

Byte 3: SDRAM Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	31	1	SDRAM7
Bit 6	32	1	SDRAM6
Bit 5	34	1	SDRAM5
Bit 4	35	1	SDRAM4
Bit 3	36	1	SDRAM3
Bit 2	38	1	SDRAM2
Bit 1	39	1	SDRAM 1
Bit 0	40	1	SDRAM0

Byte 4: SDRAM Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	FS2#
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	19	1	SDRAM12
Bit 3	20	1	SDRAM11
Bit 2	21	1	SDRAM10
Bit 1	22	1	SDRAM 9
Bit 0	30	1	SDRAM8

Byte 5: Reserved Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	FS0#
Bit 6	-	X	MODE#
Bit 5	-	X	FS1#
Bit 4	48	1	REF0
Bit 3	1	1	REF1
Bit 2	7	1	AGP0
Bit 1	8	1	AGP1
Bit 0	46	1	IOAPIC

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inferted logic load of the input frequency select pin conditions.

Byte 6: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved (Note)
Bit6	-	0	Reserved (Note)
Bit5	-	0	Reserved (Note)
Bit4	-	0	Reserved (Note)
Bit3	-	0	Reserved (Note)
Bit2	-	1	Reserved (Note)
Bit1	-	1	Reserved (Note)
Bit0	-	0	Reserved (Note)

Note: Don't write into this register, writing into this register can cause malfunction

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9248-105 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

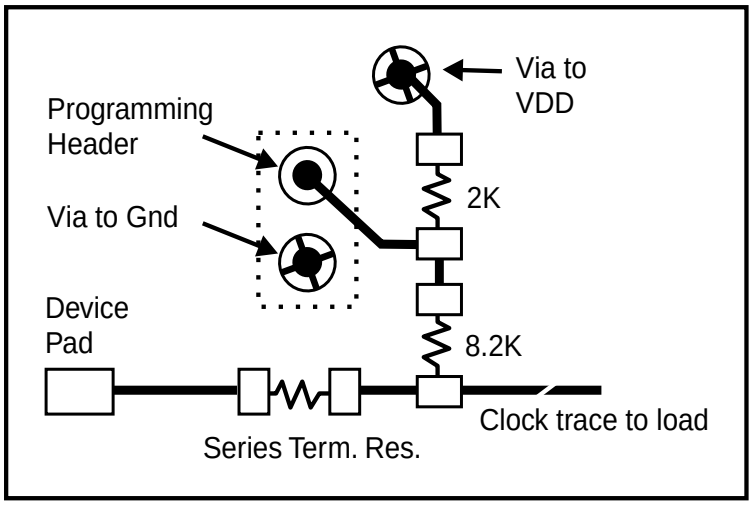
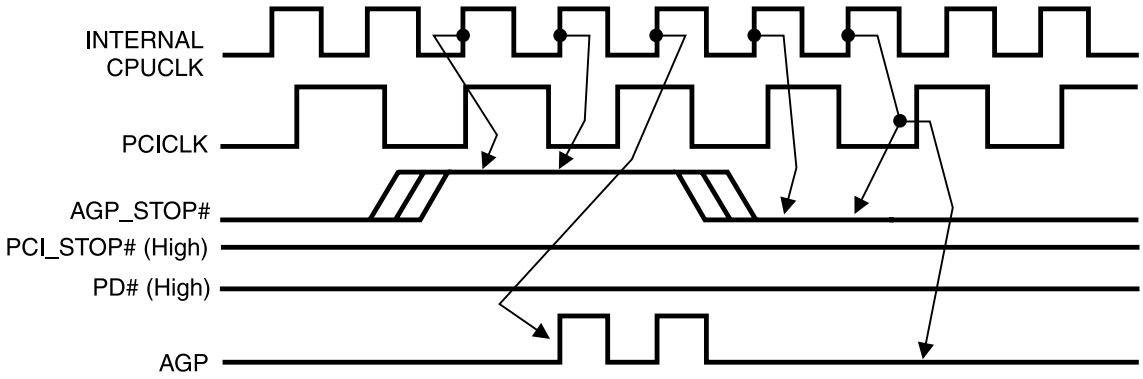


Fig. 1

AGP_STOP# Timing Diagram

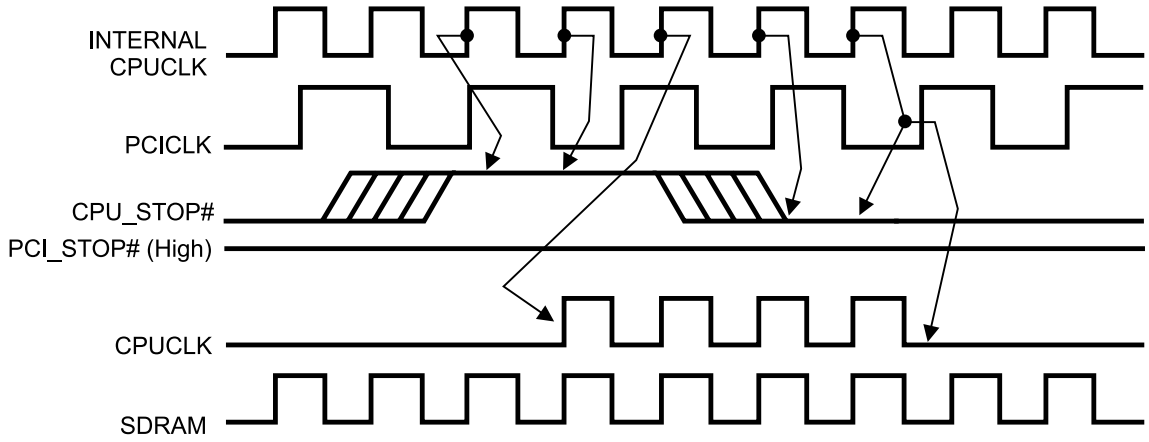
AGP_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the AGP clocks. for low power operation. AGP_STOP# is synchronized by the **ICS9248-105**. The AGPCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. AGPCLK on latency is less than AGPCLK and AGPCLK off latency is less than 4 AGPCLKs. This function is available only with MODE pin latched low.



Notes:
1. All timing is referenced to the internal CPUCLK.
2. AGP_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS9248-105**.
3. All other clocks continue to run undisturbed.
4. PD# and PCI_STOP# are shown in a high (true) state.
5. Only applies if MODE pin latched 0 at power up.

CPU_STOP# Timing Diagram

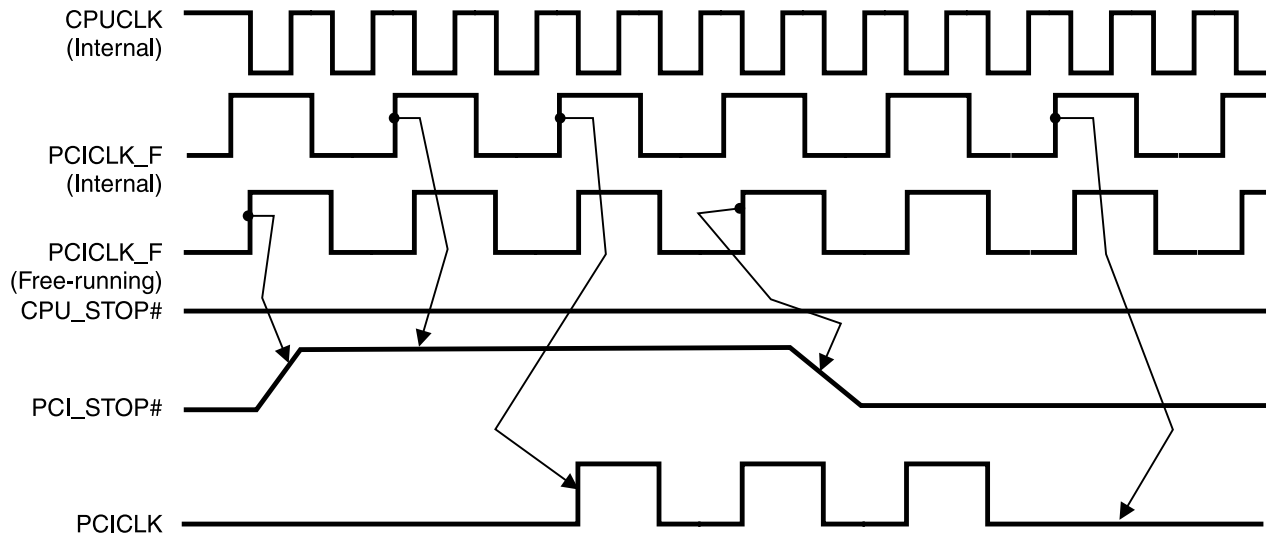
CPU_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU_STOP# is synchronized by the **ICS9248-105**. The minimum that the CPU clock is enabled (CPU_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.



Notes:
1. All timing is referenced to the internal CPU clock.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9248-105.
3. All other clocks continue to run undisturbed. (including SDRAM outputs).

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9248-105**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICSXXXX** internally. The minimum that the PCICLK clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248-105.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI_STOP# and CPU_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.

Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Supply Current	I_{DD}	C_L = 0 pF; Select @ 66M			180	mA
	I_{DDL}				30	mA
Input frequency	F_i	V_{DD} = 3.3 V;				MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pS
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	mS
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.				mS
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	mS
Skew[1]	$T_{CPU-BUS}$	V_T = 1.5 V;	1.0		3.0	nS

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2A}[1]	$V_O = V_{DD}*(0.5)$ Output P	10		20	Ω
Output Impedance	R_{DSN2A}[1]	$V_O = V_{DD}*(0.5)$ Output N	10		20	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA			0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V			-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19			mA
Rise Time	t_{r2A}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4		2.0	nS
Fall Time	t_{f2A}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4		2.0	nS
Duty Cycle	d_{t2A}[1]	V_T = 1.25 V	45.0		55.0	%
Skew (Window)	t_{sk2A}[1]	V_T = 1.25 V			175	pS
Jitter						

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 24M, 48M, REF 1

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP5}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output Impedance	R_{DSN5}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH5}	I_{OH} = -14 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 6.0 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-20	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	10			mA
Rise Time	t_{r5}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V			4.0	nS
Fall Time	t_{f5}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V			4.0	nS
Duty Cycle	d_{t5}[1]	V_T = 1.5 V	45.0		55.0	%
Jitter	t_{j1s5}[1]	V_T = 1.5 V			250	pS
	t_{jabs5}[1]	V_T = 1.5 V			800	pS

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -18 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	25			mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V			2.0	nS
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V			2.0	nS
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45.0		55.0	%
Skew Window	t_{sk1}[1]	V_T = 1.5 V			250	pS
Jitter	t_{j1s1}[1]	V_T = 1.5 V			150	pS
	t_{jabs1}[1]	V_T = 1.5 V			500	pS

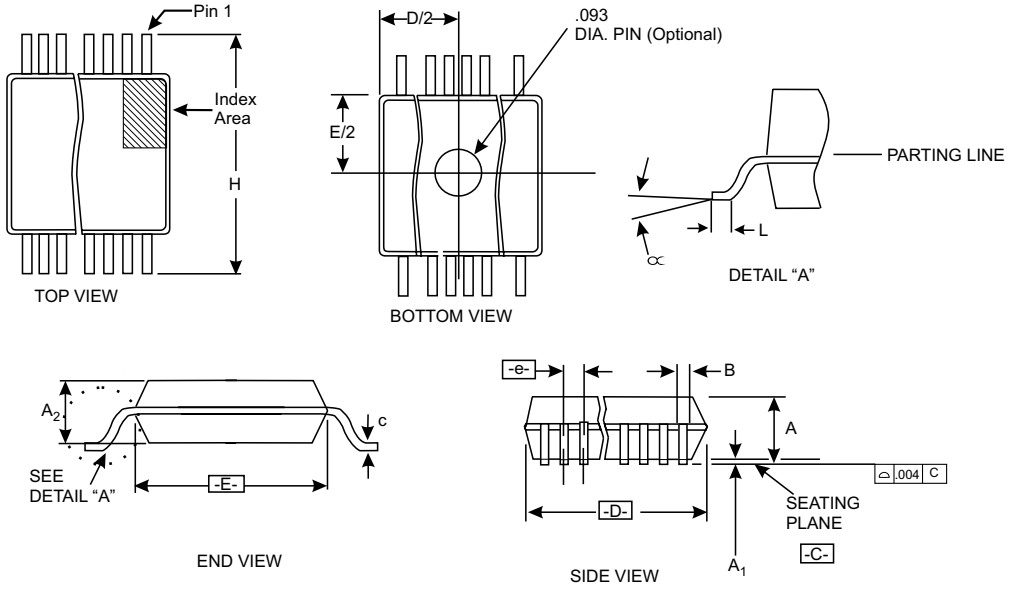
[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} =V_{DDL} 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2A}[1]	$V_O = V_{DD}*(0.5)$	10		20	Ω
Output Impedance	R_{DSN2A}[1]	$V_O = V_{DD}*(0.5)$	10		20	Ω
Output High Voltage	V_{OH2A}	I_{OH} = -28 mA	2.4			V
Output Low Voltage	V_{OL2A}	I_{OL} = 19 mA			0.4	V
Output High Current	I_{OH2A}	V_{OH} = 2.0 V			-42	mA
Output Low Current	I_{OL2A}	V_{OL} = 0.8 V	33			mA
Rise Time	t_{r2A}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	nS
Fall Time	t_{f2A}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	nS
Duty Cycle	d_{t2A}[1]	V_T = 1.5 V	45		55	%
Skew Window (output to output)	t_{sk2A}[1]	V_T = 1.5 V			400	pS
Skew (Bufferin to output)	t_{sk2A}[1]	V_T = 1.5 V				nS

[1]Guarenteed by design, not 100% tested in production.



SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.102	.110	AC	.620	.625	.630	48
A1	.008	.012	.016					
A2	.087	.090	.094					
B	.008	-	.0135					
c	.005	-	.010					
D	See Variations							
E	.291	.295	.299					
e	0.025 BSC							
H	.395	-	.420					
h	.010	.013	.016					
L	.020	-	.040					
N	See Variations							
∝	0°	-	8°					

"For current dimensional specifications, see JEDEC 95."

Dimensions in inches

48 Pin 300 mil SSOP Package

Ordering Information

ICS9248yF-105-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device