# M5M416160DJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

## DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.**Self refresh current is low enough for battery back-up application.**

## FEATURES

| Type name | $\overline{RAS}$ access time (max.ns) | $\overline{CAS}$ access time (max.ns) | Address access time (max.ns) | $\overline{OE}$ access time (max.ns) | Cycle time (min.ns) | Power dissipation (typ.mW) |
|---|---|---|---|---|---|---|
| **M5M416160DXX-5,-5S** | 50 | 13 | 25 | 13 | 90 | 540 |
| **M5M416160DXX-6,-6S** | 60 | 15 | 30 | 15 | 110 | 430 |
| **M5M416160DXX-7,-7S** | 70 | 20 | 35 | 20 | 130 | 385 |

XX=J,TP

- Standard 42 pin SOJ, 50 pin TSOP
- Single 5.0V ±10% supply
- Low stand-by power dissipation
  5.5mW (Max) ---------- CMOS Input level
- Low operating power dissipation
  M5M416160Dxx-5,-5S ---------- 660.0mW (Max)
  M5M416160Dxx-6,-6S ---------- 525.0mW (Max)
  M5M416160Dxx-7,-7S ---------- 470.0mW (Max)
- Fast-page mode , Read-modify-write,$\overline{RAS}$-only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
  All inputs, output TTL compatible and low capacitance
- 4096 refresh cycles every 64ms ($A_0$~$A_{11}$)
  4096 refresh cycles every 128ms ($A_0$~$A_{11}$)*
  *: Applicable to self refresh version (M5M416160DJ,TP-5S,-6S, -7S : option) only

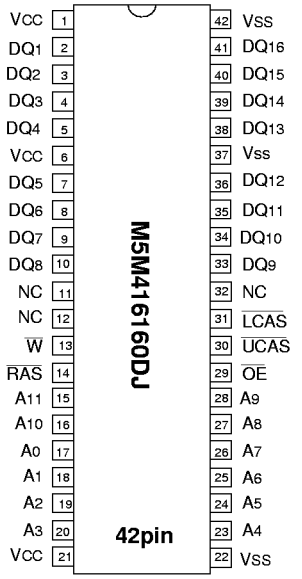
## APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

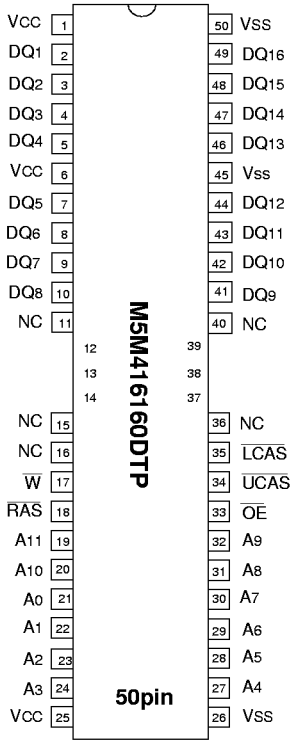
## PIN DESCRIPTION

| Pin name | Function |
|---|---|
| $A_0$~$A_{11}$ | Address inputs |
| $DQ_1$~$DQ_{16}$ | Data inputs / outputs |
| $\overline{RAS}$ | Row address strobe Input |
| $\overline{UCAS}$ | Upper byte control column address strobe input |
| $\overline{LCAS}$ | Lower byte control column address strobe input |
| $\overline{W}$ | Write control input |
| $\overline{OE}$ | Output enable input |
| $V_{CC}$ | Power supply (+5.0V) |
| $V_{SS}$ | Ground (0V) |

## PIN CONFIGURATION (TOP VIEW)




Outline 42P0N-A (400mil SOJ)




Outline 50P3G-F (400mil TSOP Normal Bend)

NC : NO CONNECTION



MITSUBISHI ELECTRIC

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## FUNCTION

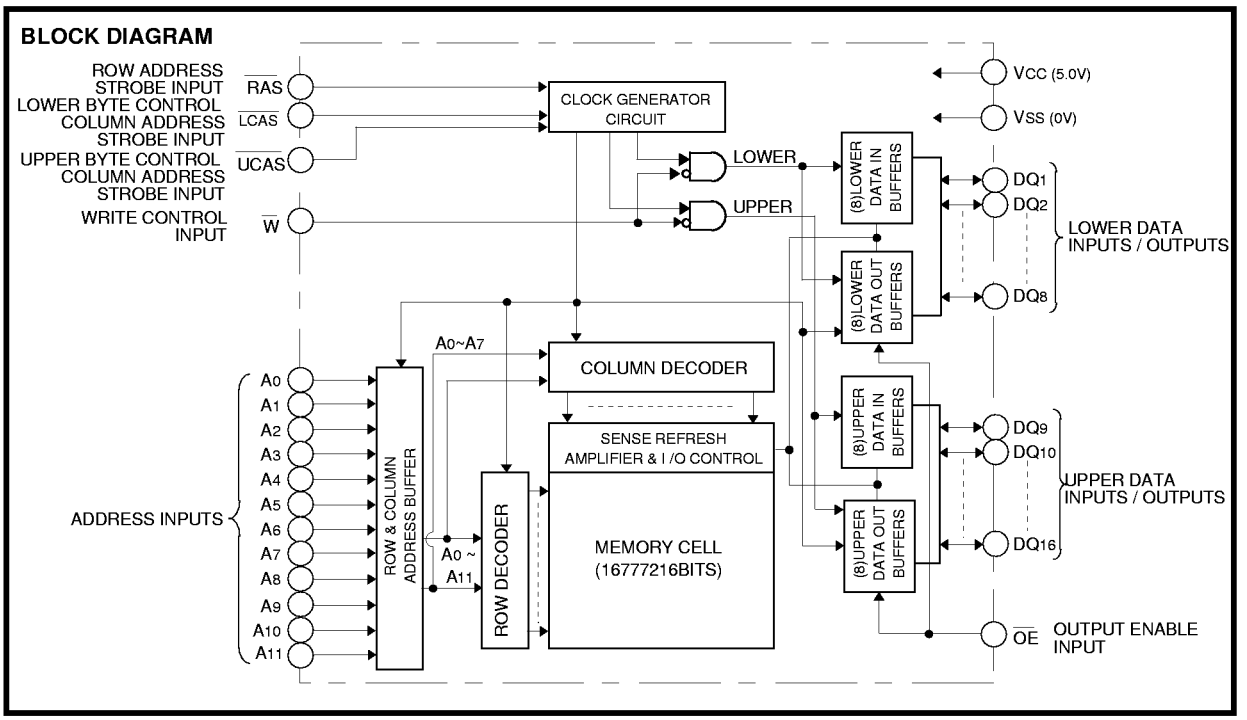
The M5M416160DJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

### Table 1 Input conditions for each mode

| Operation | Inputs | | | | | Input/Output | | Refresh | Remark |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{LCAS}$ | $\overline{UCAS}$ | $\overline{W}$ | $\overline{OE}$ | DQ1~DQ8 | DQ9~DQ16 | | |
| Lower byte Read | ACT | ACT | NAC | NAC | ACT | VLD | OPN | YES | Fast page mode identical |
| Upper byte Read | ACT | NAC | ACT | NAC | ACT | OPN | VLD | YES | |
| Word Read | ACT | ACT | ACT | NAC | ACT | VLD | VLD | YES | |
| Lower Byte Write | ACT | ACT | NAC | ACT | NAC | DIN | DNC | YES | |
| Upper Byte Write | ACT | NAC | ACT | ACT | NAC | DNC | DIN | YES | |
| Word write | ACT | ACT | ACT | ACT | NAC | DIN | DIN | YES | |
| $\overline{RAS}$-only refresh | ACT | NAC | NAC | DNC | DNC | OPN | OPN | YES | |
| Hidden refresh | ACT | ACT | ACT | NAC | ACT | VLD | VLD | YES | |
| Self refresh | ACT | ACT | ACT | NAC | DNC | OPN | OPN | YES | |
| $\overline{CAS}$ before $\overline{RAS}$ refresh | ACT | ACT | ACT | DNC | DNC | OPN | OPN | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | OPN | OPN | NO | |

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

## BLOCK DIAGRAM



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FAST PAGE MODE 16777216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | -1~7 | V |
| $V_I$ | Input voltage | | -1~7 | V |
| $V_O$ | Output voltage | | -1~7 | V |
| $I_O$ | Output current | | 50 | mA |
| $P_d$ | Power dissipation | Ta=25 °C | 1000 | mW |
| $T_{opr}$ | Operating temperature | | 0~70 | °C |
| $T_{stg}$ | Storage temperature | | -65~150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High-level input voltage, all inputs | 2.4 | | 5.5 | V |
| $V_{IL}$ | Low-level input voltage, all inputs | -1** | | 0.8 | V |

Note 1 : All voltage values are with respect to $V_{SS}$.

**** : ViL(min.) is -2.0V when undershoot width is less than 25ns.(The width is defined as the period when the voltage level below Vss.)**

## ELECTRICAL CHARACTERISTICS (Ta=0~70°C, $V_{CC}$=5.0V±0%, $V_{SS}$=0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$=-5mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$=4.2mA | 0 | | 0.4 | V |
| $I_{OZ}$ | Off-state output current | | Q floating 0V≤$V_{OUT}$ ≤5.5V | -10 | | 10 | μA |
| $I_I$ | Input current | | 0V≤$V_{IN}$≤6V, Other inputs pins=0V | -10 | | 10 | μA |
| $I_{CC1(AV)}$ | Average supply current from $V_{CC}$, operating (Note 3,4,5) | M5M416160D-5,-5S | $\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC}$=$t_{WC}$=min. output open | | | 120 | mA |
| | | M5M416160D-6,-6S | | | | 95 | |
| | | M5M416160D-7,-7S | | | | 85 | |
| $I_{CC2}$ | Supply current from $V_{CC}$, stand-by (Note 6) | | $\overline{RAS}$= $\overline{CAS}$ =$V_{IH}$, output open | | | 2 | mA |
| | | | $\overline{RAS}$= $\overline{CAS}$ ≥$V_{CC}$ -0.2V output open | | | 1 | |
| | | | | | | 0.3* | |
| $I_{CC3(AV)}$ | Average supply current from $V_{CC}$, refreshing (Note 3,5) | M5M416160D-5,-5S | $\overline{RAS}$ cycling, $\overline{CAS}$=$V_{IH}$ $t_{RC}$=min. output open | | | 120 | mA |
| | | M5M416160D-6,-6S | | | | 95 | |
| | | M5M416160D-7,-7S | | | | 85 | |
| $I_{CC4(AV)}$ | Average supply current from $V_{CC}$ Fast-page-mode (Note 3,4,5) | M5M416160D-5,-5S | $\overline{RAS}$=$V_{IL}$, $\overline{CAS}$ cycling $t_{PC}$=min. output open | | | 80 | mA |
| | | M5M416160D-6,-6S | | | | 70 | |
| | | M5M416160D-7,-7S | | | | 65 | |
| $I_{CC6(AV)}$ | Average supply current from $V_{CC}$ $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3) | M5M416160D-5,-5S | $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $t_{RC}$=min. output open | | | 120 | mA |
| | | M5M416160D-6,-6S | | | | 95 | |
| | | M5M416160D-7,-7S | | | | 85 | |
| $I_{CC8(AV)}$* | Average supply current from $V_{CC}$ Extended-refresh cycle (Note 6) | M5M416160D (S) | Stand-by: $\overline{RAS}$≥Vcc-0.2V $\overline{CAS}$≥Vcc-0.2V or $\overline{CAS}$≤0.2V $\overline{CAS}$ before $\overline{RAS}$ refresh: $\overline{RAS}$ cycling $\overline{CAS}$≤0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W}$≤0.2V or ≥Vcc-0.2V $\overline{OE}$≤0.2V or ≥Vcc-0.2V $A_0$~$A_{11}$≤0.2V or ≥Vcc-0.2V DQ=open, $t_{RC}$=125μs, $t_{RAS}$=$t_{RASmin}$~1μs | | | 600 | μA |
| $I_{CC9(AV)}$* | Average supply current from $V_{CC}$ Self-refresh cycle | M5M416160D (S) | $\overline{RAS}$=$\overline{CAS}$≤0.2V | | | 400 | μA |

Note 2: Current flowing into an IC is positive, out is negative.

3: $I_{CC1}$ (AV), $I_{CC3}$ (AV) and $I_{CC4}$ (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: $I_{CC1}$ (AV) and $I_{CC4}$ (AV) are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while $\overline{RAS}$=$V_{IL}$ and $\overline{LCAS}$/$\overline{UCAS}$=$V_{IH}$ .

* : Applicable to self refresh version (M5M416160DJ,TP-5S,-6S,-7S : option) only

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**CAPACITANCE** (Ta=0~70°C, $V_{CC}$=5.0V±10%, $V_{SS}$=0V, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $C_{I(A)}$ | Input capacitance, address inputs | $V_I$=$V_{SS}$<br>f=1MHz<br>$V_I$=25mVrms | | | 5 | pF |
| $C_{I(\overline{OE})}$ | Input capacitance, $\overline{OE}$ input | | | | 7 | pF |
| $C_{I(\overline{W})}$ | Input capacitance, write control input | | | | 7 | pF |
| $C_{I(\overline{RAS})}$ | Input capacitance, $\overline{RAS}$ input | | | | 7 | pF |
| $C_{I(\overline{CAS})}$ | Input capacitance, $\overline{CAS}$ input | | | | 7 | pF |
| $C_{I/O}$ | Input/Output capacitance, data ports | | | | 7 | pF |

**SWITCHING CHARACTERISTICS** (Ta=0~70°C, $V_{CC}$=5.0V±10%, Vss=0V, unless otherwise noted, see notes 6,13,14)

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M416160D-5,-5S | | M5M416160D-6,-6S | | M5M416160D-7,-7S | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{CAC}$ | Access time from $\overline{CAS}$ | (Note 7,8) | | 13 | | 15 | | 20 | ns |
| $t_{RAC}$ | Access time from $\overline{RAS}$ | (Note 7,9) | | 50 | | 60 | | 70 | ns |
| $t_{AA}$ | Columu address access time | (Note 7,10) | | 25 | | 30 | | 35 | ns |
| $t_{CPA}$ | Access time from $\overline{CAS}$ precharge | (Note 7,11) | | 30 | | 35 | | 40 | ns |
| $t_{OEA}$ | Access time from $\overline{OE}$ | (Note 7) | | 13 | | 15 | | 20 | ns |
| $t_{CLZ}$ | Output low impedance time from $\overline{CAS}$ low | (Note 7) | 5 | | 5 | | 5 | | ns |
| $t_{OFF}$ | Output disable time after $\overline{CAS}$ high | (Note 12) | | 13 | | 15 | | 15 | ns |
| $t_{OEZ}$ | Output disable time after $\overline{OE}$ high | (Note 12) | | 13 | | 15 | | 15 | ns |

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 64ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to $V_{OH}$=2.4V($I_{OH}$=-5mA) / $V_{OL}$=0.4V($I_{OL}$=4.2mA) load 100pF.
The reference levels for measuring of output signal are 2.4V($V_{OH}$) and 0.4V($V_{OL}$).

8: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

9: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If $t_{RCD}$ or $t_{RAD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ will increase by amount that $t_{RCD}$ exceeds the value shown.

10: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

12: $t_{OFF(max)}$ and $t_{OEZ\ (max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT}$ ≤ I ±10 μA I) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

**TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Fast-Page Mode Cycles)**
($T_a$=0~70°C, $V_{CC}$=5.0V±10%, $V_{SS}$=0V, unless otherwise noted, see notes 13,14)

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M416160D-5,-5S | | M5M416160D-6,-6S | | M5M416160D-7,-7S | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{REF}$ | Refresh cycle time | | | 64 | | 64 | | 64 | ms |
| $t_{REF}$* | Refresh cycle time | | | 128 | | 128 | | 128 | ms |
| $t_{RP}$ | $\overline{RAS}$ high pulse width | | 30 | | 40 | | 50 | | ns |
| $t_{RCD}$ | Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low | (Note 15) | 18 | 37 | 20 | 45 | 20 | 50 | ns |
| $t_{CRP}$ | Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low | | 10 | | 10 | | 10 | | ns |
| $t_{RPC}$ | Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low | | 0 | | 0 | | 0 | | ns |
| $t_{CPN}$ | $\overline{CAS}$ high pulse width | | 10 | | 10 | | 13 | | ns |
| $t_{RAD}$ | Column address delay time from $\overline{RAS}$ low | (Note 16) | 13 | 25 | 15 | 30 | 15 | 35 | ns |
| $t_{ASR}$ | Row address setup time before $\overline{RAS}$ low | | 0 | | 0 | | 0 | | ns |
| $t_{ASC}$ | Column address setup time before $\overline{CAS}$ low | (Note 17) | 0 | 10 | 0 | 10 | 0 | 10 | ns |
| $t_{RAH}$ | Row address hold time after $\overline{RAS}$ low | | 8 | | 10 | | 10 | | ns |
| $t_{CAH}$ | Column address hold time after $\overline{CAS}$ low | | 13 | | 15 | | 15 | | ns |
| $t_{DZC}$ | Delay time, data to $\overline{CAS}$ low | (Note 18) | 0 | | 0 | | 0 | | ns |
| $t_{DZO}$ | Delay time, data to $\overline{OE}$ low | (Note 18) | 0 | | 0 | | 0 | | ns |
| $t_{CDD}$ | Delay time, $\overline{CAS}$ high to data | (Note 19) | 13 | | 15 | | 15 | | ns |
| $t_{ODD}$ | Delay time, $\overline{OE}$ high to data | (Note 19) | 13 | | 15 | | 15 | | ns |
| $t_T$ | Transition time | (Note 20) | 1 | 50 | 1 | 50 | 1 | 50 | ns |

Note 13: The timing requirements are assumed $t_T$=5ns.
14: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
15: $t_{RCD(max)}$ is specified as a reference point only. If $t_{RCD}$ is less than $t_{RCD(max)}$, access time is $t_{RAC}$. If $t_{RCD}$ is greater than $t_{RCD(max)}$, access time is controlled exclusively by $t_{CAC}$ or $t_{AA}$. $t_{RCD(min)}$ is specified as $t_{RCD(min)}=t_{RAH(min)}+2t_T+t_{ASC(min)}$.
16: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD}\geq t_{RAD(max)}$ and $t_{ASC}\leq t_{ASC(max)}$, access time is controlled exclusively by $t_{AA}$.
17: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD}\geq t_{RCD(max)}$ and $t_{ASC}\geq t_{ASC(max)}$, access time is controlled exclusively by $t_{CAC}$.
18: Either $t_{DZC}$ or $t_{DZO}$ must be satisfied.
19: Either $t_{CDD}$ or $t_{ODD}$ must be satisfied.
20: $t_T$ is measured between $V_{IH(min)}$ and $V_{IL(max)}$.
* : Applicable to self refresh version (M5M416160DJ,TP-5S,-6S,-7S : option) only

**Read and Refresh Cycles**

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M416160D-5,-5S | | M5M416160D-6,-6S | | M5M416160D-7,-7S | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{RC}$ | Read cycle time | | 90 | | 110 | | 130 | | ns |
| $t_{RAS}$ | $\overline{RAS}$ low pulse width | | 50 | 10000 | 60 | 10000 | 70 | 10000 | ns |
| $t_{CAS}$ | $\overline{CAS}$ low pulse width | | 13 | 10000 | 15 | 10000 | 20 | 10000 | ns |
| $t_{CSH}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ low | | 50 | | 60 | | 70 | | ns |
| $t_{RSH}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ low | | 13 | | 15 | | 20 | | ns |
| $t_{RCS}$ | Read setup time before $\overline{CAS}$ low | | 0 | | 0 | | 0 | | ns |
| $t_{RCH}$ | Read hold time after $\overline{CAS}$ high | (Note 21) | 0 | | 0 | | 0 | | ns |
| $t_{RRH}$ | Read hold time after $\overline{RAS}$ high | (Note 21) | 10 | | 10 | | 10 | | ns |
| $t_{RAL}$ | Column address to $\overline{RAS}$ hold time | | 25 | | 30 | | 35 | | ns |
| $t_{OCH}$ | $\overline{CAS}$ hold time after $\overline{OE}$ low | | 13 | | 15 | | 20 | | ns |
| $t_{ORH}$ | $\overline{RAS}$ hold time after $\overline{OE}$ low | | 13 | | 15 | | 20 | | ns |

Note 21: Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.

### Write Cycle (Early Write and Delayed Write)

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M416160D-5,-5S | | M5M416160D-6,-6S | | M5M416160D-7,-7S | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{WC}$ | Write cycle time | | 90 | | 110 | | 130 | | ns |
| $t_{RAS}$ | $\overline{RAS}$ low pulse width | | 50 | 10000 | 60 | 10000 | 70 | 10000 | ns |
| $t_{CAS}$ | $\overline{CAS}$ low pulse width | | 13 | 10000 | 15 | 10000 | 20 | 10000 | ns |
| $t_{CSH}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ low | | 50 | | 60 | | 70 | | ns |
| $t_{RSH}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ low | | 13 | | 15 | | 20 | | ns |
| $t_{WCS}$ | Write setup time before $\overline{CAS}$ low | (Note 23) | 0 | | 0 | | 0 | | ns |
| $t_{WCH}$ | Write hold time after $\overline{CAS}$ low | | 8 | | 10 | | 15 | | ns |
| $t_{CWL}$ | $\overline{CAS}$ hold time after $\overline{W}$ low | | 13 | | 15 | | 20 | | ns |
| $t_{RWL}$ | $\overline{RAS}$ hold time after $\overline{W}$ low | | 13 | | 15 | | 20 | | ns |
| $t_{WP}$ | Write pulse width | | 8 | | 10 | | 15 | | ns |
| $t_{DS}$ | Data setup time before $\overline{CAS}$ low or $\overline{W}$ low | | 0 | | 0 | | 0 | | ns |
| $t_{DH}$ | Data hold time after $\overline{CAS}$ low or $\overline{W}$ low | | 10 | | 15 | | 15 | | ns |
| $t_{OEH}$ | $\overline{OE}$ hold time after $\overline{W}$ low | | 13 | | 15 | | 20 | | ns |

### Read-Write and Read-Modify-Write Cycles

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M416160D-5,-5S | | M5M416160D-6,-6S | | M5M416160D-7,-7S | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{RWC}$ | Read write/read modify write cycle time | (Note 22) | 131 | | 155 | | 180 | | ns |
| $t_{RAS}$ | $\overline{RAS}$ low pulse width | | 91 | 10000 | 105 | 10000 | 120 | 10000 | ns |
| $t_{CAS}$ | $\overline{CAS}$ low pulse width | | 54 | 10000 | 60 | 10000 | 70 | 10000 | ns |
| $t_{CSH}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ low | | 91 | | 105 | | 120 | | ns |
| $t_{RSH}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ low | | 54 | | 60 | | 70 | | ns |
| $t_{RCS}$ | Read setup time before $\overline{CAS}$ low | | 0 | | 0 | | 0 | | ns |
| $t_{CWD}$ | Delay time, $\overline{CAS}$ low to $\overline{W}$ low | (Note 23) | 36 | | 40 | | 45 | | ns |
| $t_{RWD}$ | Delay time, $\overline{RAS}$ low to $\overline{W}$ low | (Note 23) | 73 | | 85 | | 95 | | ns |
| $t_{AWD}$ | Delay time, address to $\overline{W}$ low | (Note 23) | 48 | | 55 | | 60 | | ns |
| $t_{CWL}$ | $\overline{CAS}$ hold time after $\overline{W}$ low | | 13 | | 15 | | 20 | | ns |
| $t_{RWL}$ | $\overline{RAS}$ hold time after $\overline{W}$ low | | 13 | | 15 | | 20 | | ns |
| $t_{WP}$ | Write pulse width | | 8 | | 10 | | 10 | | ns |
| $t_{DS}$ | Data setup time before $\overline{W}$ low | | 0 | | 0 | | 0 | | ns |
| $t_{DH}$ | Data hold time after $\overline{W}$ low | | 10 | | 10 | | 15 | | ns |
| $t_{OEH}$ | $\overline{OE}$ hold time after $\overline{W}$ low | | 13 | | 15 | | 15 | | ns |

Note 22: $t_{RWC}$ is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.

23: $t_{WCS}$, $t_{CWD}$, $t_{RWD}$ and $t_{AWD}$ and, $t_{CPWD}$ are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CPWD} \geq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to $V_{IH}$) is indeterminate.

### Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle) (Note 24)

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M416160D-5,-5S | | M5M416160D-6,-6S | | M5M416160D-7,-7S | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PC}$ | Fast page mode read/write cycle time | | 35 | | 40 | | 45 | | ns |
| $t_{PRWC}$ | Fast page mode read write/read modify write cycle time | | 76 | | 85 | | 95 | | ns |
| $t_{RAS}$ | $\overline{RAS}$ low pulse width for read write cycle | (Note 25) | 85 | 125000 | 100 | 125000 | 115 | 125000 | ns |
| $t_{CP}$ | $\overline{CAS}$ high pulse width | (Note 26) | 8 | 12 | 10 | 15 | 10 | 15 | ns |
| $t_{CPRH}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ precharge | | 30 | | 35 | | 40 | | ns |
| $t_{CPWD}$ | Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low | (Note 23) | 53 | | 60 | | 65 | | ns |

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

25: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

26: $t_{CP(max)}$ is specified as a reference point only.

**$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle** (Note 27)

| Symbol | Parameter | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | M5M416160D-5,-5S | | M5M416160D-6,-6S | | M5M416160D-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| $t_{CSR}$ | $\overline{CAS}$ setup time before $\overline{RAS}$ low | 10 | | 10 | | 10 | | ns |
| $t_{CHR}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ low | 10 | | 10 | | 15 | | ns |

Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

## SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/ -6S/ -7S. The other characteristics and requirements than the below are same as normal devices.

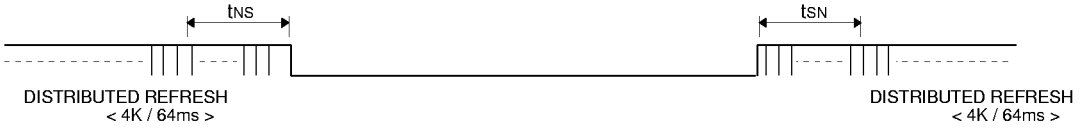
**TIMING REQUIREMENTS** ($T_a$=0~70°C, $V_{CC}$=5.0V ±10%, $V_{SS}$=0V, unless otherwise noted, see notes 13,14)

| Symbol | Parameter | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | M5M416160D-5S | | M5M416160D-6S | | M5M416160D-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| $t_{RASS}$ | Self Refresh $\overline{RAS}$ low pulse width | 100 | | 100 | | 100 | | µs |
| $t_{RPS}$ | Self Refresh $\overline{RAS}$ high precharge time | 90 | | 110 | | 130 | | ns |
| $t_{CHS}$ | Self Refresh $\overline{RAS}$ hold time | - 50 | | - 50 | | - 50 | | ns |
| $t_{RSR}$ | Read setup time before $\overline{RAS}$ low | 10 | | 10 | | 10 | | ns |
| $t_{RHR}$ | Read hold time after $\overline{RAS}$ low | 10 | | 10 | | 15 | | ns |

## SELF REFRESH ENTRY & EXIT CONDITIONS

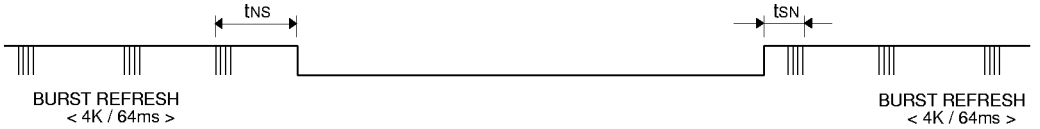
**(1) In case of distributed refresh**

The last / first full refresh cycles (4K) must be made within $t_{NS}$ / $t_{SN}$ before / after self refresh, on the condition of $t_{NS} \leq 64$ms and $t_{SN} \leq 64$ms.



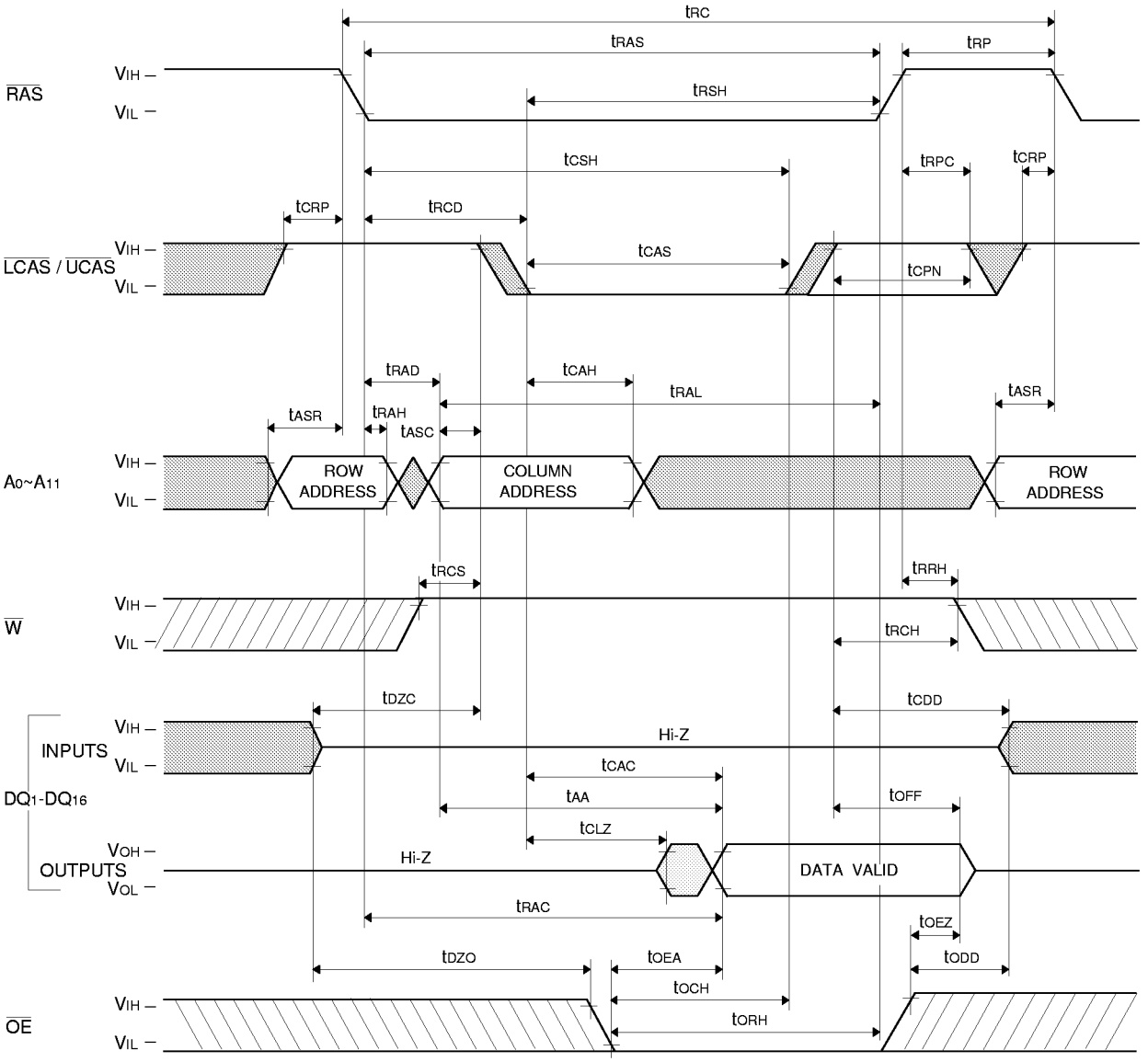

**(2) In case of burst refresh**

The last / first full refresh cycles (4K) must be made within $t_{NS}$ / $t_{SN}$ before / after self refresh, on the condition of $t_{NS}+t_{SN} \leq 64$ms.



**Timing Diagrams** ( Note 28 )

**Read Cycle**



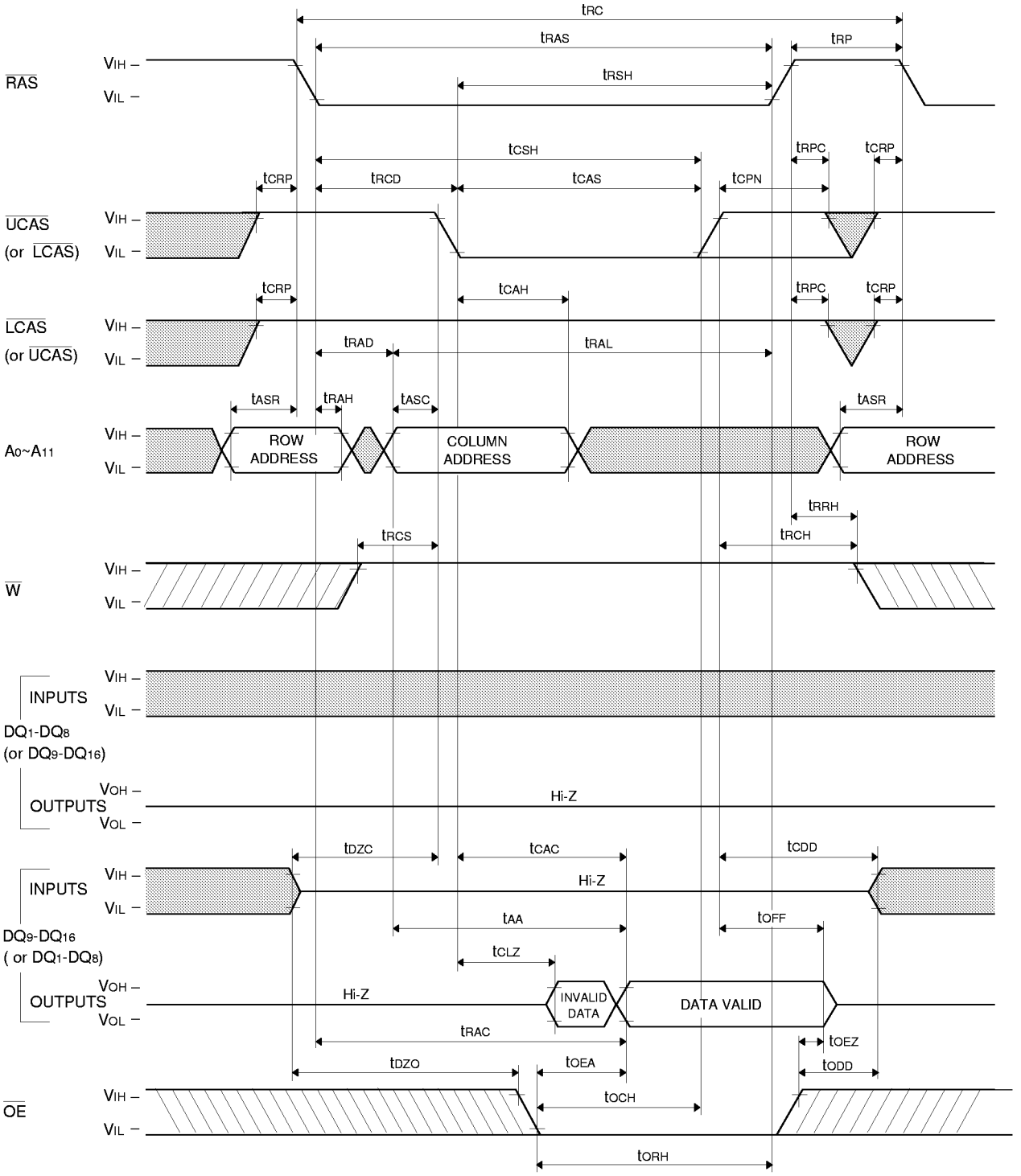

Note 28

Indicates the don't care input.
VIH(min.)≤VIN≤VIH(max) or VIL(min.)≤VIN≤VIL(max)

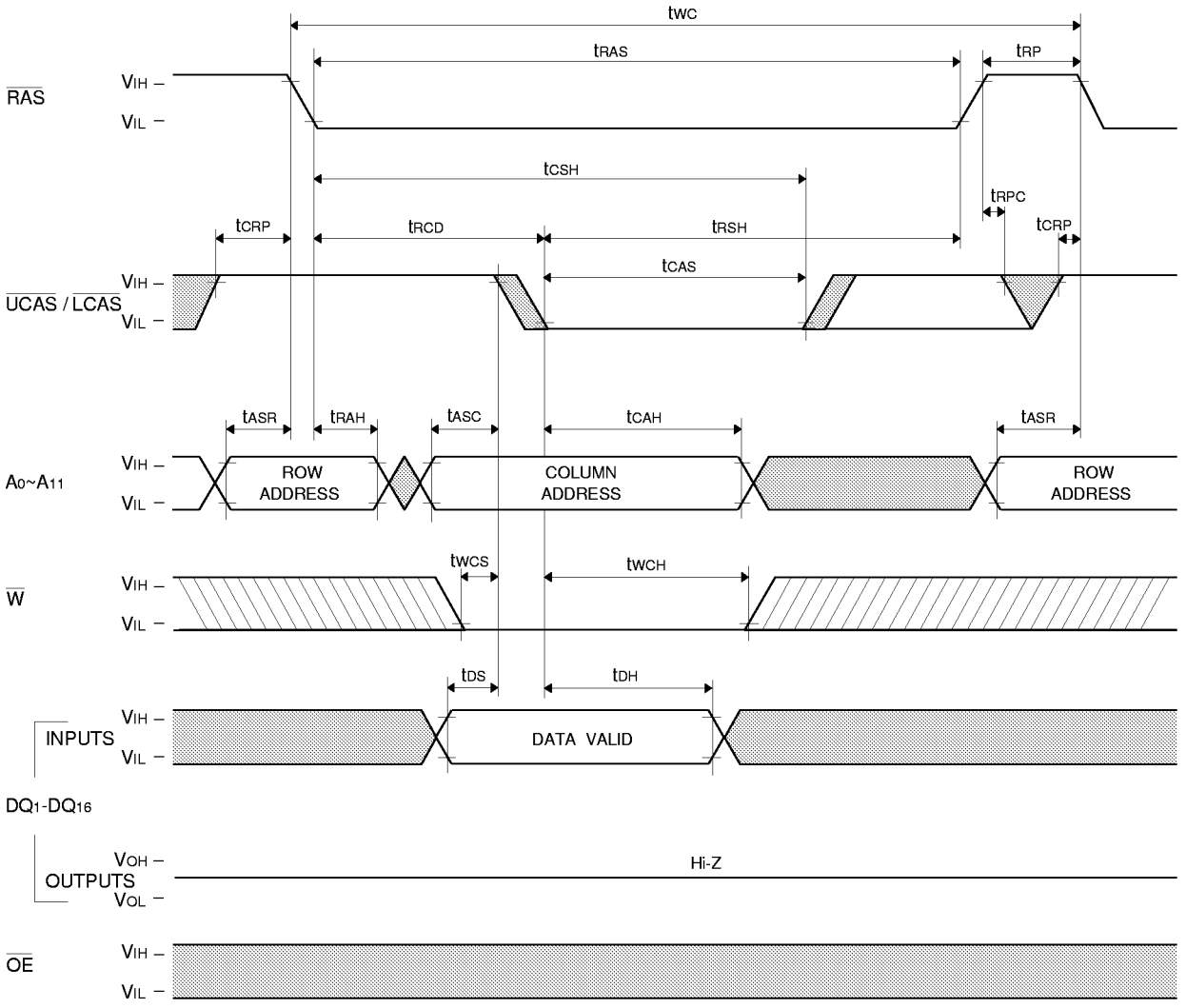
Indicates the invalid output.

Indicates the skew of the two inputs.

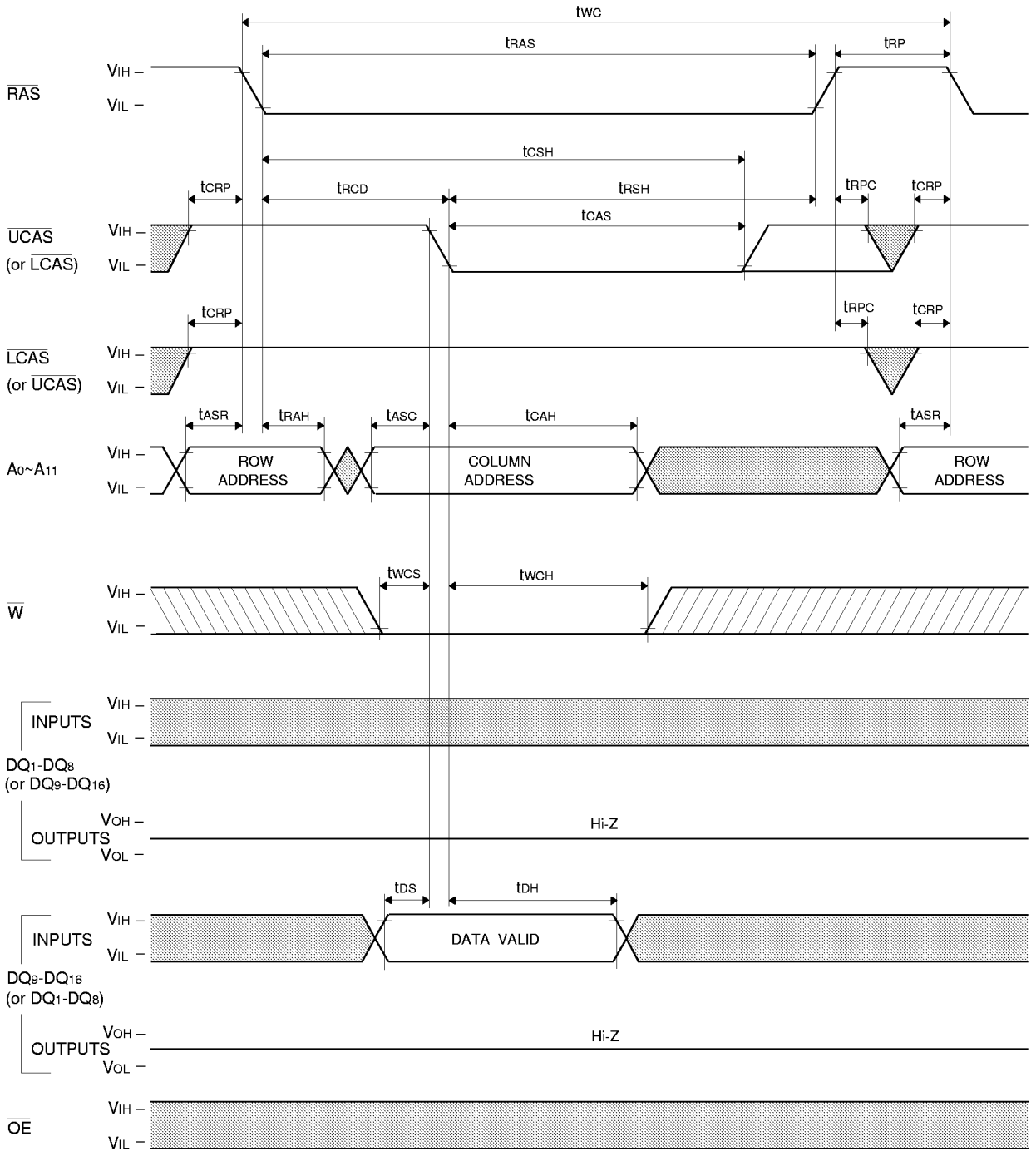
**Upper / (Lower) Byte Read Cycle**



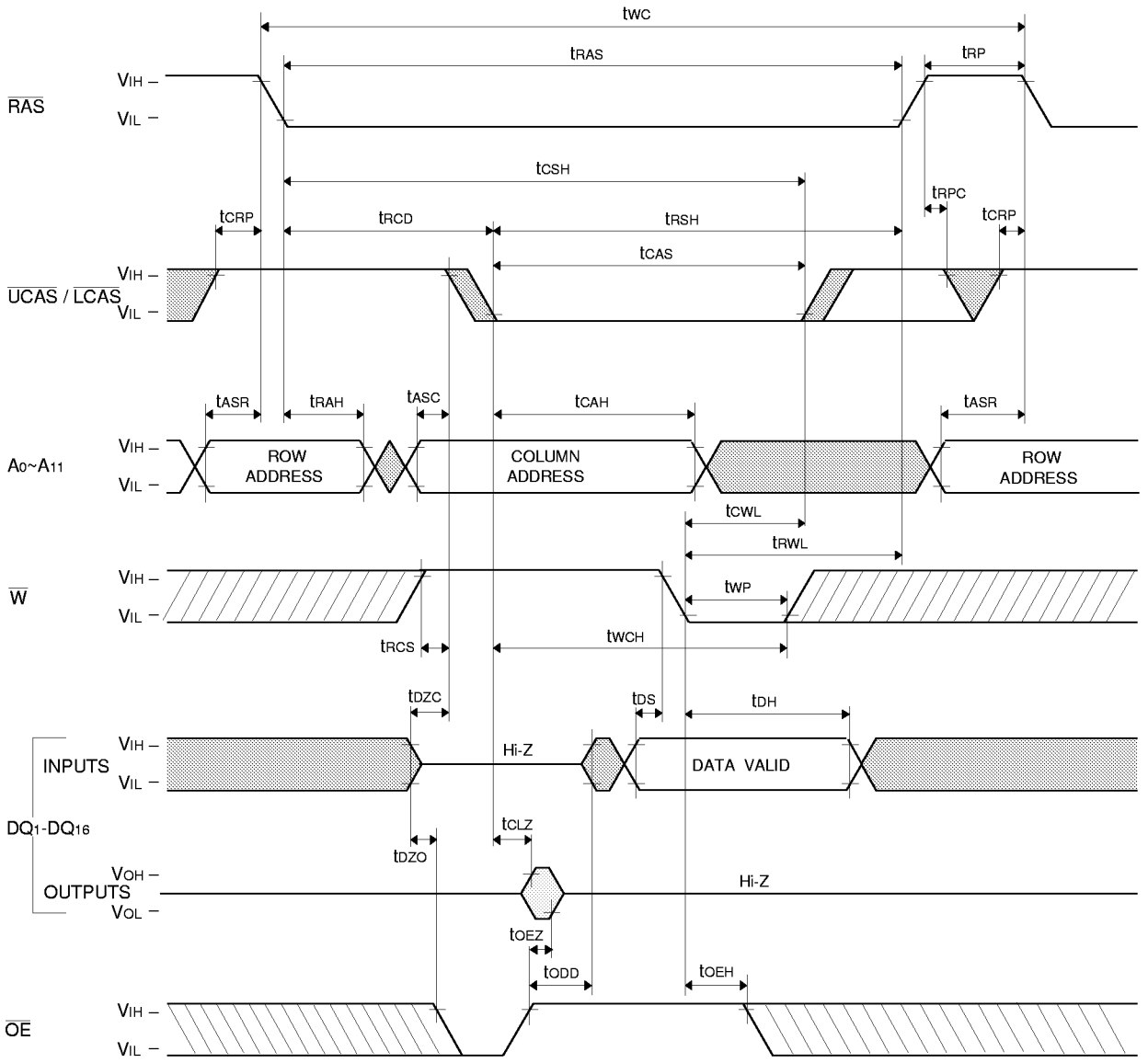
**Write Cycle (Early write)**



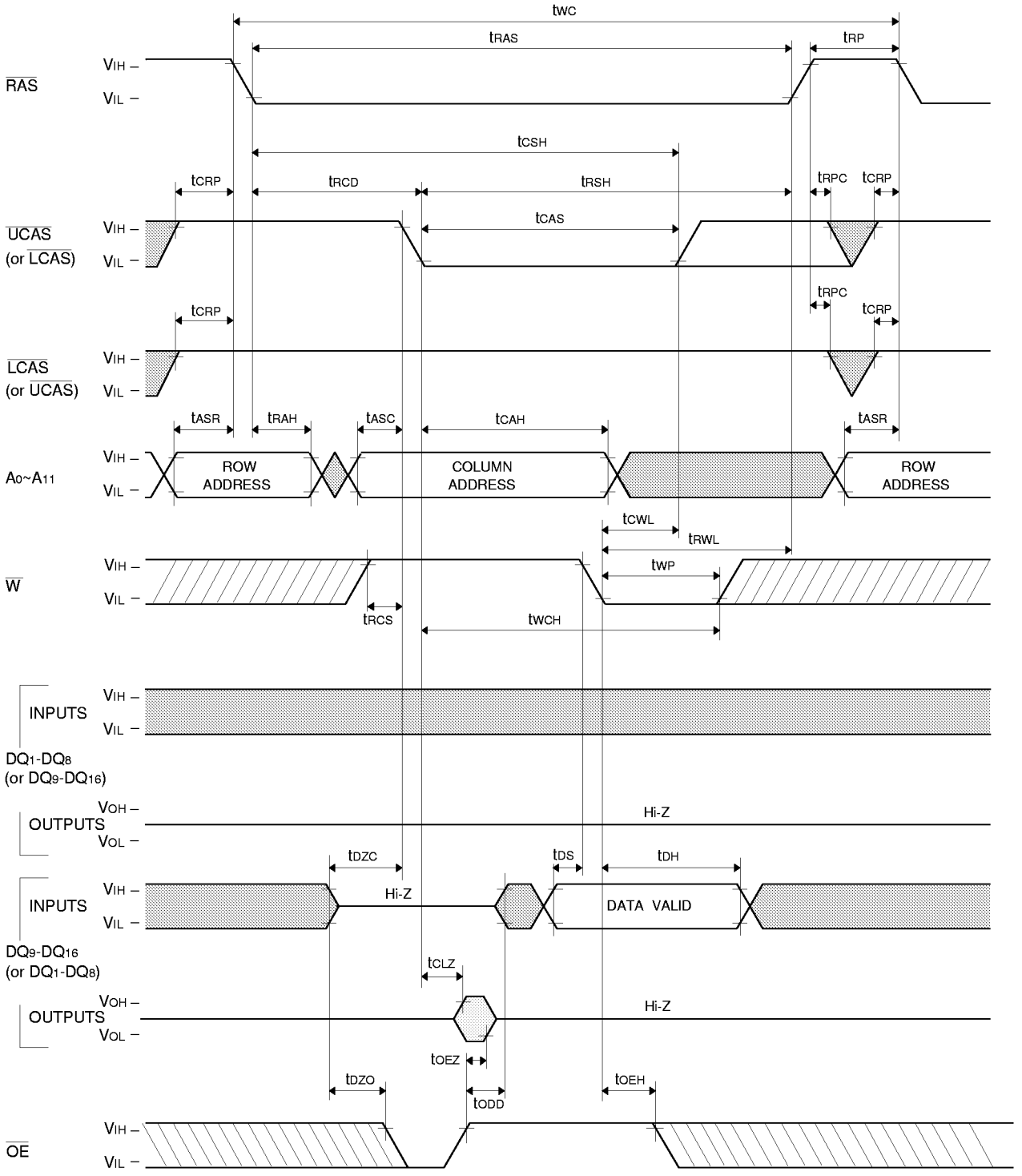
**Upper / (Lower) Byte Write Cycle (Early write)**



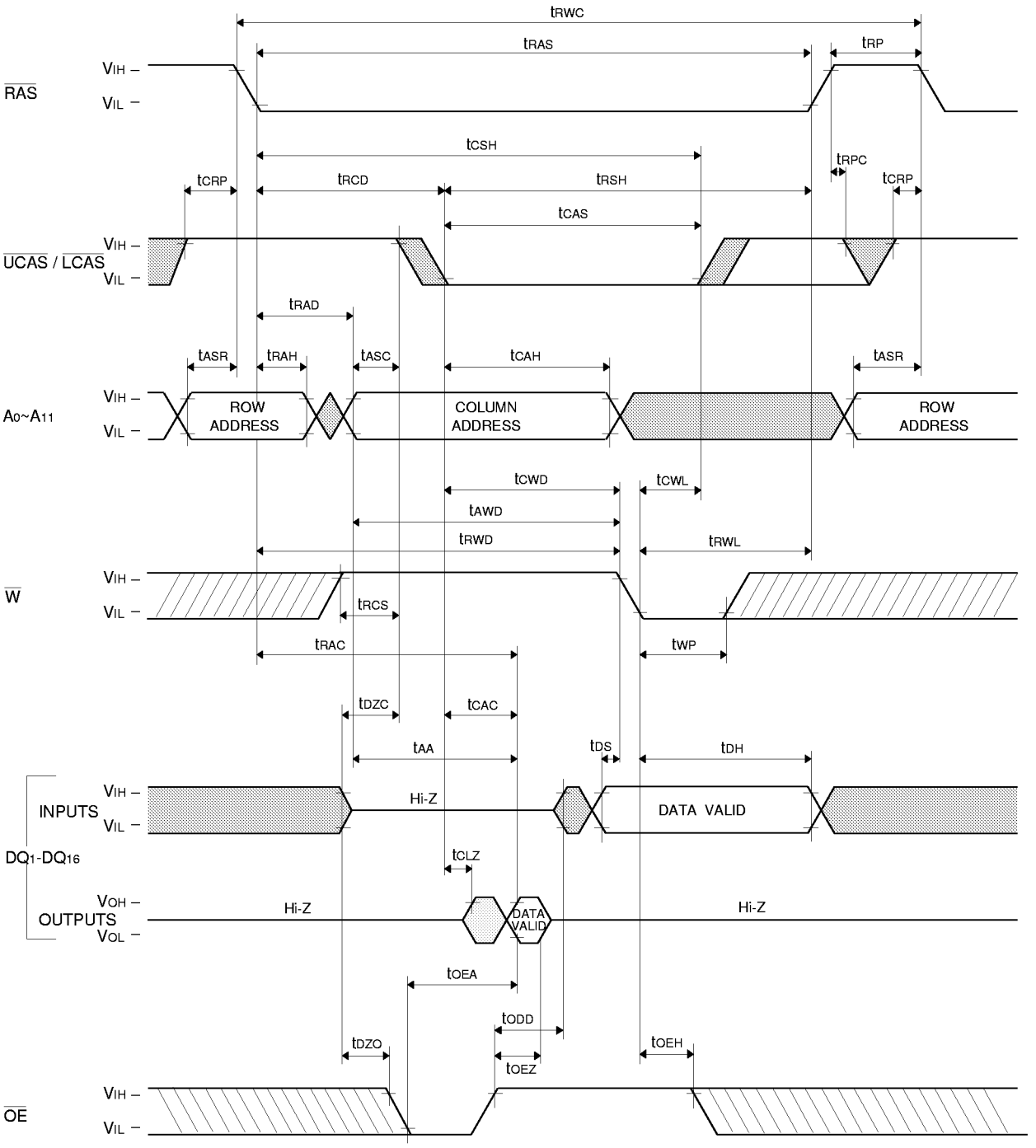
**Write Cycle (Delayed write)**



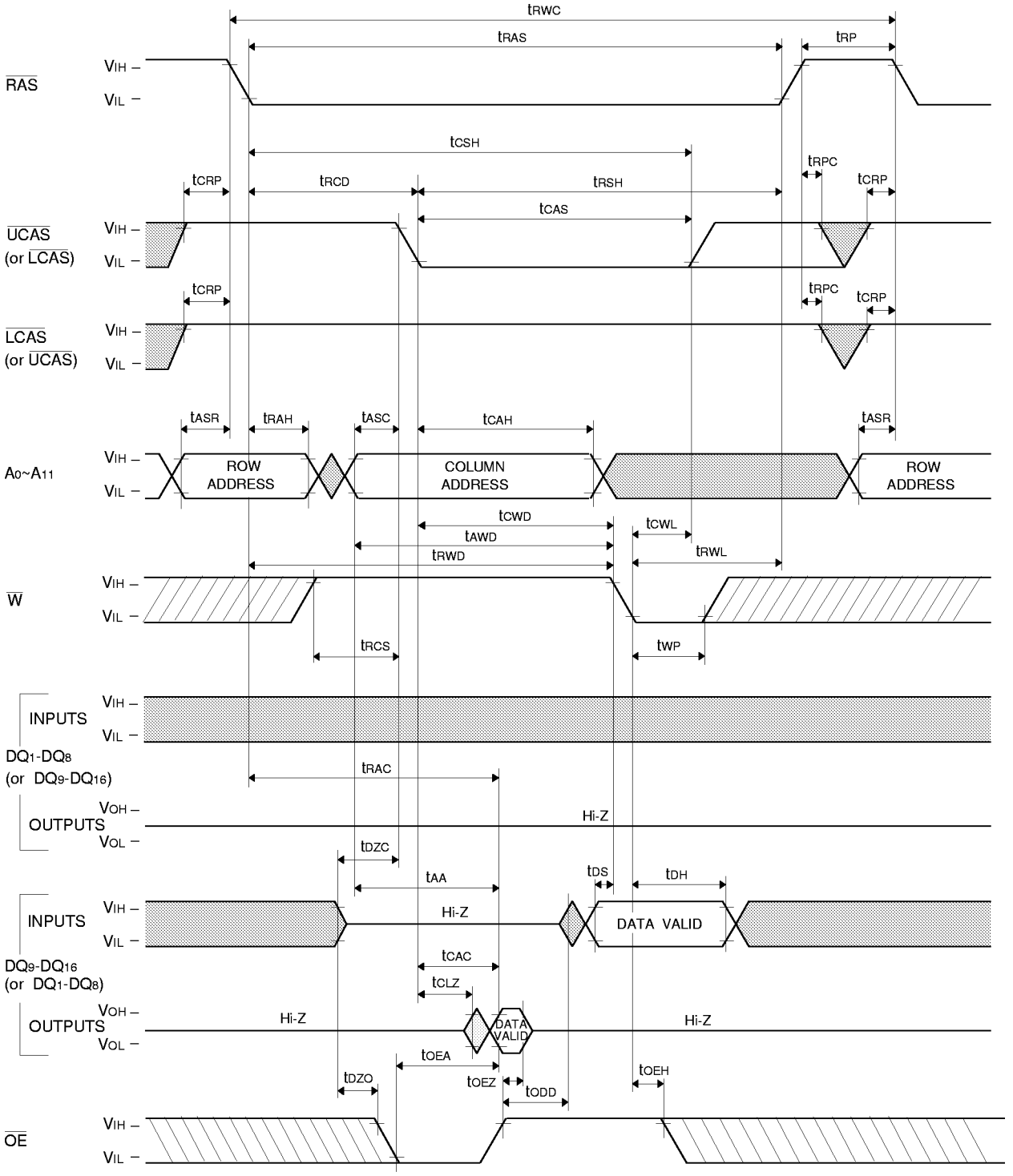
**Upper / (Lower) Byte Write Cycle (Delayed write)**



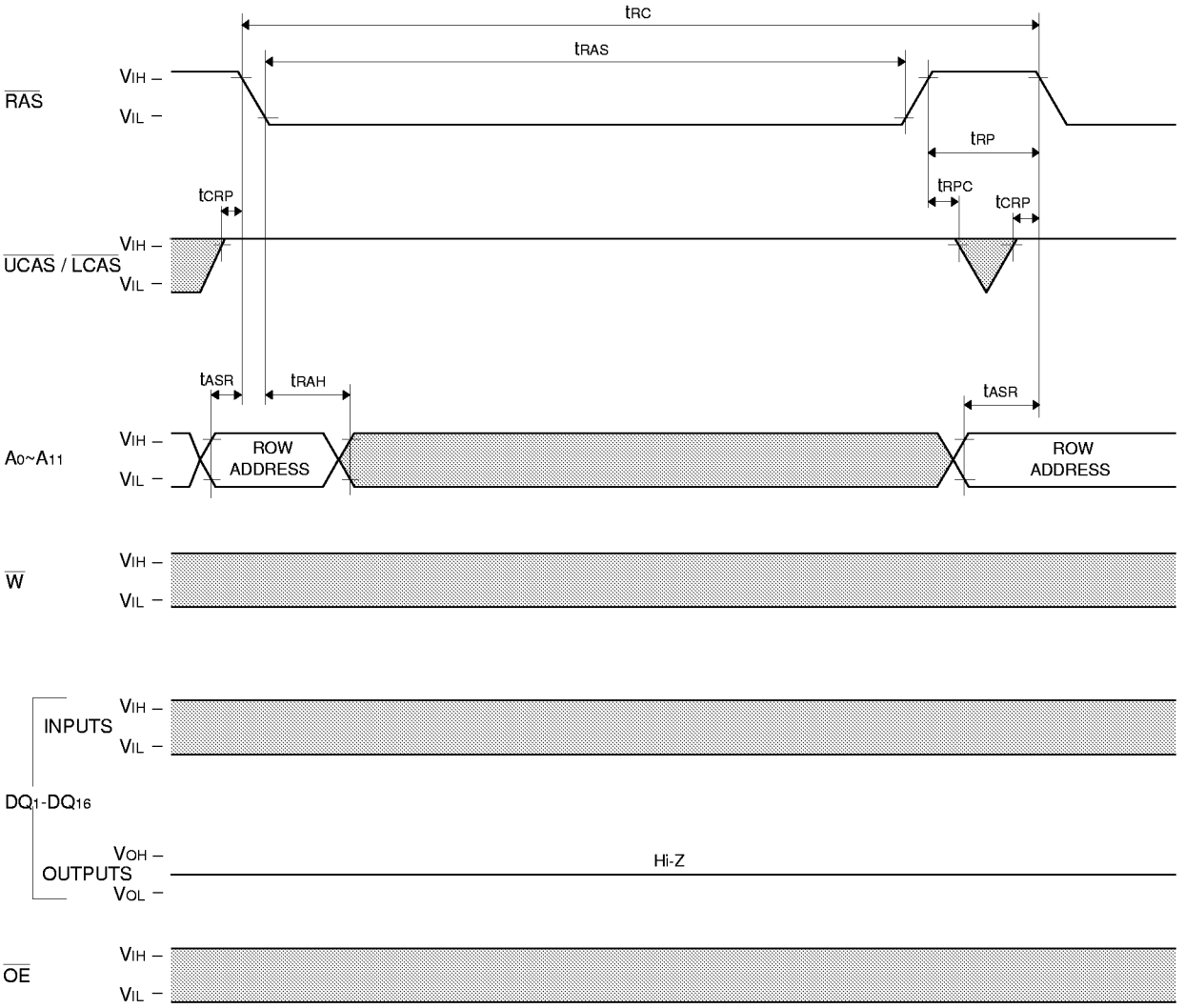
**Read-Write, Read-Modify-Write Cycle**



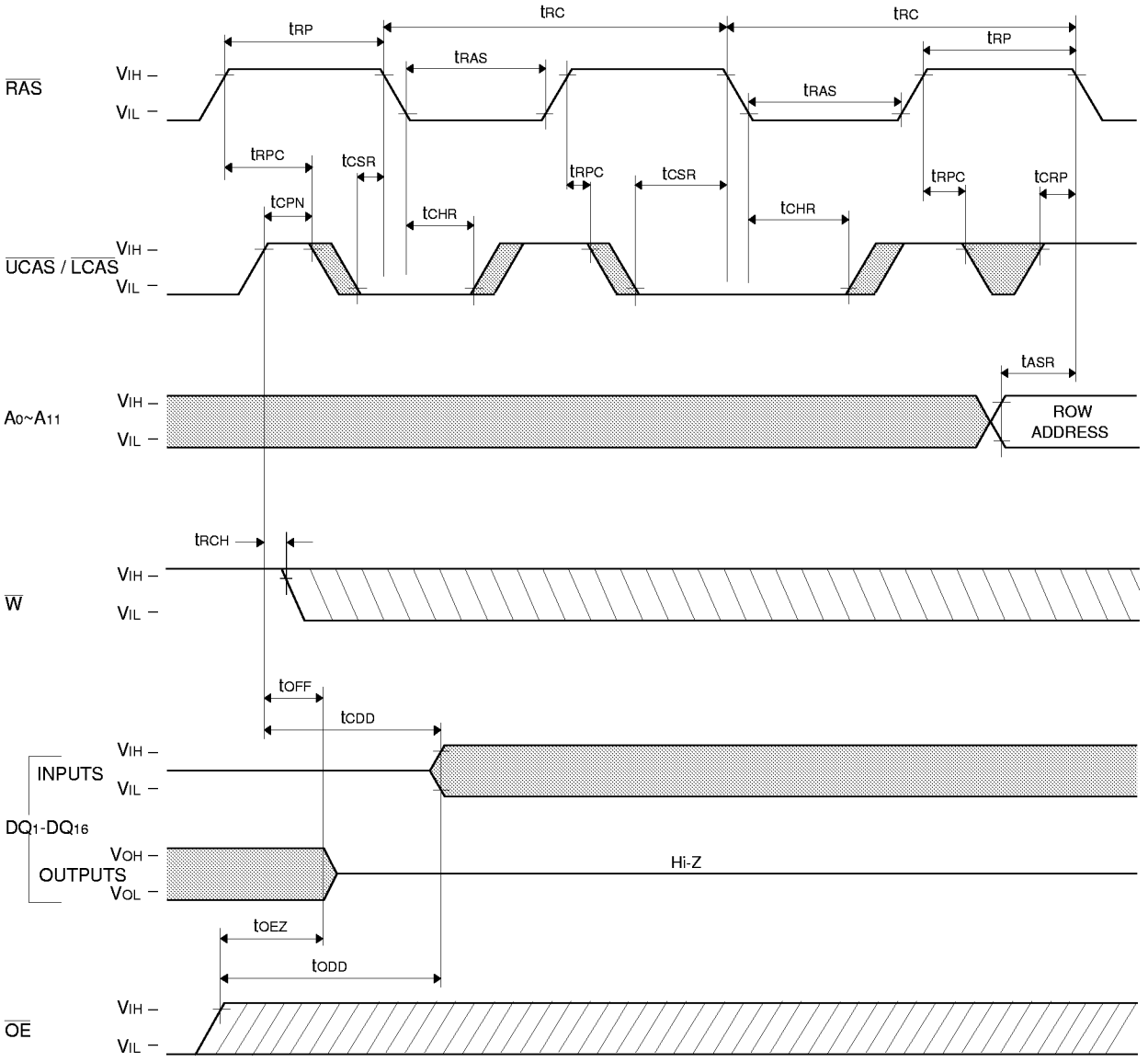
**Read-Upper / (Lower) Write, Read-Modify-Upper / (Lower) Write Cycle**



**$\overline{RAS}$-only Refresh Cycle**

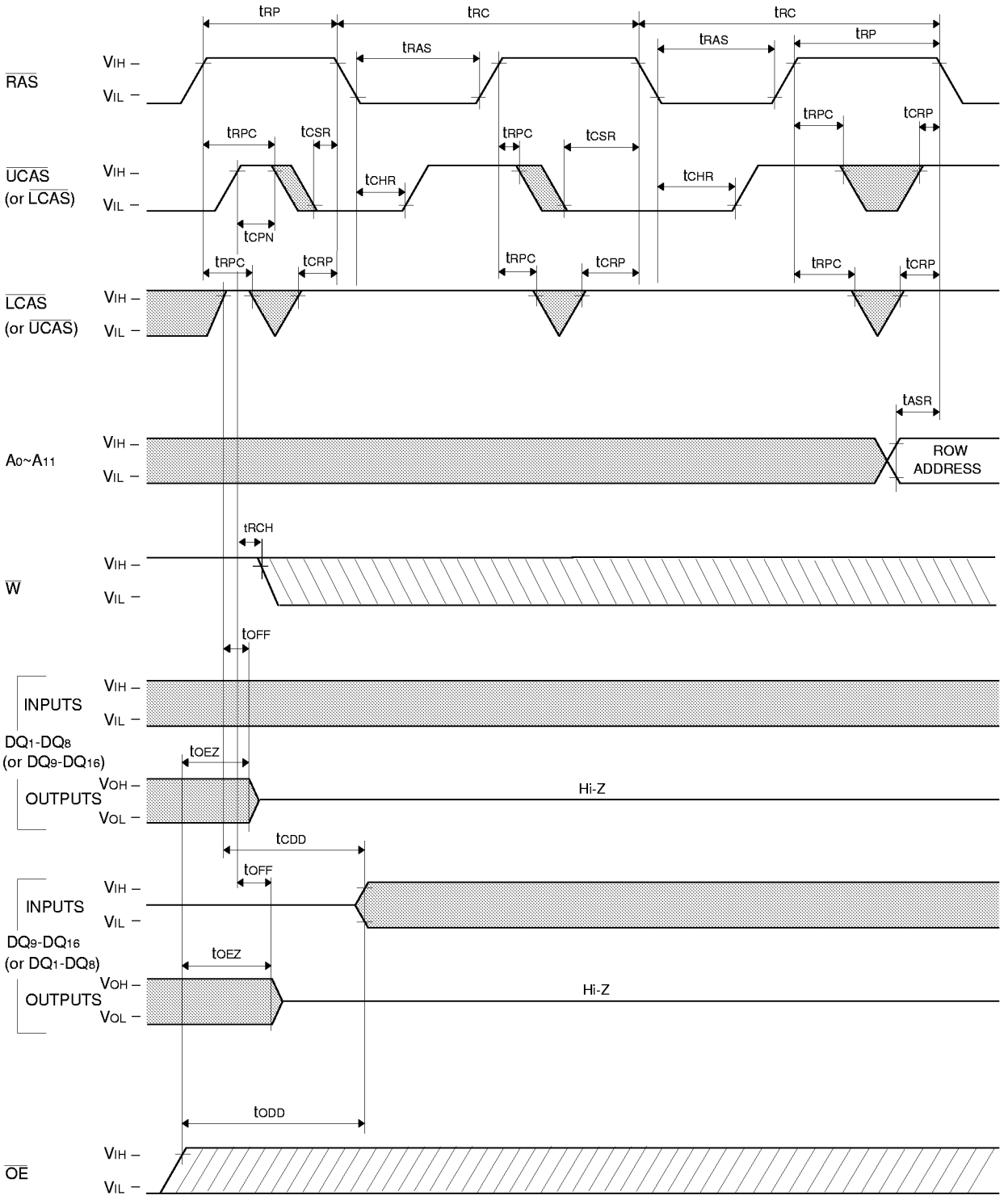


**$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle ***



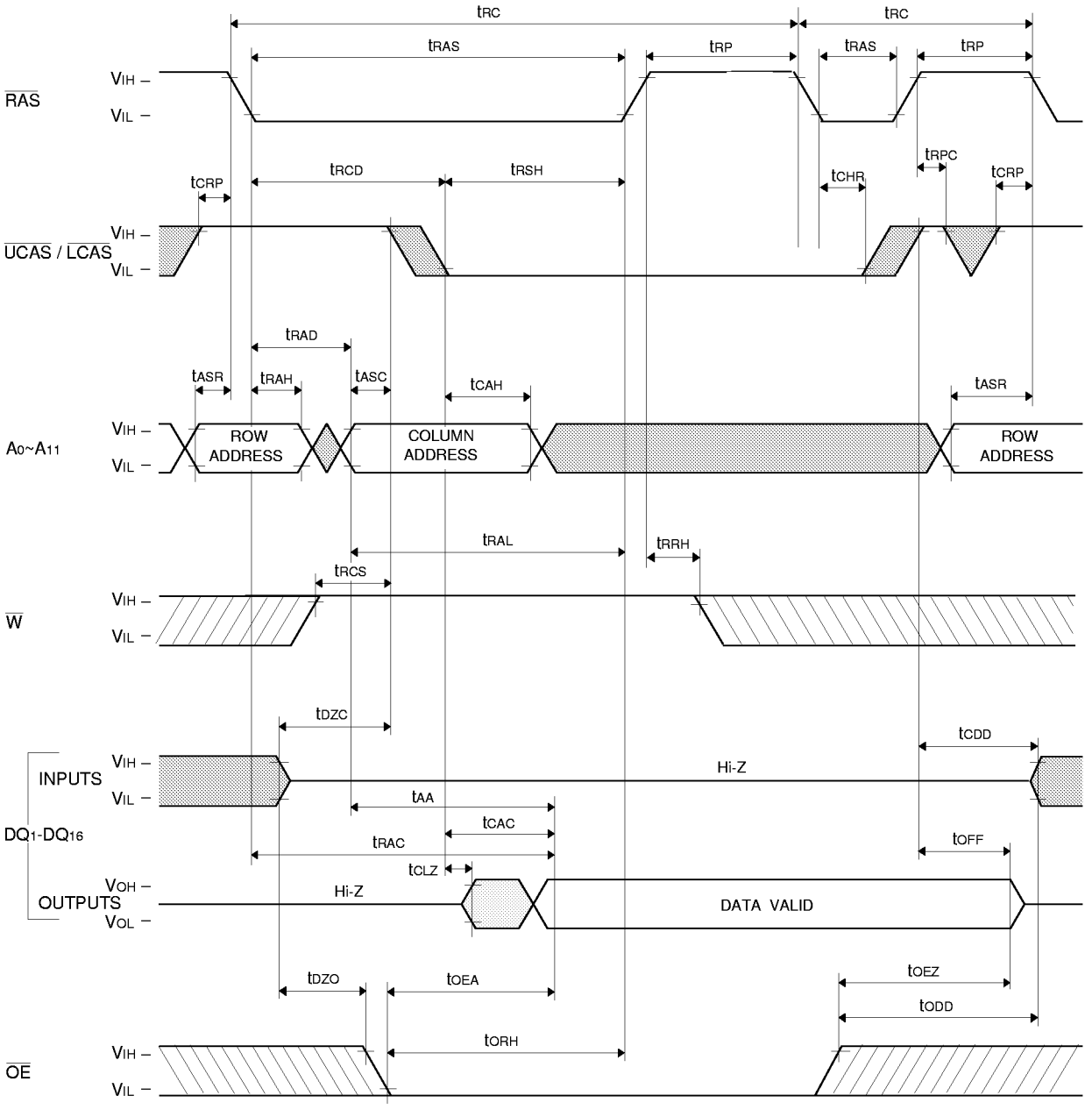

* : Applicable to self refresh version (M5M416160DJ,TP-5S,-6S,-7S : option) only

**Upper / (Lower) $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle ***



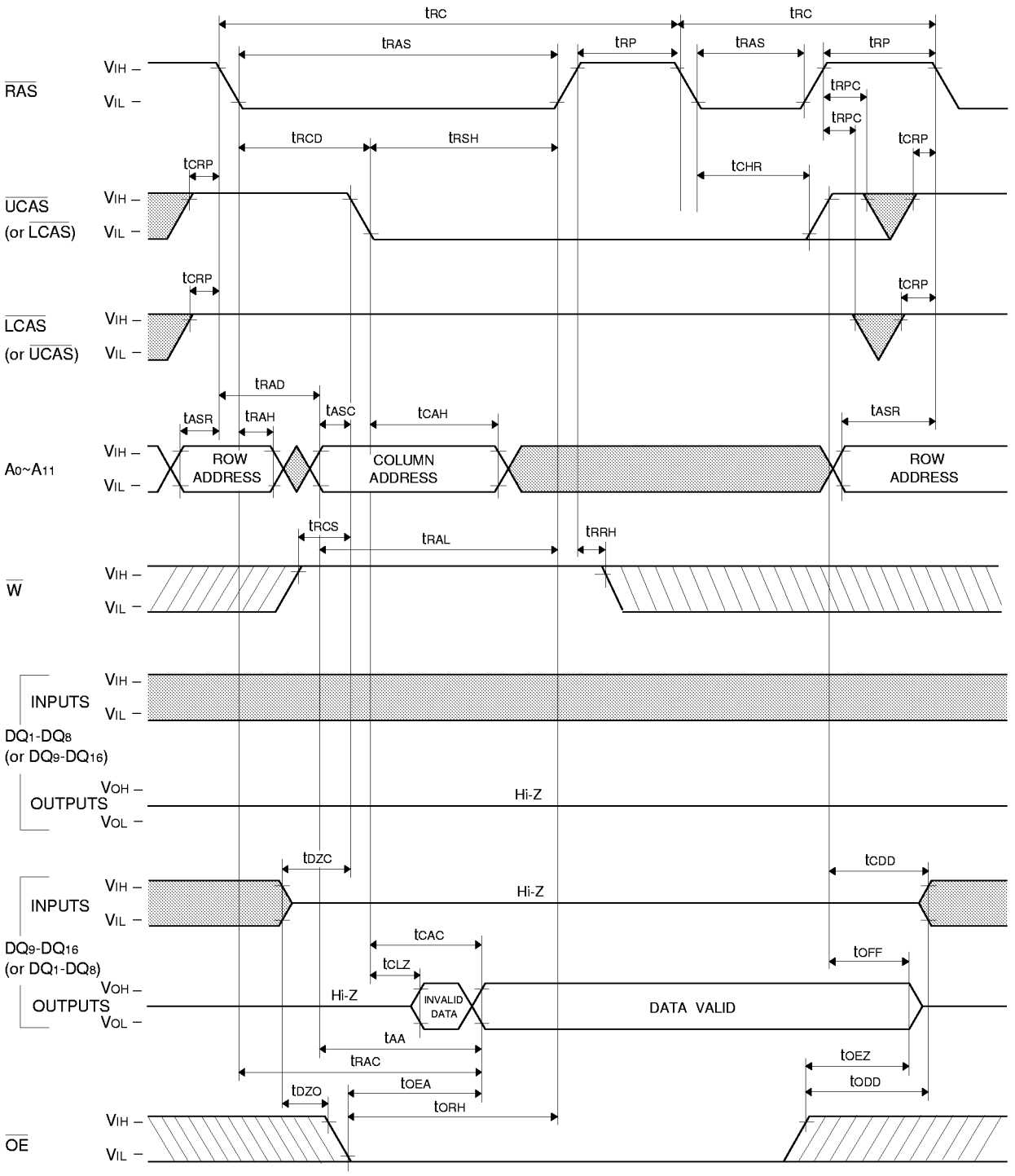

* : Applicable to self refresh version (M5M416160DJ,TP-5S,-6S,-7S : option) only

**Hidden Refresh Cycle (Read)** (Note 29)



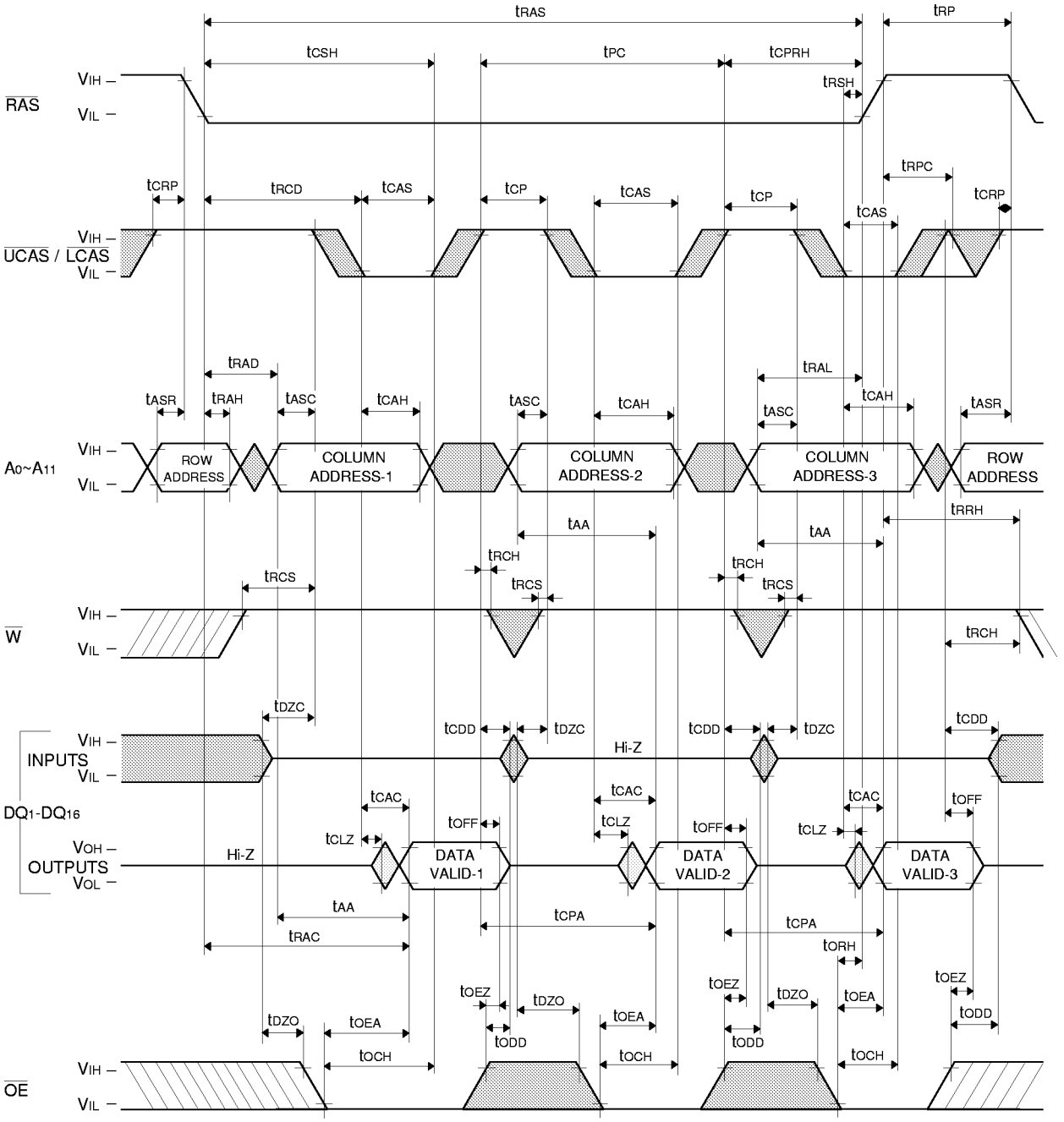

Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

**Upper / (Lower) Hidden Refresh Cycle (Byte Read)** (Note 30)

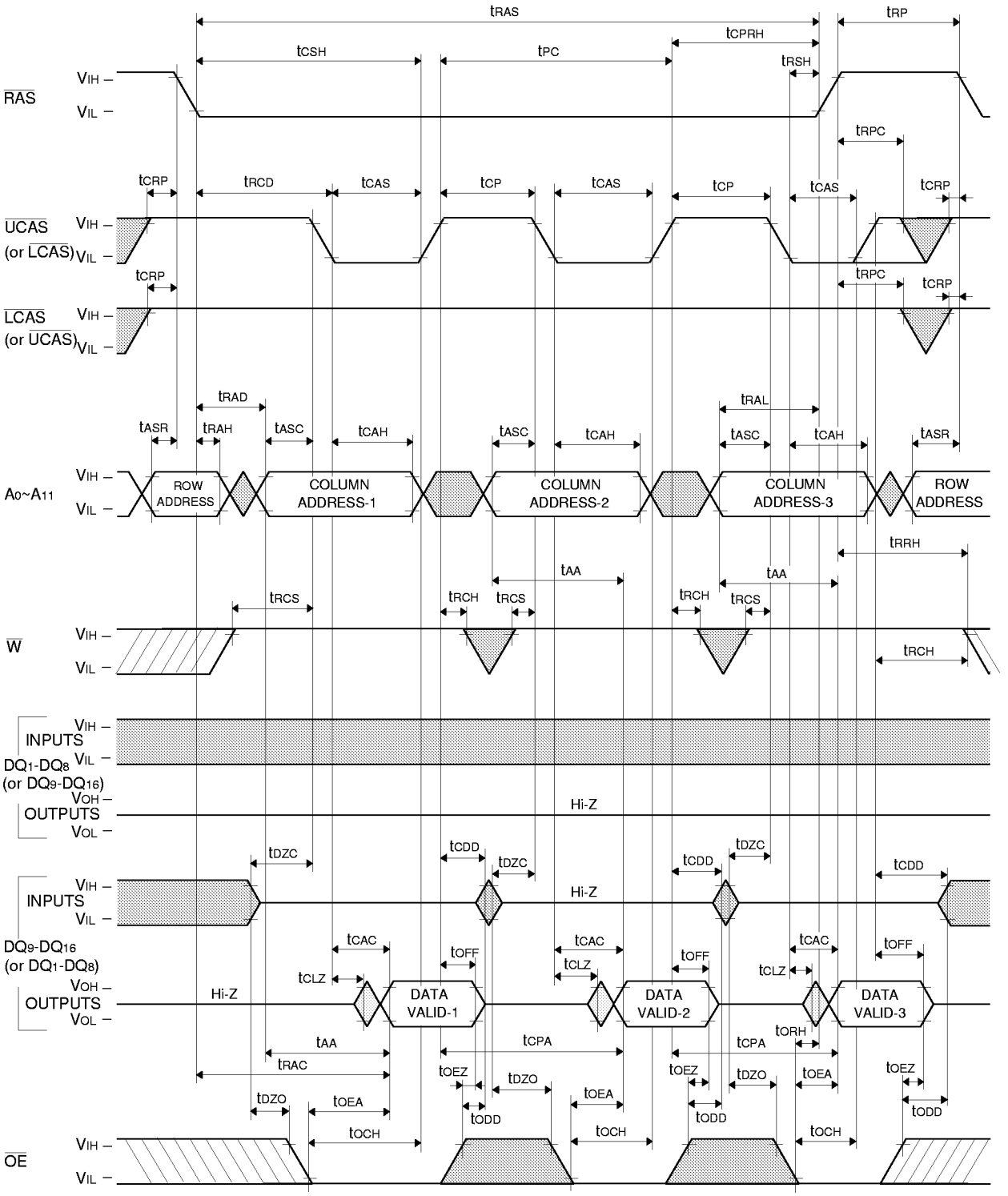



Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

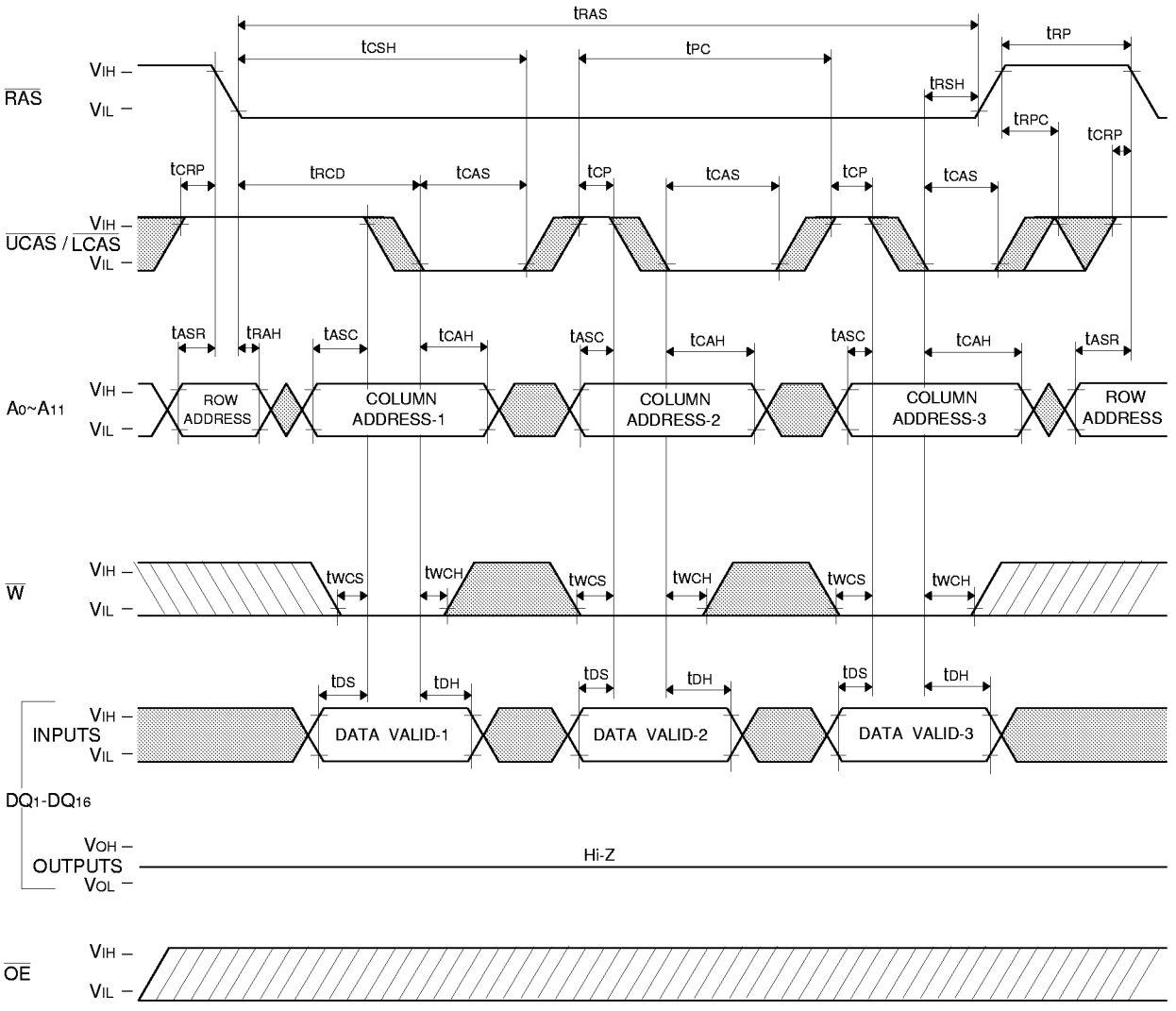
**Fast Page Mode Read Cycle**



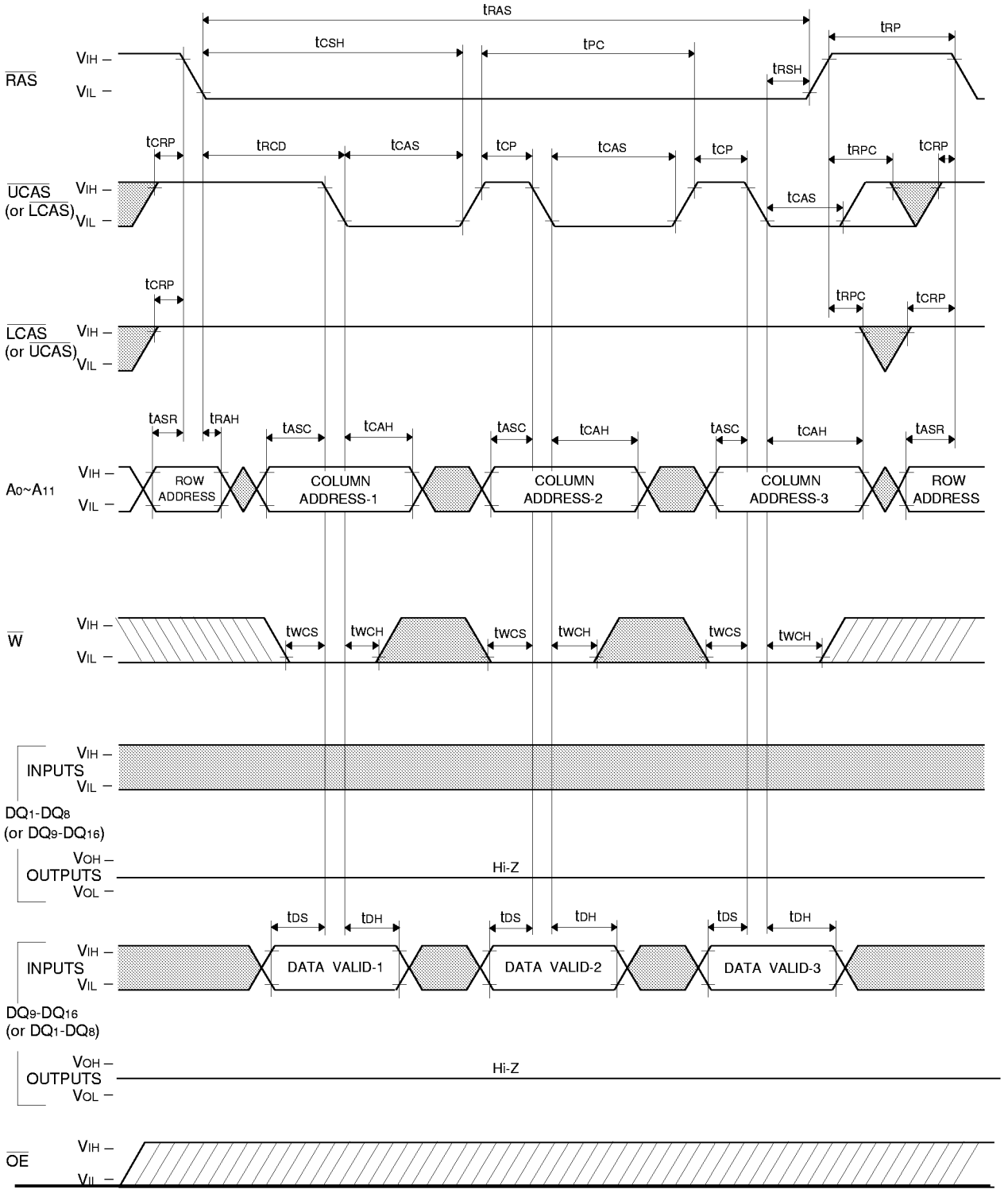
**Upper / (Lower) Fast Page Mode Read Cycle**



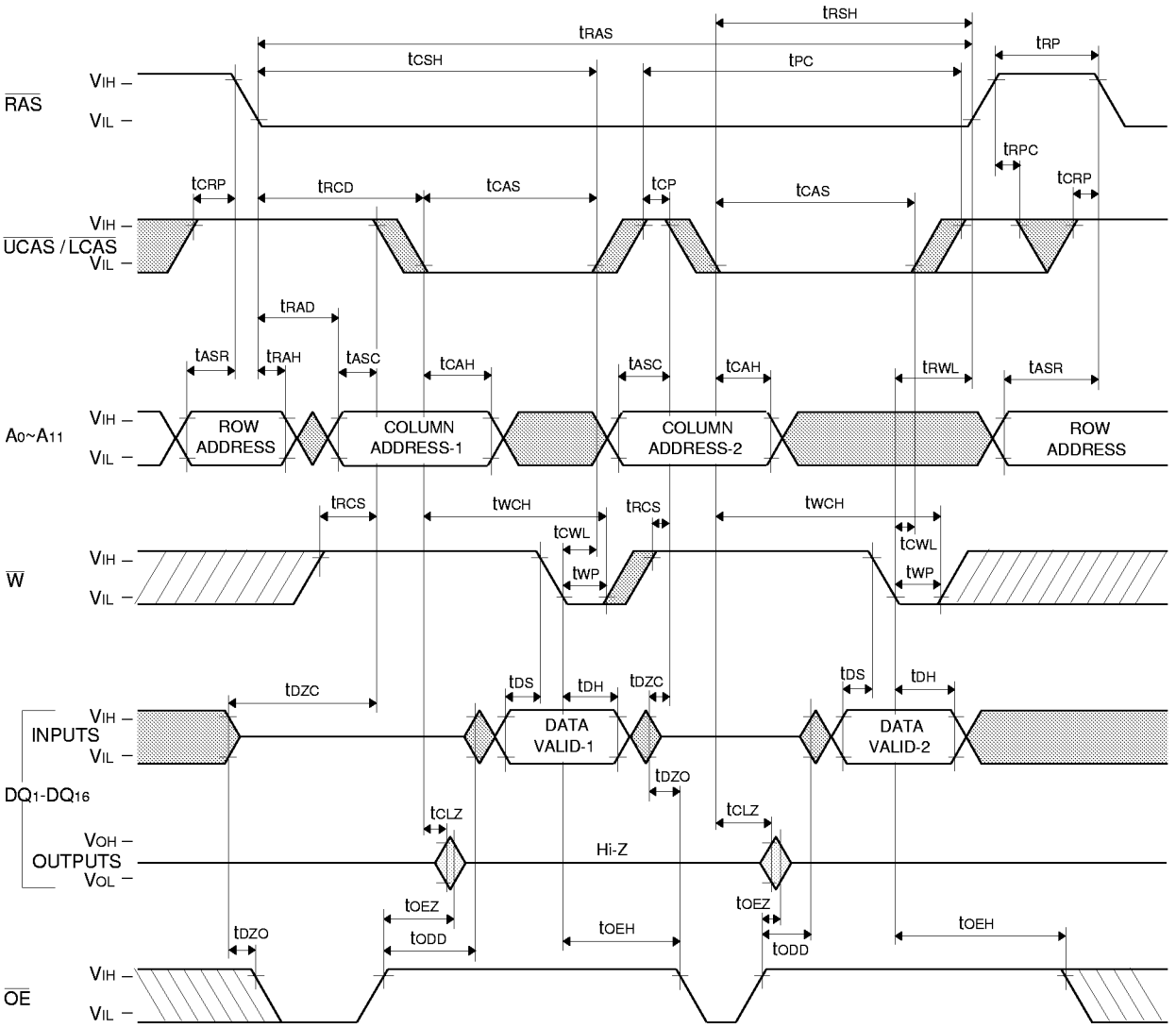
**Fast Page Mode Write Cycle (Early Write)**



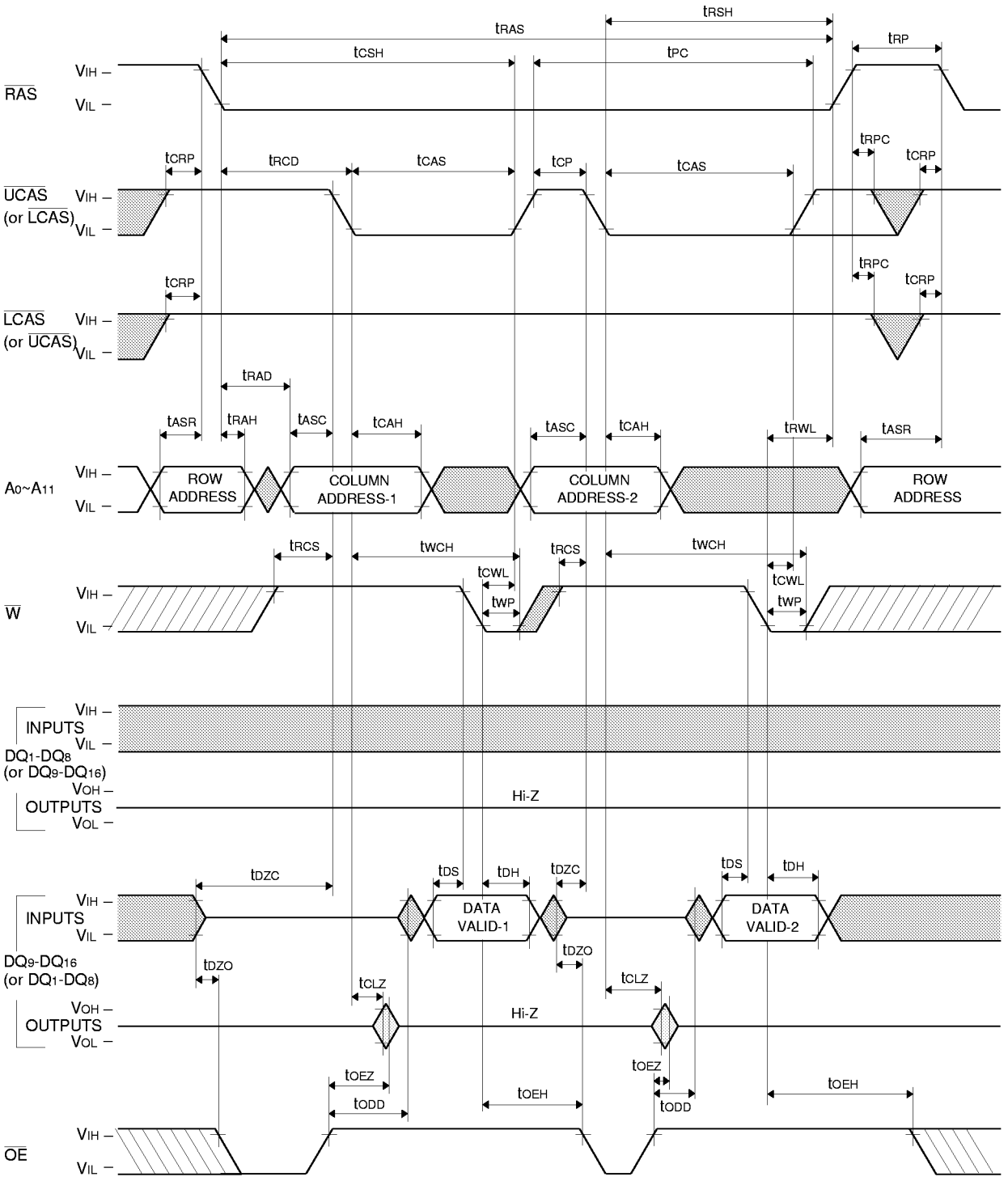
**Fast Page Mode Upper / (Lower) Byte Write Cycle (Early Write)**



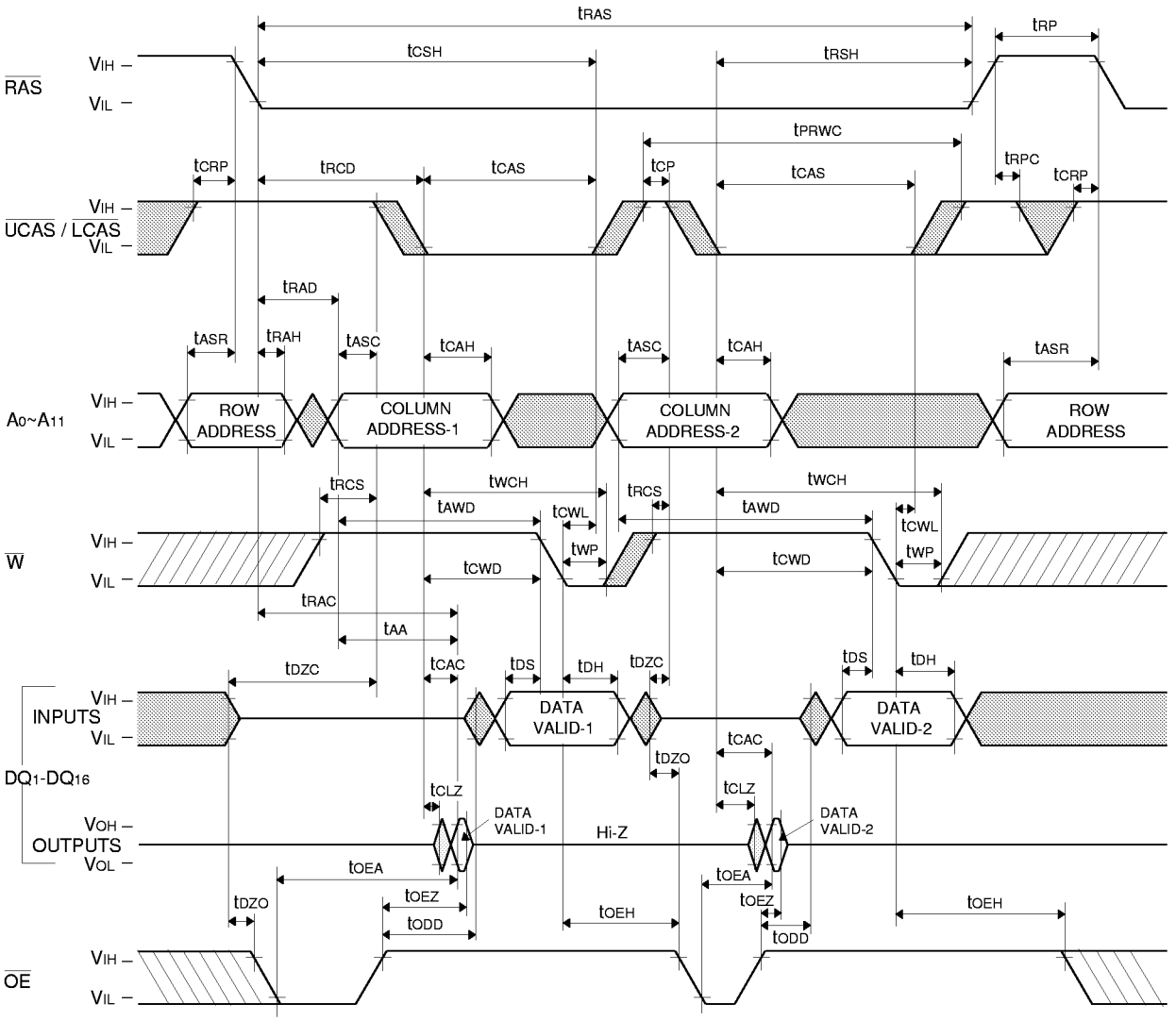
**Fast Page Mode Write Cycle (Delayed Write)**



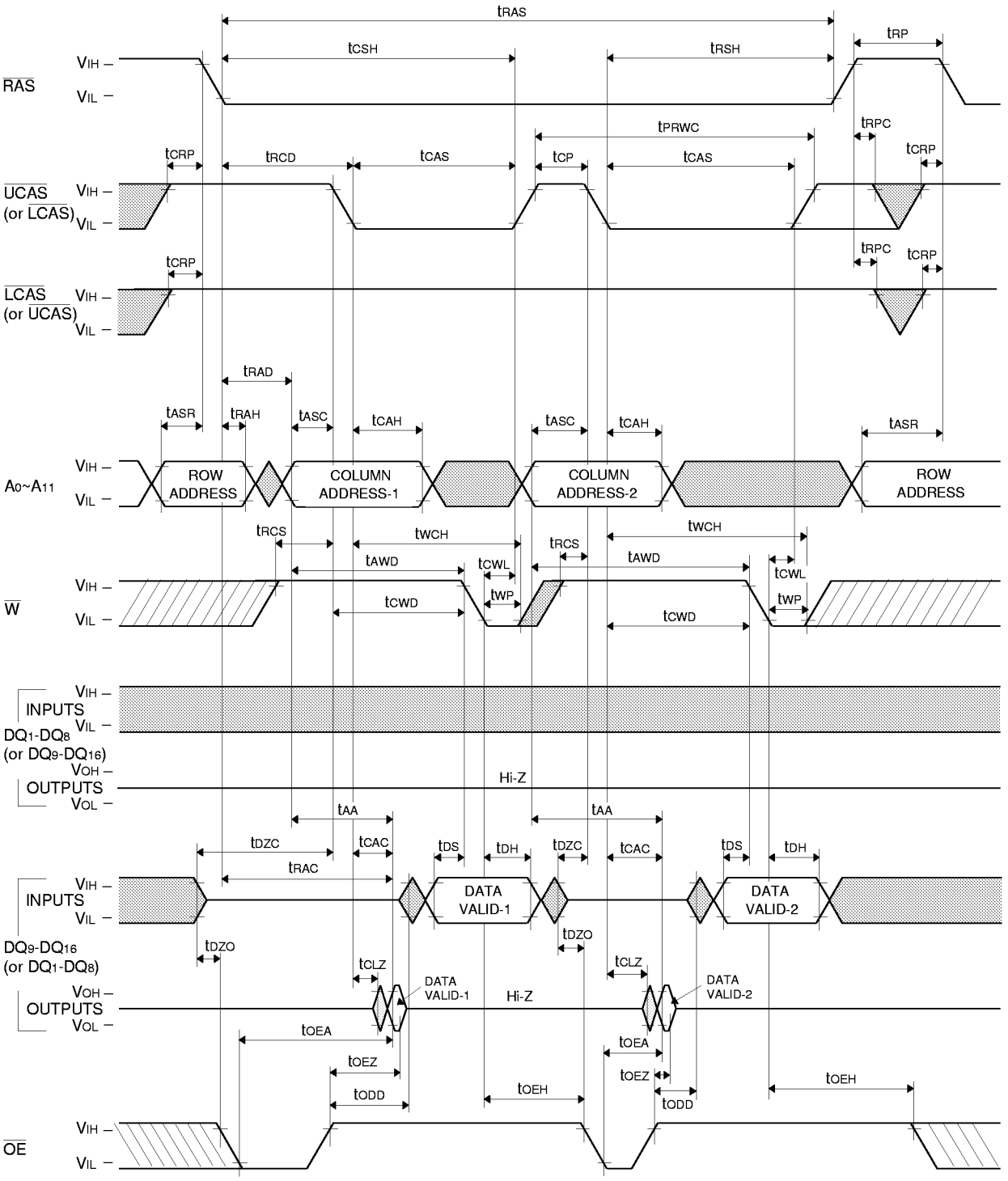
**Fast Page Mode Upper / (Lower) Byte Write Cycle (Delayed Write)**



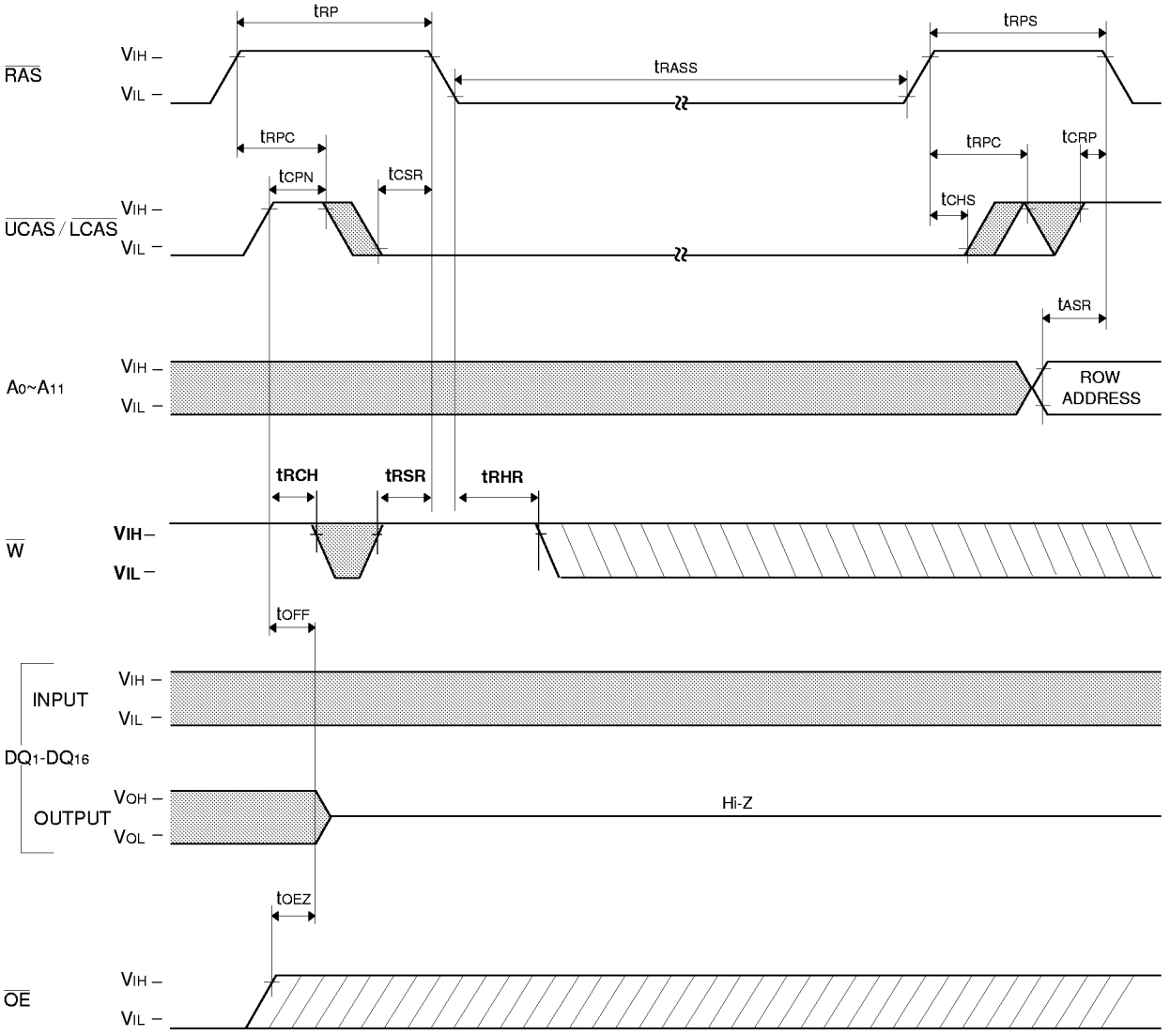
**Fast Page Mode Read-Write, Read-Modify-Write Cycle**



**Fast Page Mode Read-Upper / (Lower) Write, Read-Modify-Upper / (Lower) Write Cycle**

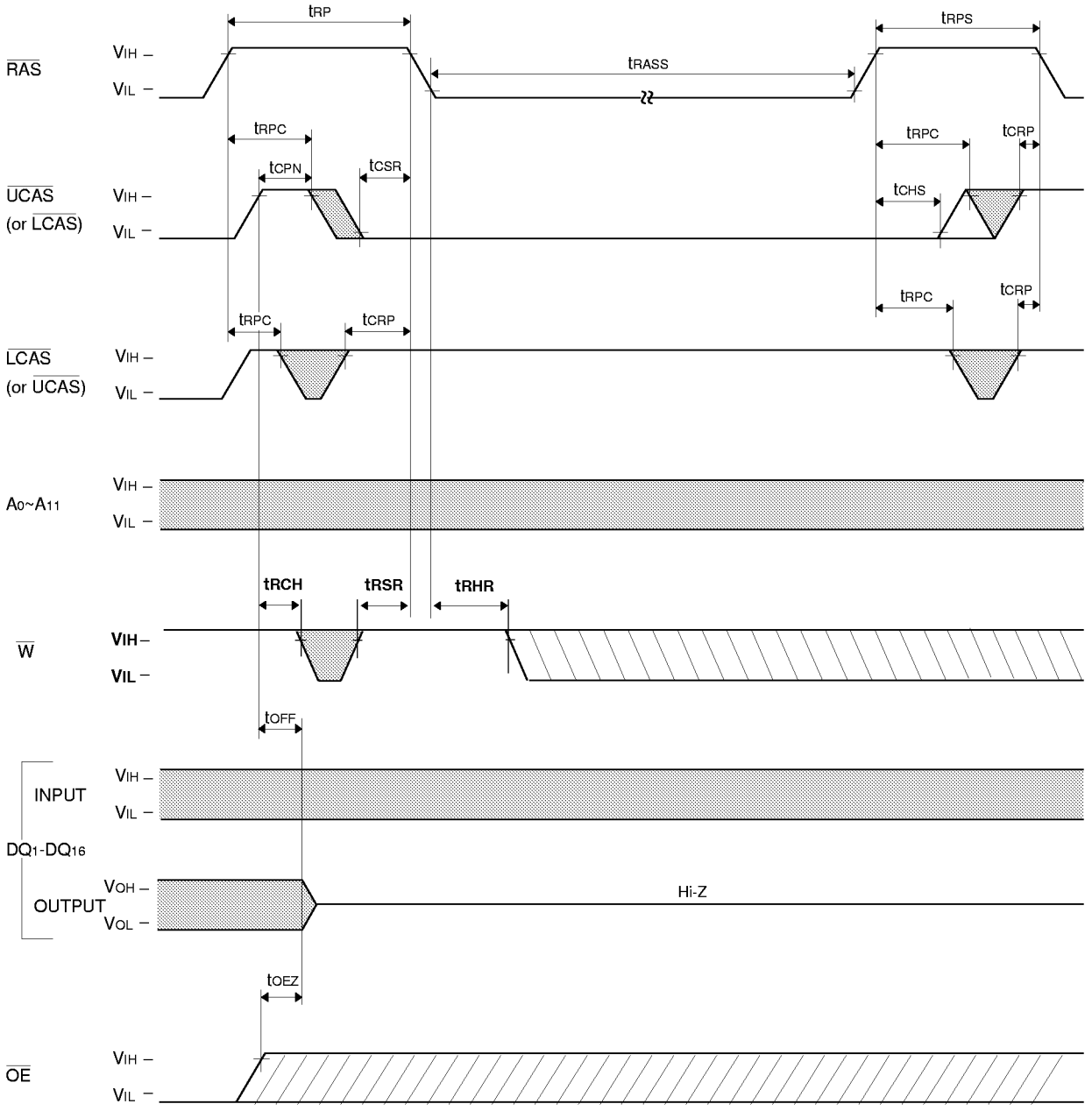


**Self Refresh Cycle***




* : Applicable to self refresh version (M5M416160DJ,TP-5S,-6S,-7S : option) only

**Upper / (Lower) Self Refresh Cycle ***




* : Applicable to self refresh version (M5M416160DJ,TP-5S,-6S,-7S : option) only