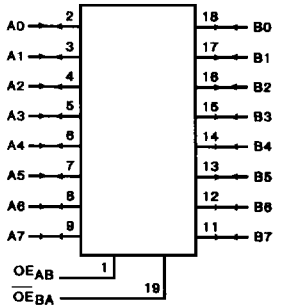
CD54/74FCT7623
CD54/74FCT7623AT

July 1990



FUNCTIONAL DIAGRAM

Octal Bus Transceiver, 3-State (B Side), Open-Drain (A Side), Non-Inverting

Type Features:

- *Buffered inputs*
- *Typical Propagation delay: 5.2ns @ V_{CC} = 5V, T_A = +25°C, C_L = 50pF (FCT7623)*

The CD54/74FCT7623 and CD54/74FCT7623AT octal bus transceivers use a small-geometry BiCMOS technology. The output stages are a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enchances switching speed and is capable of sinking 48 to 64 milliamperes.

The CD54/74FCT7623 and CD54/74FCT7623AT are non-inverting 3-state bidirectional transceiver-buffers intended for two-way transmission from "A" bus to "B" bus or "B" bus to "A" bus, depending on the logic levels of the Output Enable (OE_{AB}, $\overline{OE}_{BA}$) inputs.

This design is a modified version of the CD54/74FCT623. It differs in that the 3-state outputs are on the B side only; the A side outputs are open drain.

The CD54/74FCT7623 and CD54/74FCT7623AT is supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to 70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT7623 is also available in chip form (H suffix). This unpackaged device is operable over the -55°C to +125°C temperature range.

Family Features:

- *SCR-latchup-resistant BiCMOS process and circuit design*
- *FCTXXXX - Speed of bipolar FAST*/AS/S; FCTXXXXAT - 30% faster than FAST/AS/S with significantly reduced power consumption*
- *64/48-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ V_{CC} = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to V_{CC}*
- *BiCMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

OUTPUT ENABLE INPUTS		OPERATION
$\overline{OE}_{BA}$	OE_{AB}	
L	L	B Data to (Open Drain) A Bus
H	H	A Data (TTL) to (3-State) B Bus
H	L	Isolation
L	H	B Data to (Open Drain) A Bus, A Data (TTL) to (3-State) B Bus

H = HIGH level
L = LOW level
To prevent excess currents in the HIGH-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

File Number **2358**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

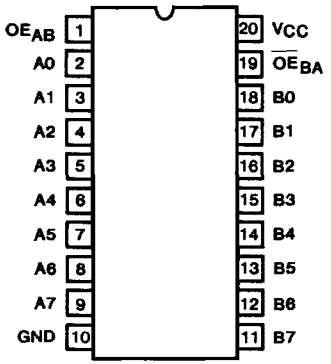
DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5V$) ..... -20mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5V$) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, I_O ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, I_O ..... -30mA
DC V_{CC} CURRENT (I_{CC}) 140mA
DC GROUND CURRENT (I_{GND}) 528mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C (PACKAGE TYPE E) 500mW
For T_A = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For T_A = -55°C to +70°C (PACKAGE TYPE M) 400mW
For T_A = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:

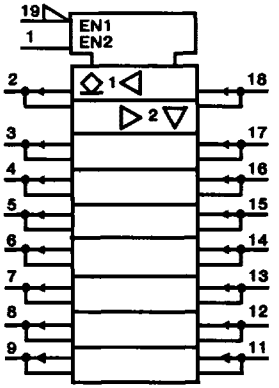
The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, V_{CC}*:	CD74 Series, T_A = 0°C to 70°C	4.75	5.25	V
	CD54 Series, T_A = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, V_I		0	V_{CC}	V
DC Output Voltage, V_O		0	$\leq V_{CC}$	V
Operating Temperature, T_A		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.



TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; V_{CC} max = 5.25V, V_{CC} min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; V_{CC} max = 5.5V, V_{CC} min = 4.5V

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A)						UNITS
					+25°C		0°C to +70°C		-55°C to +125°C		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IH} or	-15	MIN	2.4	-	2.4	-	-	-	V
		V_{IL}	-12	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	V_{OL}	V_{IH} or	64	MIN	-	0.55	-	0.55	-	-	V
		V_{IL}	48	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	I_{IH}	V_{CC}		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	I_{IL}	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	I_{OZH}	V_{CC}		MAX	-	0.5	-	10	-	10	µA
	I_{OZL}	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	I_{OS}	V_{CC} or GND $V_O = 0$		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at V_{CC} or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

SWITCHING CHARACTERISTICS

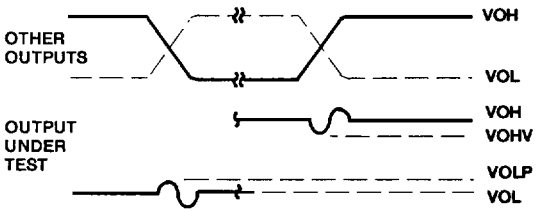
FCT Series: t_r, t_f = 2.5ns, C_L = 50pF, R_L = See Figure 4

CHARACTERISTICS	SYMBOL	V_{CC} (V)	CD54/74FCT7623					CD54/74FCT7623AT					UNITS
			AMBIENT TEMPERATURE (T_A)										
			+25°C	0°C to +70°C		-55°C to +125°C		+25°C	0°C to +70°C		-55°C to +125°C		
			TYP	MIN	MAX	MIN	MAX	TYP	MIN	MAX	MIN	MAX	
Propagation Delays: A Data to B Bus	t_{PLH}, t_{PHL}	5†	5.3	1.5	7	1.5	7.5						ns
B Data to A Bus	t_{PZL}	5	5.3	1.5	7	1.5	7.5						ns
	t_{PLZ}	5	9.8	1.5	13	1.5	13.5						ns
Output Enable or Disable to Output 3-State (B Side)	t_{PZH}, t_{PZL} t_{PLZ}, t_{PHZ}	5	5.6	1.5	7.5	1.5	10						ns
Off-State Enabling, Disabling Times (A Side)	t_{PZL}, t_{PLZ}	5	7.1	1.5	9.5	1.5	10						ns
Power Dissipation Capacitance	C_{PD}§	-	33 Typical					33 Typical					pF
Min. (Valley) V_{OHV} (B Side) During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Figure 1	5	0.5 Typical @ +25°C										V
Max. (Peak) V_{OLP} During Switching of Other Outputs(Output Under Test Not Switching)	V_{OLP} See Figure 1	5	1 Typical @ +25°C										V
Input Capacitance	C_I	-	-	-	10	-	10	-	-		-		pF
3-State Output Capacitance (B Side)	C_O	-	-	-	15	-	15	-	-		-		pF
Off-State Output Capacitance (A Side)	C_O	-	-	-	15	-	15	-	-		-		pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C
typ. is @ 5V

§C_{PD}, measured per function, is used to determine the dynamic power consumption.
P_D (per package) = V_{CC} I_{CC} + Σ (V_{CC}^2 f_i C_{PD} + V_O^2 f_o C_L + V_{CC} ΔI_{CC} D) where:
V_{CC} = supply voltage
ΔI_{CC} = flow through current x unit load
C_L = output load capacitance
D = duty cycle of input high
f_o = output frequency
f_i = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
2. Input pulses have the following characteristics: PRR $\leq$ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

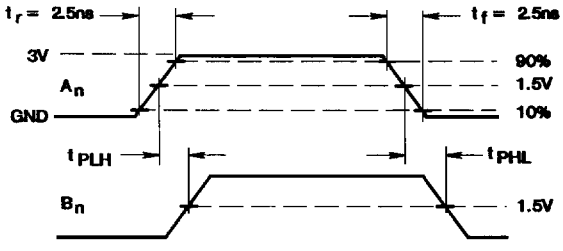


Figure 2 - Propagation delay times (A Data to B Bus).

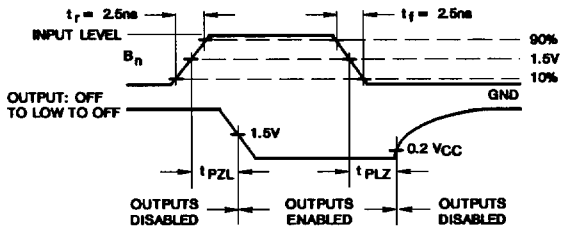
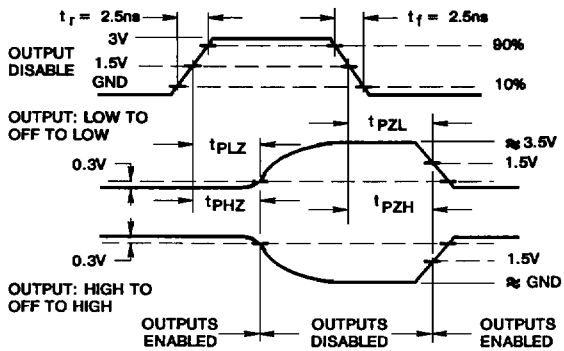
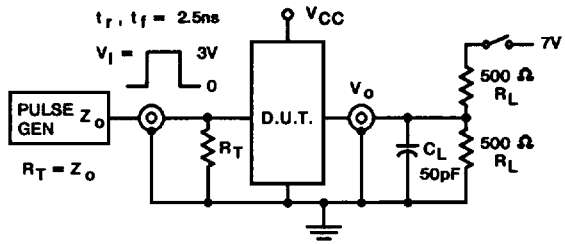


Figure 3 - Open-drain propagation delay times (B Data to A Outputs).





TEST	SWITCH POSITION
t_{PLZ}, t_{PZL}, OPEN DRAIN	CLOSED
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	OPEN

Figure 4 - Three-state propagation delay times and test circuit.