# 512Kx8 MONOLITHIC FLASH

*PRELIMINARY**

## FEATURES

- Access Times of 70, 90, 120 and 150nS
- Packaging
  - 32 pin, Hermetic Ceramic, 0.600" DIP (Package 300)
  - 32 lead, Hermetic Ceramic, 0.400" SOJ (Package 101)
  - 32 pin, Rectangular Cermamic Leadless Chip Carrier (Package 601)
  - 32 lead Flat Pack(1) (Package 201)
- 10,000 Erase/Program Cycles
- Sector Erase Architecture
  - 8 equal size sectors of 64K bytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Organized as 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Programming. 5V ±10% Supply.
- Low Power CMOS, 30mA Read Current, Typical
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Built in Decoupling Caps for Low Noise Operation
- Page Program Operation and Internal Program Control Time.

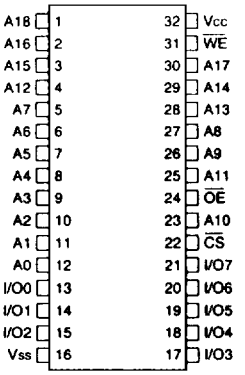
* *This data sheet describes a product under development and is subject to change or cancellation without notice.*

*Note: Programming information available upon request.*

### PIN CONFIGURATION FOR WMF512K8-XXX5

**32 DIP**
**32 CSOJ**
**32 FP(1)**

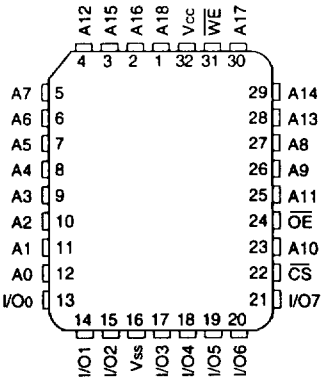
**TOP VIEW**




### PIN CONFIGURATION FOR WMF512K8-XCLX5

**32 CLCC**

**TOP VIEW**




### PIN DESCRIPTION

| | |
|---|---|
| $A_{0-18}$ | Address Inputs |
| $I/O_{0-7}$ | Data Input/Output |
| $\overline{CS}$ | Chip Select |
| $\overline{OE}$ | Output Enable |
| $\overline{WE}$ | Write Enable |
| Vcc | +5.0V Power |
| Vss | Ground |

(1): Advanced information, package under development

*WHMES024*

## ABSOLUTE MAXIMUM RATINGS

| Parameter | | Unit |
|---|---|---|
| Operating Temperature | -55 to +125 | °C |
| Supply Voltage ($V_{CC}$) (1) | -2.0 to +7.0 | V |
| Signal Voltage Range(any pin except $A_9$) (2) | -2.0 to +7.0 | V |
| Storage Temperature Range | -65 to +150 | °C |
| Lead Temperature (soldering, 10 seconds) | +300 | °C |
| Data Retention | 10 years | |
| Endurance (erase/program cycles) | 10,000 | |
| $A_9$ Voltage for sector protect ($V_{ID}$) (3) | -2.0 to +14.0 | V |

**NOTES:**
1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot $V_{SS}$ to -2.0 V for periods of up to 20nS. Maximum DC voltage on output and I/O pins is $V_{CC}$ + 0.5V. During voltage transitions, outputs may overshoot to $V_{CC}$ + 2.0 V for periods of up to 20nS.
3. Minimum DC input voltage on $A_9$ pin is -0.5V. During voltage transitions, $A_9$ may overshoot $V_{SS}$ to -2V for periods of up to 20nS. Maximum Dc input voltage on $A_9$ is +13.5V which may overshoot to 14.0 V for periods up to 20nS.

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.5 | V |
| Input High Voltage | $V_{IH}$ | 2.0 | $V_{CC}$ + 0.5 | V |
| Input Low Voltage | $V_{IL}$ | -0.5 | +0.8 | V |
| Operating Temp. (Mil.) | $T_A$ | -55 | +125 | °C |
| Operating Temp. (Ind.) | $T_A$ | -40 | +85 | °C |
| $A_9$ Volatage for Sector Protect | $V_{ID}$ | 11.5 | 12.5 | V |

## CAPACITANCE

($T_A$ = +25°C)

| Parameter | Symbol | Conditions | Max | Unit |
|---|---|---|---|---|
| Address Input capacitance | $C_{AD}$ | $V_{I/O}$ = 0 V, f = 1.0 MHz | 15 | pF |
| Output Enable capacitance | $C_{OE}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 15 | pF |
| Write Enable capacitance | $C_{WE}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 15 | pF |
| Chip Select capacitance | $C_{CS}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 15 | pF |
| Data I/O capacitance | $C_{I/O}$ | $V_{I/O}$ = 0 V, f = 1.0 MHz | 15 | pF |

This parameter is guaranteed by design but not tested.

## DC CHARACTERISTICS - CMOS COMPATIBLE

($V_{CC}$ = 5.0V, $V_{SS}$ = 0V, $T_A$ = -55°C to +125°C)

| Parameter | Symbol | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | $V_{CC}$ = 5.5, $V_{IN}$ = GND to $V_{CC}$ | | 10 | µA |
| Output Leakage Current | $I_{LOx32}$ | $V_{CC}$ = 5.5, $V_{IN}$ = GND to $V_{CC}$ | | 10 | µA |
| $V_{CC}$ Active Current for Read (1) | $I_{CC1}$ | $\overline{CS}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$, f = 5mHz | | 50 | mA |
| $V_{CC}$ Active Current for Program or Erase (2) | $I_{CC2}$ | $\overline{CS}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$ | | 60 | mA |
| $V_{CC}$ Standby Current | $I_{CC4}$ | $V_{CC}$ = 5.5, $\overline{CS}$ = $V_{IH}$, f = 5MHz | | 1.6 | mA |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 12.0 mA, $V_{CC}$ = 4.5 | | 0.45 | V |
| Output High Voltage | $V_{OH1}$ | $I_{OH}$ = -2.5 mA, $V_{CC}$ = 4.5 | 0.85 x $V_{CC}$ | | V |
| Low $V_{CC}$ Lock-Out Voltage | $V_{LKO}$ | | 3.2 | 4.2 | V |

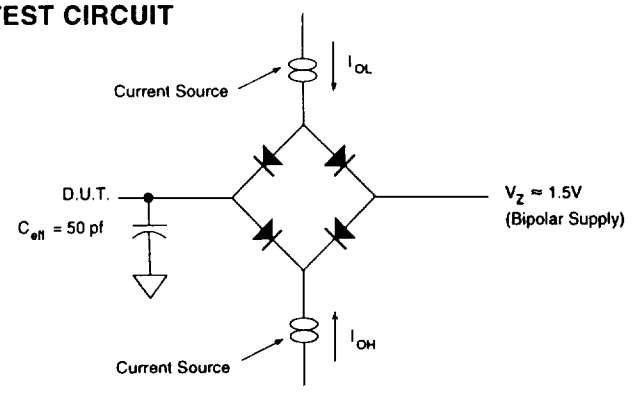
**NOTES:**
1. The Icc current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at $V_{IH}$.
2. Icc active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: $V_{IL}$ = 0.3V, $V_{IH}$ = $V_{CC}$ - 0.3V

## AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED

(VCC = 5.0V, VSS = 0V, TA = -55°C to +125°C)

| Parameter | Symbol | | -70 | | -90 | | -120 | | -150 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | | | |
| Write Cycle Time | tAVAV | tWC | 70 | | 90 | | 120 | | 150 | | nS |
| Write Enable Setup Time | tWLEL | tWS | 0 | | 0 | | 0 | | 0 | | nS |
| Chip Select Pulse Width | tELEH | tCP | 45 | | 45 | | 50 | | 50 | | nS |
| Address Setup Time | tAVEL | tAS | 0 | | 0 | | 0 | | 0 | | nS |
| Data Setup Time | tDVEH | tDS | 45 | | 45 | | 50 | | 50 | | nS |
| Data Hold Time | tEHDX | tDH | 0 | | 0 | | 0 | | 0 | | nS |
| Address Hold Time | tELAX | tAH | 45 | | 45 | | 50 | | 50 | | nS |
| Chip Select Pulse Width High | tEHEL | tCPH | 20 | | 20 | | 20 | | 20 | | nS |
| Duration of Byte Programming Operation | tWHWH1 | | 16 | | 16 | | 16 | | 16 | | µS |
| Chip and Sector Erase Time | tWHWH2 | | | 30 | | 30 | | 30 | | 30 | Sec |
| Read Recovery Time | tGHEL | | 0 | | 0 | | 0 | | 0 | | µS |
| Chip Programming Time | | | | 50 | | 50 | | 50 | | 50 | Sec |
| Chip Erase Time | tWHWH2 | | | 120 | | 120 | | 120 | | 120 | Sec |

### AC TEST CIRCUIT




### AC TEST CONDITIONS

| Parameter | Typ | Unit |
|---|---|---|
| Input Pulse Levels | VIL = 0, VIH = 3.0 | V |
| Input Rise and Fall | 5 | nS |
| Input and Output Reference Level | 1.5 | V |
| Output Timing Reference Level | 1.5 | V |

**NOTES:**
VZ is programmable from -2V to +7V.
IOL & IOH programmable from 0 to 16mA.
Tester Impedance ZO = 75 Ω.
VZ is typically the midpoint of VOH and VOL.
IOL & IOH are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

## AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{WE}$ CONTROLLED

($V_{CC}$ = 5.0V, $T_A$ = -55°C to +125°C)

| Parameter | Symbol | | -70 | | -90 | | -120 | | -150 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | $t_{AVAV}$ | $t_{WC}$ | 70 | | 90 | | 120 | | 150 | | nS |
| Chip Select Setup Time | $t_{ELWL}$ | $t_{CS}$ | 0 | | 0 | | 0 | | 0 | | nS |
| Write Enable Pulse Width | $t_{WLWH}$ | $t_{WP}$ | 45 | | 45 | | 50 | | 50 | | nS |
| Address Setup Time | $t_{AVWH}$ | $t_{AS}$ | 0 | | 0 | | 0 | | 0 | | nS |
| Data Setup Time | $t_{DVWH}$ | $t_{DS}$ | 45 | | 45 | | 50 | | 50 | | nS |
| Data Hold Time | $t_{WHDX}$ | $t_{DH}$ | 0 | | 0 | | 0 | | 0 | | nS |
| Address Hold Time | $t_{WHAX}$ | $t_{AH}$ | 45 | | 45 | | 50 | | 50 | | nS |
| Write Enable Pulse Width High | $t_{WHWL}$ | $t_{WPH}$ | 20 | | 20 | | 20 | | 20 | | nS |
| Duration of Byte Programming Operation | $t_{WHWH1}$ | | 16 | | 16 | | 16 | | 16 | | µS |
| Sector Erase Time | $t_{WHWH2}$ | | | 30 | | 30 | | 30 | | 30 | Sec |
| Read Recovery Time before Write | $t_{GHWL}$ | | 0 | | 0 | | 0 | | 0 | | µS |
| Vcc Set-up Time | $t_{VCS}$ | | 50 | | 50 | | 50 | | 50 | | µs |
| Chip Programming Time | | | | 50 | | 50 | | 50 | | 50 | Sec |
| Output Enable Setup Time | | $t_{OES}$ | 0 | | 0 | | 0 | | 0 | | nS |
| Output Enable Hold Time (1) | | $t_{OEH}$ | 10 | | 10 | | 10 | | 10 | | nS |
| Chip Erase Time | $t_{WHWH2}$ | | | 120 | | 120 | | 120 | | 120 | Sec |

1. For Toggle and Data Polling.

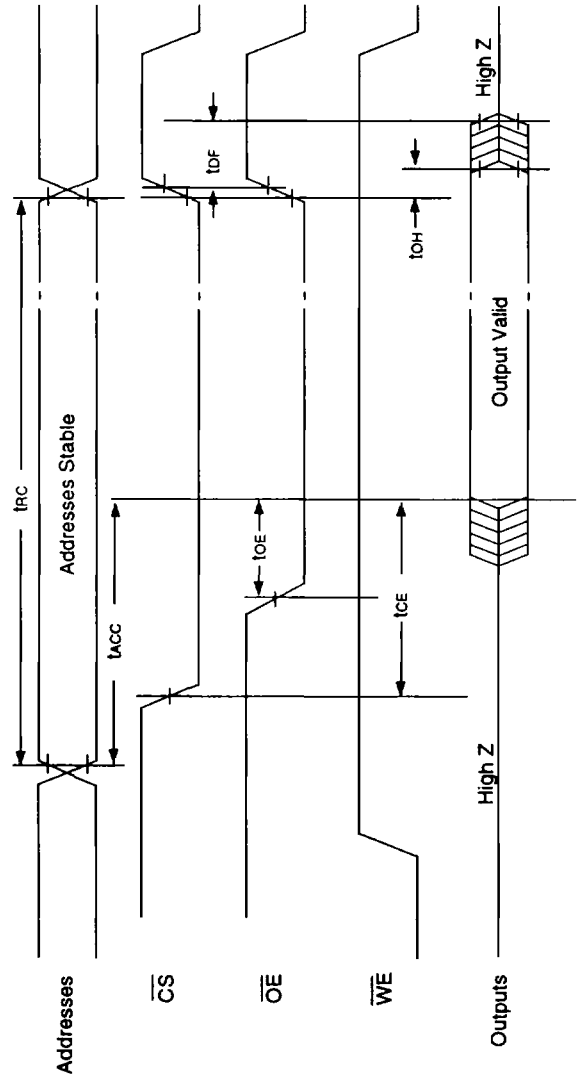
## AC CHARACTERISTICS – READ ONLY OPERATIONS

($V_{CC}$ = 5.0V, $T_A$ = -55°C to +125°C)

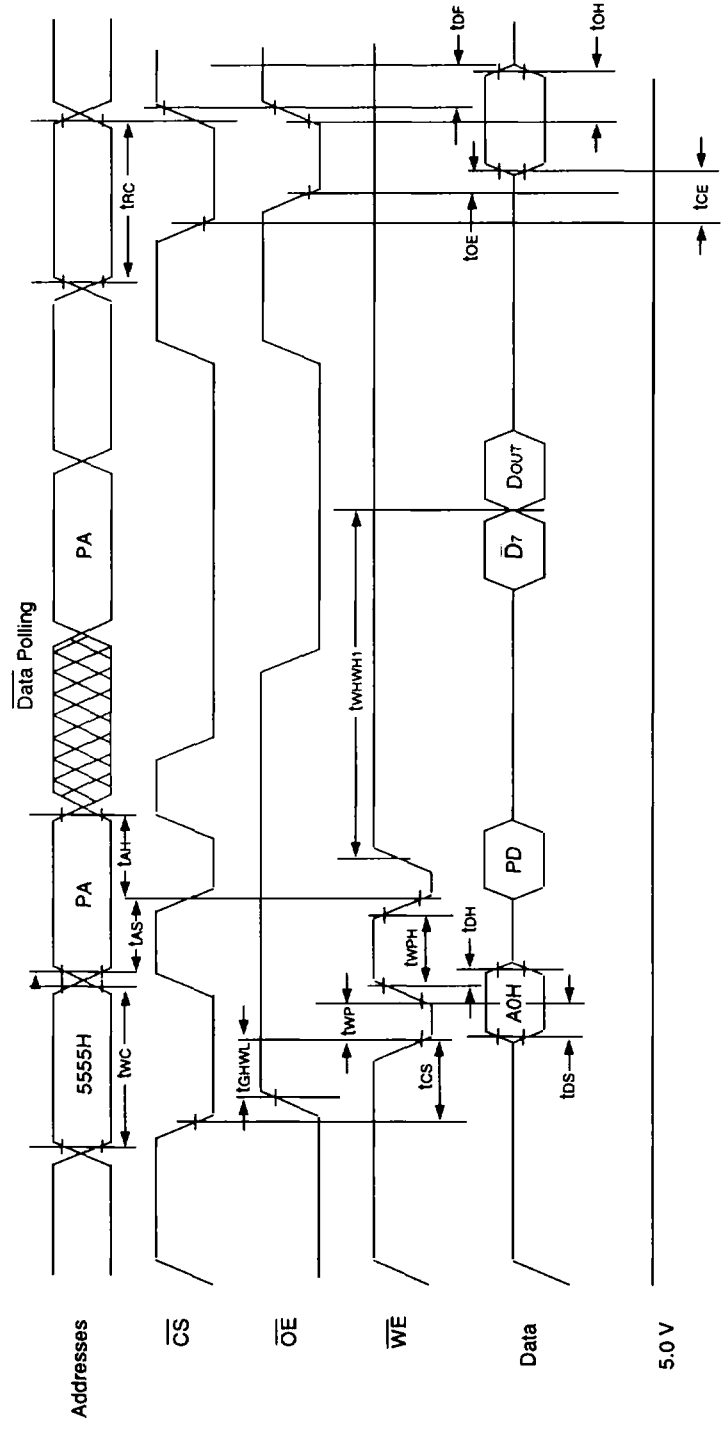
| Parameter | Symbol | | -70 | | -90 | | -120 | | -150 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | $t_{AVAV}$ | $t_{RC}$ | 70 | | 90 | | 120 | | 150 | | nS |
| Address Access Time | $t_{AVQV}$ | $t_{ACC}$ | | 70 | | 90 | | 120 | | 150 | nS |
| Chip Select Access Time | $t_{ELQV}$ | $t_{CE}$ | | 70 | | 90 | | 120 | | 150 | nS |
| Output Enable to Output Valid | $t_{GLQV}$ | $t_{OE}$ | | 35 | | 35 | | 50 | | 55 | nS |
| Chip Select to Output High Z (1) | $t_{EHQZ}$ | $t_{DF}$ | | 20 | | 20 | | 30 | | 35 | nS |
| Output Enable High to Output High Z (1) | $t_{GHQZ}$ | $t_{DF}$ | | 20 | | 20 | | 30 | | 35 | nS |
| Output Hold from Address, $\overline{CS}$ or $\overline{OE}$ Change, whichever is First | $t_{AXQX}$ | $t_{OH}$ | 0 | | 0 | | 0 | | 0 | | nS |

1. Guaranteed by design, but not tested

## AC WAVEFORMS FOR READ OPERATIONS

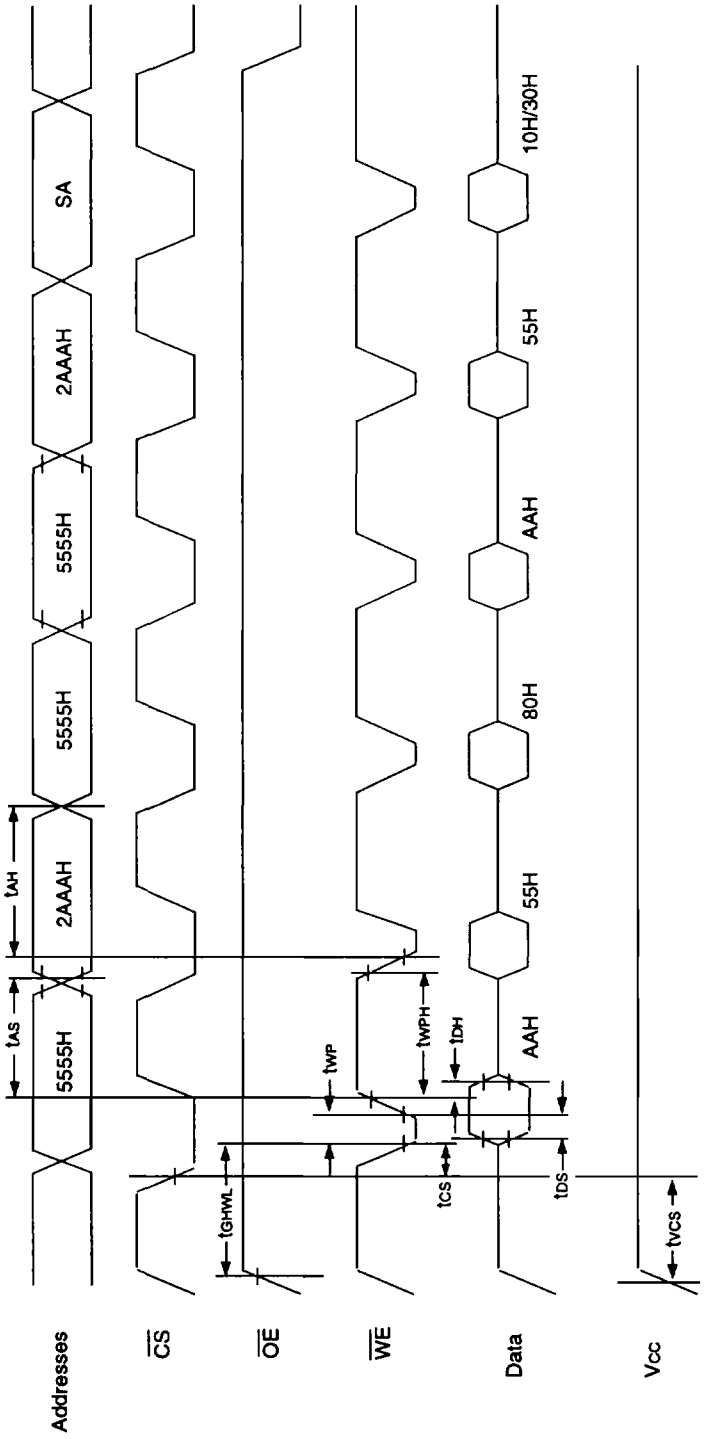


## WRITE/ERASE/PROGRAM OPERATION, $\overline{WE}$ CONTROLLED



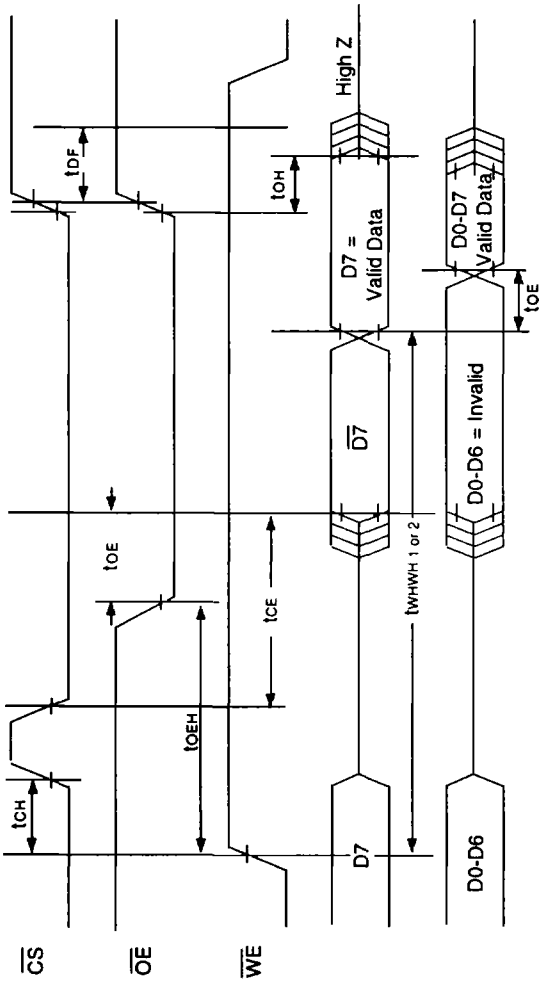

**NOTES:**
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

## AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS

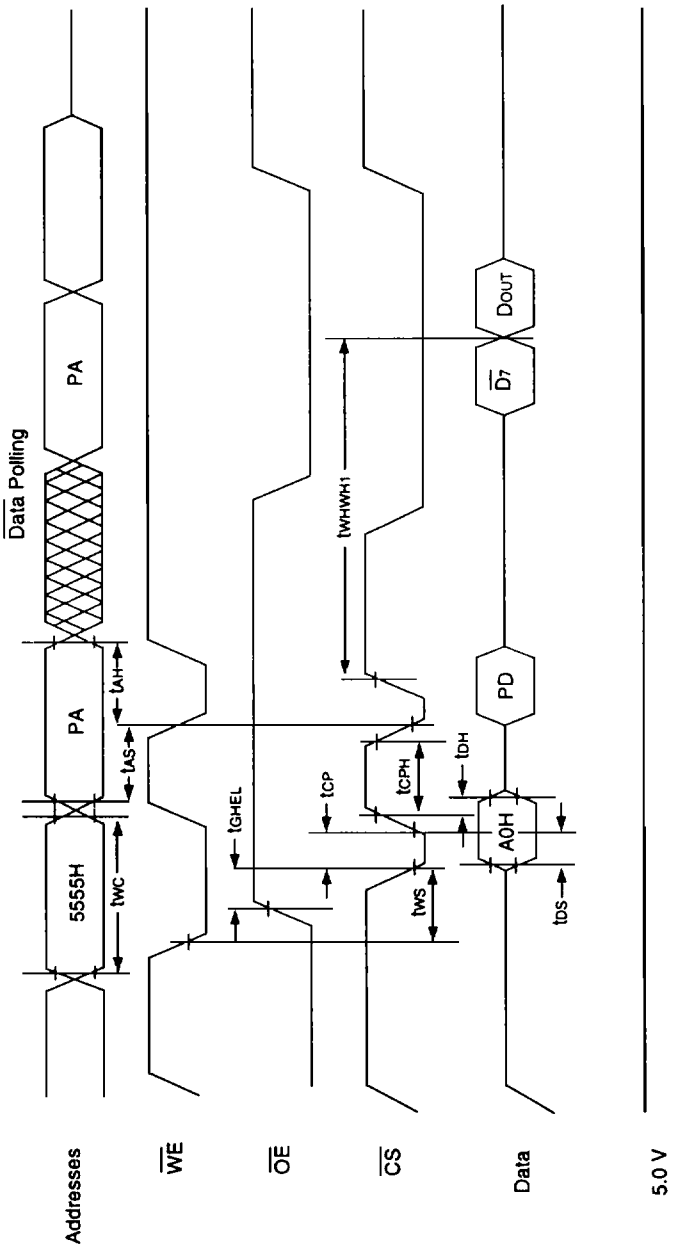



**NOTE:**
1. SA is the sector address for Sector Erase.

## AC WAVEFORMS FOR $\overline{\text{DATA}}$ POLLING DURING EMBEDDED ALGORITHM OPERATIONS



## ALTERNATE $\overline{CS}$ CONTROLLED PROGRAMMING OPERATION TIMINGS




**NOTES:**

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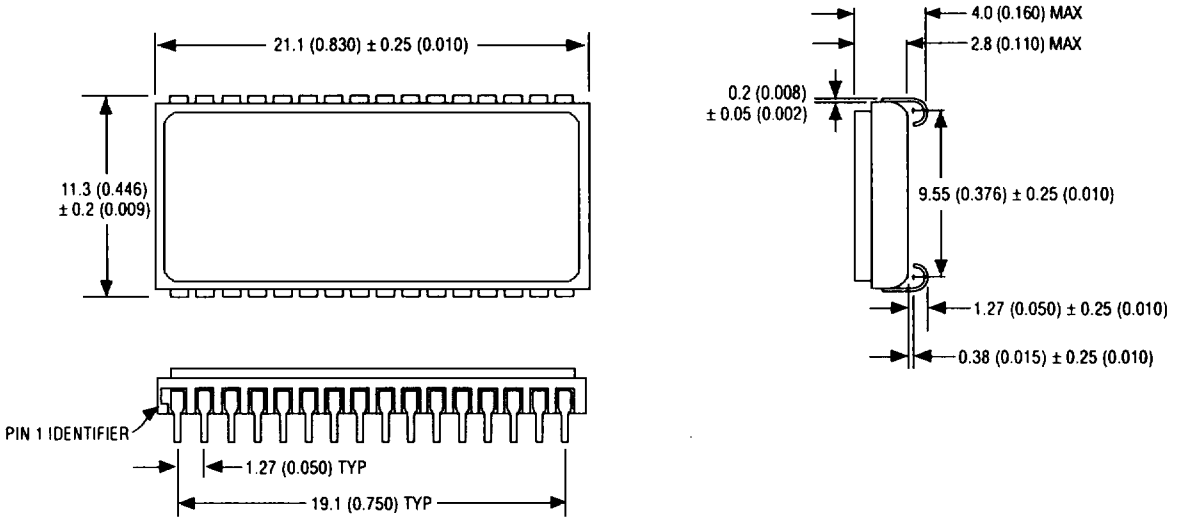
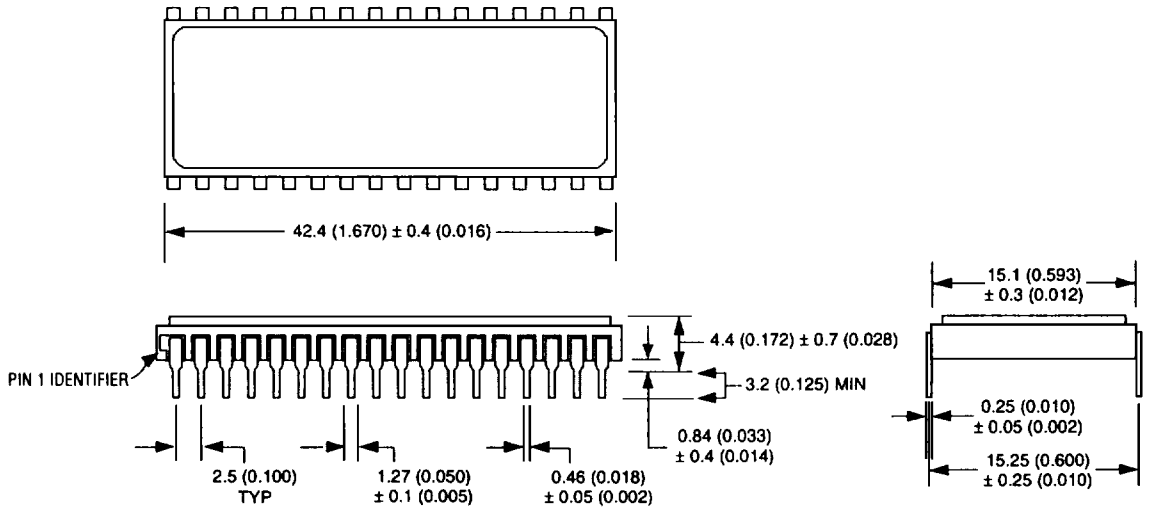
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

## PACKAGE 101: 32 LEAD, CERAMIC SOJ



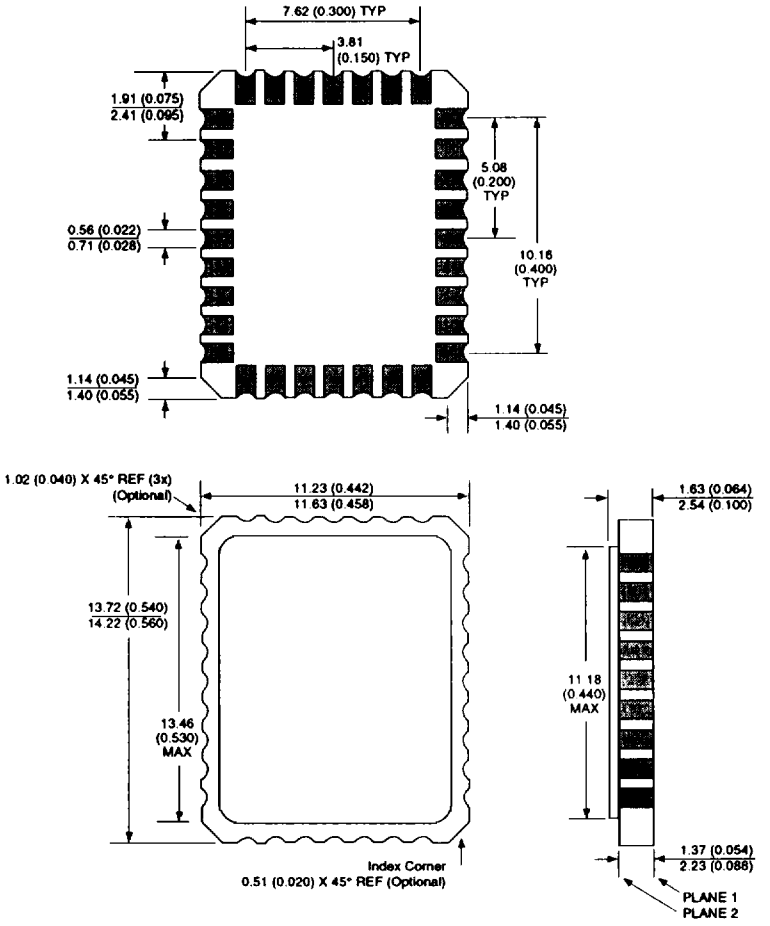

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

## PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



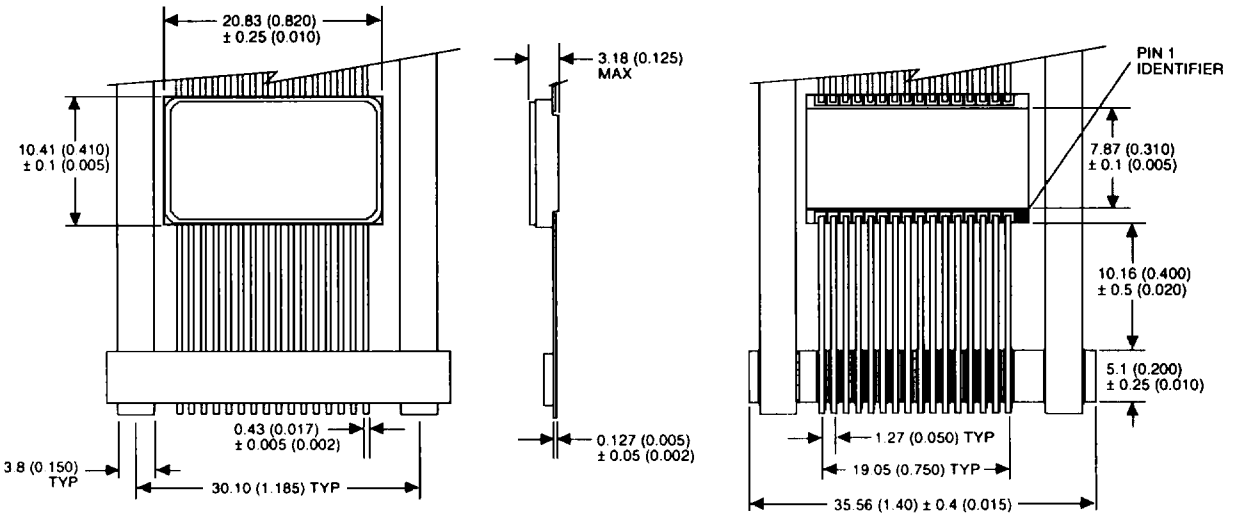

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

## PACKAGE 601: 32 PIN, RECTANGULAR CERAMIC LEADLESS CHIP CARRIER



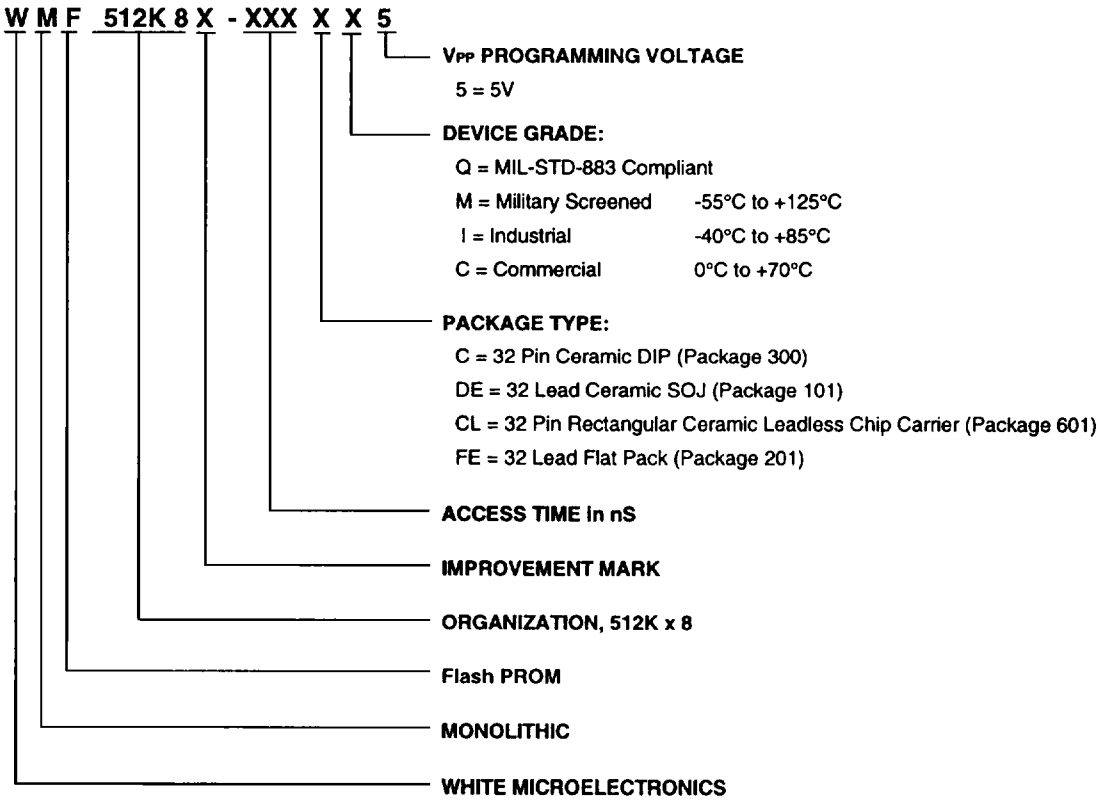

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

## PACKAGE 201: 32 LEAD, CERAMIC FLAT PACK




ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

## ORDERING INFORMATION




| DEVICE TYPE | SPEED | PACKAGE | SMD NO. |
|---|---|---|---|
| 512K x 8 SRAM Monolithic | 150nS | 32 pin DIP | 5962-96692 01HXX |
| 512K x 8 SRAM Monolithic | 120nS | 32 pin DIP | 5962-96692 02HXX |
| 512K x 8 SRAM Monolithic | 90nS | 32 pin DIP | 5962-96692 03HXX |
| 512K x 8 SRAM Monolithic | 70nS | 32 pin DIP | 5962-96692 04HXX |
| 512K x 8 SRAM Monolithic | 150nS | 32 pin CSOJ | 5962-96692 01HYX |
| 512K x 8 SRAM Monolithic | 120nS | 32 pin CSOJ | 5962-96692 02HYX |
| 512K x 8 SRAM Monolithic | 90nS | 32 pin CSOJ | 5962-96692 03HYX |
| 512K x 8 SRAM Monolithic | 70nS | 32 pin CSOJ | 5962-96692 04HYX |