



ICS8302I-01

LOW SKEW, 1-TO-2 LVCMOS / LVTTTL FANOUT BUFFER W/ COMPLEMENTARY OUTPUT

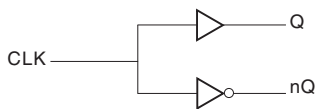
GENERAL DESCRIPTION

The ICS8302I-01 is a low skew, 1-to-2 LVCMOS/LVTTTL Fanout Buffer w/Complementary Output. The ICS8302I-01 has a single ended clock input. The single ended clock input accepts LVCMOS or LVTTTL input levels. The ICS8302I-01 is characterized at full 3.3V for input V_{DD} , and mixed 3.3V and 2.5V for output operating supply modes (V_{DDO}). Guaranteed output and part-to-part skew characteristics make the ICS8302I-01 ideal for clock distribution applications demanding well defined performance and repeatability.

FEATURES

- Complementary LVCMOS / LVTTTL output
- LVCMOS / LVTTTL clock input accepts LVCMOS or LVTTTL input levels
- Maximum output frequency: 250MHz
- Output skew: 165ps (maximum)
- Part-to-part skew: 800ps (maximum)
- Small 8 lead SOIC package saves board space
- Full 3.3V or 3.3V core/2.5V output supply modes
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free compliant packages

BLOCK DIAGRAM



PIN ASSIGNMENT

| | | | |
|-----------|---|---|-----------|
| V_{DDO} | 1 | 8 | Q |
| V_{DD} | 2 | 7 | GND |
| CLK | 3 | 6 | V_{DDO} |
| GND | 4 | 5 | nQ |

ICS8302I-01 8-Lead SOIC

3.8mm x 4.8mm, x 1.47mm package body

M Package
Top View



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TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|--------|------------------|--------|----------|---|
| 1, 6 | V _{DDO} | Power | | Output supply pins. |
| 2 | V _{DD} | Power | | Power supply pin. |
| 3 | CLK | Input | Pulldown | LVCMOS / LVTTTL clock input. |
| 4,7 | GND | Power | | Power supply ground. |
| 5 | nQ | Output | | Complementary clock output. LVCMOS / LVTTTL interface levels. |
| 8 | Q | Output | | Clock output. LVCMOS / LVTTTL interface levels. |

NOTE: *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|--|---|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| C _{PD} | Power Dissipation Capacitance (per output) | V _{DD} , V _{DDO} = 3.465V | | 22 | | pF |
| | | V _{DD} = 3.465V, V _{DDO} = 2.625V | | 16 | | pF |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |
| R _{OUT} | Output Impedance | | 5 | 7 | 12 | Ω |



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ABSOLUTE MAXIMUM RATINGS

| | |
|--|---------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_i | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, V_o | -0.5V to $V_{DDO} + 0.5V$ |
| Package Thermal Impedance, θ_{JA} | 112.7°C/W (0 lfpm) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------------|-----------------|---------|---------|---------|-------|
| V_{DD} | Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDO} | Output Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| | | | 2.375 | 2.5 | 2.625 | V |
| I_{DD} | Power Supply Current | | | | 13 | mA |
| I_{DDO} | Output Supply Current | | | | 4 | mA |

TABLE 3B. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|---------------------|--|---------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | 2 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | CLK $V_{DD} = V_{IN} = 3.465V$ | | | 150 | μA |
| I_{IL} | Input Low Current | CLK $V_{DD} = 3.465V, V_{IN} = 0V$ | -5 | | | μA |
| V_{OH} | Output High Voltage | $V_{DDO} = 3.465, 50\Omega$ to $V_{DDO}/2$ | 2.6 | | | V |
| | | $V_{DDO} = 3.465, I_{OH} = -100\mu A$ | 2.9 | | | V |
| | | $V_{DDO} = 2.625, 50\Omega$ to $V_{DDO}/2$ | 1.8 | | | V |
| | | $V_{DDO} = 2.625, I_{OH} = -100\mu A$ | 2.2 | | | V |
| V_{OL} | Output Low Voltage | $V_{DDO} = 3.465, 50\Omega$ to $V_{DDO}/2$ | | | 0.5 | V |
| | | $V_{DDO} = 3.465, I_{OL} = 100\mu A$ | | | 0.2 | V |
| | | $V_{DDO} = 2.625, 50\Omega$ to $V_{DDO}/2$ | | | 0.5 | V |
| | | $V_{DDO} = 2.625, I_{OL} = 100\mu A$ | | | 0.2 | V |



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TABLE 4A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|--|--------------------------|---------|---------|---------|-------|
| f_{MAX} | Output Frequency | | | | 250 | MHz |
| tp_{LH} | Propagation Delay, Low-to-High; NOTE 1 | | 1.8 | | 2.7 | ns |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 4 | | | | 165 | ps |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 3, 4 | | | | 800 | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 300 | | 800 | ps |
| odc | Output Duty Cycle | $f \leq 133MHz$ | 45 | | 55 | % |
| | | $133MHz < f \leq 250MHz$ | 40 | | 60 | % |

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 4B. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|--|--------------------------|---------|---------|---------|-------|
| f_{MAX} | Output Frequency | | | | 250 | MHz |
| tp_{LH} | Propagation Delay, Low-to-High; NOTE 1 | | 1.9 | | 2.9 | ns |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 4 | | | | 250 | ps |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 3, 4 | | | | 900 | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 100 | | 850 | ps |
| odc | Output Duty Cycle | $f \leq 133MHz$ | 45 | | 55 | % |
| | | $133MHz < f \leq 250MHz$ | 40 | | 60 | % |

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

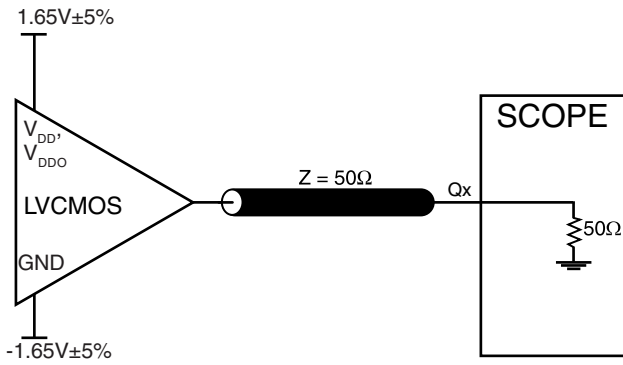
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

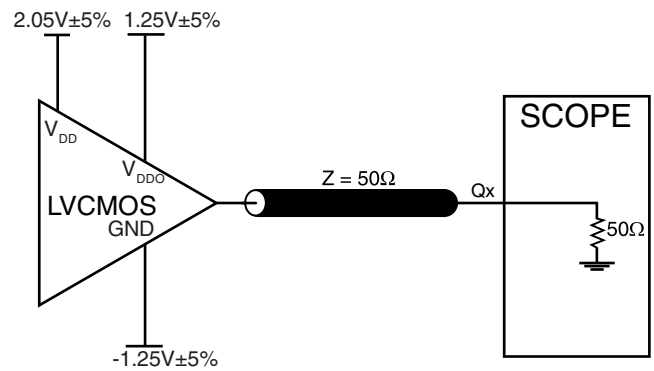
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



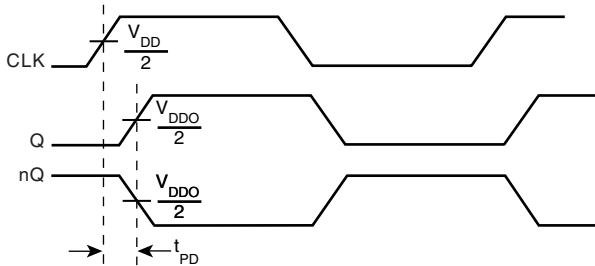
PARAMETER MEASUREMENT INFORMATION



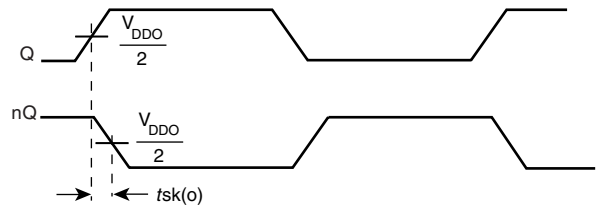
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



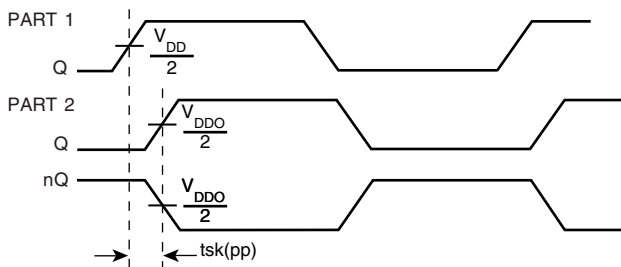
3.3V/2.5V OUTPUT LOAD AC TEST CIRCUIT



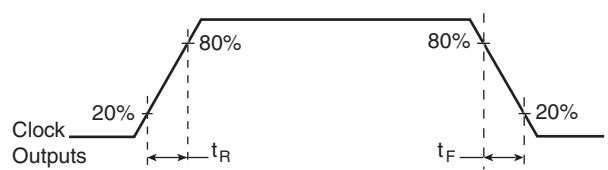
PROPAGATION DELAY



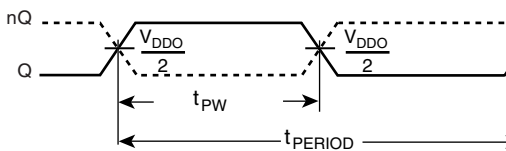
OUTPUT SKEW



PART-TO-PART SKEW



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



RELIABILITY INFORMATION

TABLE 5. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD SOIC

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|-----------|-----------|-----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 153.3°C/W | 128.5°C/W | 115.5°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 112.7°C/W | 103.3°C/W | 97.1°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8302I-01 is: 322

PACKAGE OUTLINE - SUFFIX M FOR 8 LEAD SOIC

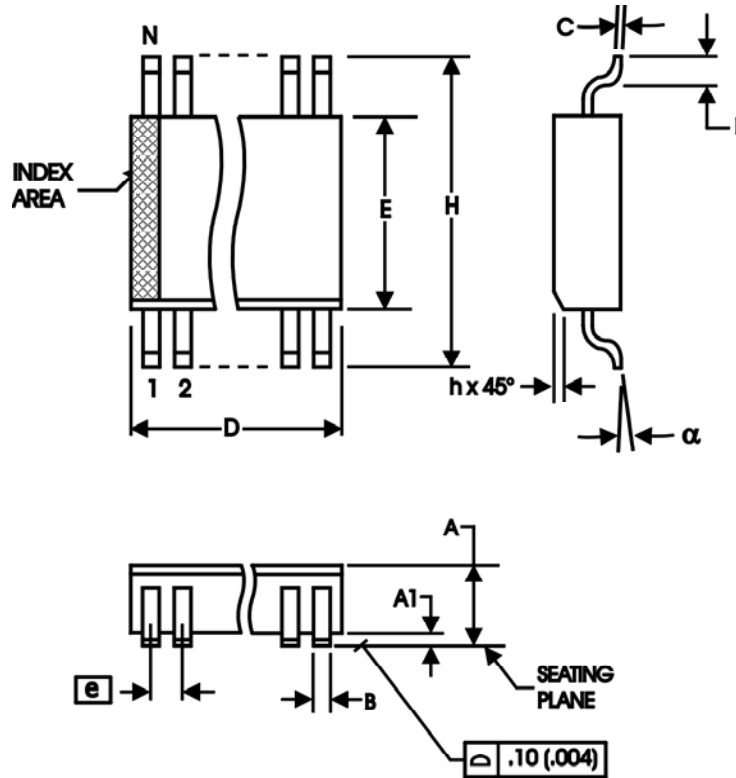


TABLE 6. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|----------|-------------|---------|
| | MINIMUM | MAXIMUM |
| N | 8 | |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| B | 0.33 | 0.51 |
| C | 0.19 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BASIC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.27 |
| α | 0° | 8° |

Reference Document: JEDEC Publication 95, MS-012



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TABLE 7. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|----------|-------------------------|--------------------|---------------|
| 8302AMI-01 | 302AI01 | 8 lead SOIC | tube | -40°C to 85°C |
| 8302AMI-01T | 302AI01 | 8 lead SOIC | 2500 tape & reel | -40°C to 85°C |
| 8302AMI-01LF | 302AI01L | 8 lead "Lead-Free" SOIC | tube | -40°C to 85°C |
| 8302AMI-01LFT | 302AI01L | 8 lead "Lead-Free" SOIC | 2500 tape & reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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| REVISION HISTORY SHEET | | | | |
|------------------------|-------|---------|--|---------|
| Rev | Table | Page | Description of Change | Date |
| A | T7 | 8 10 | Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page. | 7/29/10 |
| | | | | |
| | | | | |



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