CY2260

Clock Synthesizer/Driver for Pentium™ and Pentium Pro™ Processors

Features

- **Multiple clock outputs to meet requirements of most motherboards using Pentium™, Pentium Pro™, or Cyrix™ processors**
  - **— Four CPU clocks (CPUCLK) @ 66.66 MHz, 60.0 MHz, or 50.0 MHz, pin selectable (plus 55.0 MHz on –2, –3, and –3H options)**
  - **— Six PCI clocks (PCICLK) @ (CPUCLK/2) MHz**
  - **— One USB clock @ 48.0 MHz**
  - **— Three Ref. clocks @ 14.318 MHz (Two on –2, –3, and –3H options)**
  - **— I/O clock @ 24MHz (–2, –3, and –3H options only)**
  - **— Ref. 14.318 MHz Xtal oscillator input**
- **CPU clock jitter ≤ 200 ps cycle-to-cycle**
- **Low skew outputs**
  - **— ≤ 250 ps between CPU clocks**
  - **— ≤ 250 ps between PCI clocks (PCICLK)**
  - **— +1 ns min. to +4 ns max. skew between CPU and PCI clocks (CPU leads PCI)**
- **Output duty cycle 45% min. to 55% max.**
- **Available in 28-pin SOIC and SSOP packages**
- **Test mode support (–1 option)**
- **3.3V or 5V operation**
- **Internal pull-up resistors on S0, S1, and OE inputs**

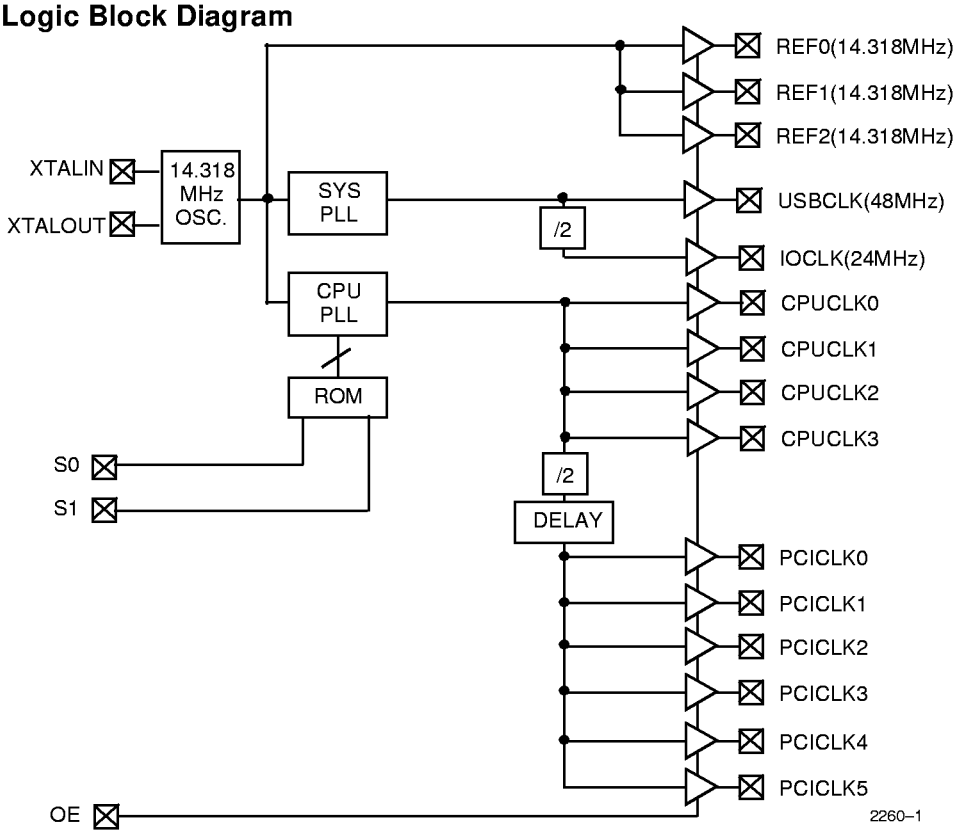
Functional Description

The CY2260 is a Clock Synthesizer/Driver chip for an Intel® Pentium or Pentium Pro processor based PC. The part outputs multiple clocks to serve the requirements of most motherboards. The CY2260 has low-skew outputs (≤ 250 ps between the CPU Clocks, ≤ 250 ps between the PCI Clocks). In addition, the CY2260 CPU clock outputs have less than 200 ps cycle-to-cycle jitter. Finally, both the PCI and CPU clock outputs meet the 1V/ns slew rate requirement of the Pentium- and Pentium Pro-based processor system.

The CY2260 accepts a 14.318 MHz reference signal as its input. The CY2260 has two PLLs, one of which generates the CPU and PCI clocks, and the other generates the Universal Serial Bus (USB) and I/O clocks. The CY2260 runs off a 3.3V or 5V supply.

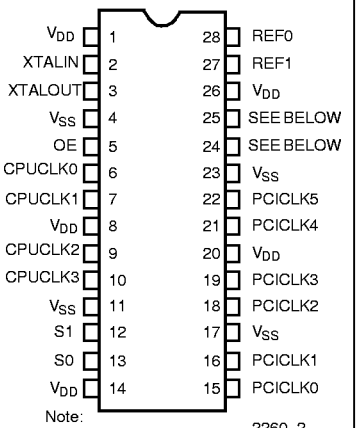
The CY2260 is available in five options. The –1 and –1H options provide three buffered reference clocks. The –2 and –3 options provide two buffered reference clocks and a 24 MHz I/O clock. The –2 and –3 options also support Cyrix processors. Finally, the –3H configuration is the same as the –3, except that it has high drive USB and I/O clocks to drive multiple outputs.

Logic Block Diagram



Pin Configuration

Top View
SOIC/SSOP



Note:
CPUCLK = CPU Clock
PCICLK = PCI Bus Clock

OPTION	PIN 24	PIN 25
–1 –1H	USBCLK 48 MHz	REF2 14.318 MHz
–2	USBCLK 48 MHz	IOCLK 24 MHz
–3 –3H	IOCLK 24 MHz	USBCLK 48 MHz

Pin Summary

Name	–1	–2	–3, -3H	Description
V_{DD}	1	1	1	Voltage supply
XTALIN[1]	2	2	2	Reference crystal input
XTALOUT[1]	3	3	3	Reference crystal feedback
V_{SS}	4	4	4	Ground
OE	5	5	5	Output Enable, Active HIGH (internal pull-up resistor to V_{DD})
CPUCLK0	6	6	6	CPU clock output
CPUCLK1	7	7	7	CPU clock output
V_{DD}	8	8	8	Voltage supply
CPUCLK2	9	9	9	CPU clock output
CPUCLK3	10	10	10	CPU clock output
V_{SS}	11	11	11	Ground
S1	12	12	12	CPU clock select input, bit 1 (internal pull-up resistor to V_{DD})
S0	13	13	13	CPU clock select input, bit 0 (internal pull-up resistor to V_{DD})
V_{DD}	14	14	14	Voltage supply
PCICLK0	15	15	15	PCI clock output
PCICLK1	16	16	16	PCI clock output
V_{SS}	17	17	17	Ground
PCICLK2	18	18	18	PCI clock output
PCICLK3	19	19	19	PCI clock output
V_{DD}	20	20	20	Voltage supply
PCICLK4	21	21	21	PCI clock output
PCICLK5	22	22	22	PCI clock output
V_{SS}	23	23	23	Ground
USBCLK	24	24	25	Universal Serial Bus clock output (48 MHz)
REF2	25			Reference clock output (14.318 MHz)
IOCLK		25	24	I/O clock output (24 MHz)
V_{DD}	26	26	26	Voltage supply
REF1	27	27	27	Reference clock output (14.318 MHz)
REF0	28	28	28	Reference clock output (14.318 MHz) for ISA slots, drives 45 pF loads

Function Table

Option	OE	S0	S1	XTALIN Input	CPUCLK	PCICLK	REF0, REF1, REF2	USBCLK	IOCLK –2,–3,–3H only
–1,–1H,–2,–3,–3H	0	X	X	14.318 MHz	High-Z	High-Z	High-Z	High-Z	High-Z
–1,–1H,–2,–3,–3H	1	0	0	14.318 MHz	50.0 MHz	25.0 MHz	14.318 MHz	48 MHz	24 MHz
–1,–1H,–2,–3,–3H	1	0	1	14.318 MHz	60.0 MHz	30.0 MHz	14.318 MHz	48 MHz	24 MHz
–1,–2,–3,–3H	1	1	0	14.318 MHz	66.66 MHz	33.33 MHz	14.318 MHz	48 MHz	24 MHz
–1,–1H	1	1	1	TCLK[2]	TCLK/2	TCLK/4	TCLK	TCLK/2	
–2,–3,–3H	1	1	1	14.318 MHz	55 MHz	27.5 MHz	14.318 MHz	48 MHz	24 MHz

Notes:

1. For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 18 pF.
2. TCLK is a test clock on the XTALIN input during test mode.

Actual Frequency Values

Clock	Target	Actual	PPM
CPUCLK	50	49.802	–3960
CPUCLK	60	60.0	0
CPUCLK	66.667	66.316	–5265
CPUCLK	55.0	54.98	–331
USBCLK (H version)	48.0	48.008	167
USBCLK (non-H)	48.0	48.109	2271
IOCLK (H version)	24.0	24.004	167
IOCLK (non-H)	24.0	24.055	2271

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... –0.5 to +7.0V

Input Voltage ..... –0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing) ... –65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C

Junction Temperature ..... +150°C

Package Power Dissipation 1W

Static Discharge Voltage ..... >2000V (per MIL–STD–883, Method 3015)

Operating Conditions[3]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage, 3.3V (5V)	3.135 (4.5)	3.6 (5.5)	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Capacitive Load on CPUCLK / PCICLK (–1, –1H option) CPUCLK / PCICLK (–2,–3, 3H options) USBCLK / IOCLK REF0 REF1 REF2		 30 20 20 45 30 25	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Electrical Characteristics V_{DD} = 3.135V to 3.6V, or 4.5V to 5.5V, T_A = 0°C to +70°C

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}[4]	High-level Input Voltage	Except Crystal Inputs			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs				0.8	V
V_{OH}	High-level Output Voltage CPUCLK / PCICLK	V_{DD} = V_{DD} Min.	I_{OH} = –23 mA	–1, –1H options	2.4		V
V_{OH}	High-level Output Voltage CPUCLK / PCICLK	V_{DD} = V_{DD} Min.	I_{OH} = –15 mA	–2,–3,–3H options			V
V_{OH}	USBCLK	V_{DD} = V_{DD} Min.	I_{OH} = –4 mA	–1,–2,–3 options			V
V_{OH}	USBCLK, IOCLK	V_{DD} = V_{DD} Min.	I_{OH} = –15 mA	–1H,–3H options			V
V_{OH}	IOCLK	V_{DD} = V_{DD} Min.	I_{OH} = –4 mA	–2,–3 options			V
V_{OH}	REF0	V_{DD} = V_{DD} Min.	I_{OH} = –15 mA	All options			V
V_{OH}	REF1	V_{DD} = V_{DD} Min.	I_{OH} = –11 mA	All options			V
V_{OH}	REF2	V_{DD} = V_{DD} Min.	I_{OH} = –8 mA	–1 option			V
V_{OL}	Low-level Output Voltage CPUCLK / PCICLK	V_{DD} = V_{DD} Min.	I_{OL} = 16 mA	–1 option		0.4	V
V_{OL}	Low-level Output Voltage CPUCLK / PCICLK	V_{DD} = V_{DD} Min.	I_{OL} = 12 mA	–2, –3,–3H options			V
V_{OL}	USBCLK	V_{DD} = V_{DD} Min.	I_{OL} = 4 mA	–1,–2,–3 options			V
V_{OL}	USBCLK	V_{DD} = V_{DD} Min.	I_{OL} = 15 mA	–1H,–3H options			V
V_{OL}	IOCLK	V_{DD} = V_{DD} Min.	I_{OL} = 4 mA	–2,–3 options			V
V_{OL}	REF0	V_{DD} = V_{DD} Min.	I_{OL} = 12 mA	All options			V
V_{OL}	REF1	V_{DD} = V_{DD} Min.	I_{OL} = 8 mA	All options			V
V_{OL}	REF2	V_{DD} = V_{DD} Min.	I_{OL} = 6 mA	–1,–1H options			V
I_{IH}	Input High Current	V_{IH} = V_{DD} = 3.3V (5V)				5 (10)	µA
I_{IL}	Input Low Current	V_{IL} = 0V, V_{DD} = 3.3V (5V)				100 (250)	µA
I_{OZ}	Output Leakage Current	Three-state			–10	+10	µA
I_{DD}	Power Supply Current	V_{DD} = 3.6V, V_{IN} = 0 or V_{DD} V_{DD} = 5.5V, V_{IN} = 0 or V_{DD}				90 150	mA mA

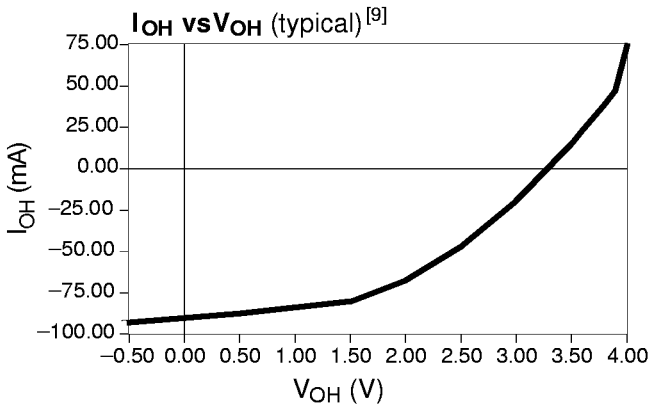
Notes:

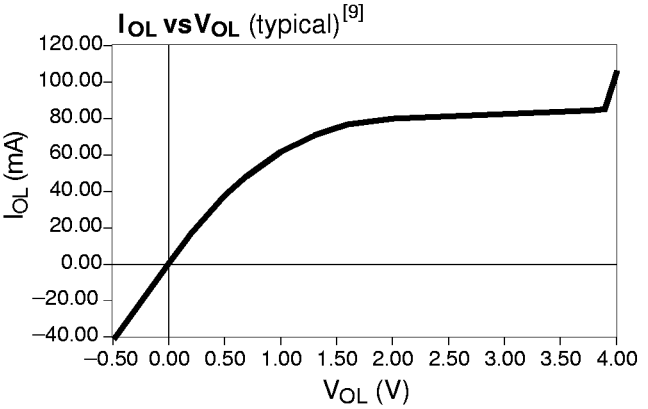
3. Electrical parameters are guaranteed with these operating conditions.
4. V_{IH} = 3.0V when V_{DD} = 5V.

Switching Characteristics[5]

Parameter	Output	Description	Test Conditions	Min.	Max.	Unit
t_1	All	Output Duty Cycle[6, 7]	$t_1 = t_{1A} \div t_{1B}$	45%	55%	
t_{1C}	CPUCLK	CPU Clock HIGH Time	Measured at 2.4V	5.0		ns
t_{1C}	PCICLK	PCI Clock HIGH Time[8]	Measured at 2.4V	12.0		ns
t_{1D}	CPUCLK	CPU Clock LOW Time	Measured at 0.4V	5.0		ns
t_{1D}	PCICLK	PCI Clock LOW Time[8]	Measured at 0.4V	12.0		ns
t_2	CPUCLK	CPU Clock Rising and Falling Edge Rate	Measured between 0.4V and 2.4V	1	4.0	V/ns
t_3	CPUCLK	CPU Clock Rise Time	Measured between 0.4V and 2.4V	0.5	2.0	ns
t_4	CPUCLK	CPU Clock Fall Time	Measured between 2.4V and 0.4V	0.5	2.0	ns
t_2	PCICLK	PCI Clock Rising and Falling Edge Rate	Measured between 0.4V and 2.4V	1	4	V/ns
t_2	REF[0:2]	Reference Clock Rising and Falling Edge Rate	Measured between 0.4V and 2.4V	0.5		V/ns
t_2	USBCLK, IOCLK	USB and I/O Clock Rising and Falling Edge Rate	Measured between 0.4V and 2.4V	0.5		V/ns
t_2	USBCLK, IOCLK (–3H,–1H Options)	USB and I/O Clock Rising and Falling Edge Rate	Measured between 0.4V and 2.4V	1.0		V/ns
t_5	CPUCLK	CPU-CPU Clock Skew	Measured at 1.5V		250	ps
t_6	PCICLK	PCI-PCI Clock Skew	Measured at 1.5V		250	ps
t_7	CPUCLK PCICLK	CPU-PCI Clock Skew (CPU leads)	Measured at 1.5V	1	4	ns
t_8	CPUCLK	Cycle-Cycle Clock Jitter	CPU Clock jitter		200	ps
t_9	CPUCLK	Pk-Pk Period Clock Jitter	Measured at 1.5V		250	ps
t_{10}	PCICLK	Pk-Pk Period Clock Jitter	Measured at 1.5V		250	ps
t_{11}	CPUCLK	Power-up Time	CPU clock stabilization from power-up		3	ms
t_{12}	PCICLK	Power-up Time	PCI clock stabilization from power-up		3	ms

Output I-V Characteristics at 3.3V



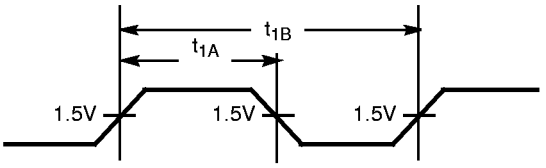


Notes:

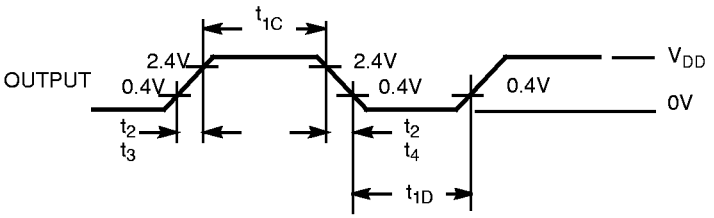
5. All parameters specified with outputs fully loaded.
6. Duty cycle is measured at 1.5V for 3.3V operation
7. Duty cycle is measured at 2.5V for 5V operation.
8. A LOW and HIGH time of 12 ns corresponds to a PCICLK frequency of 33.33 MHz. For PCICLK frequencies of 30 MHz, 27.5 MHz, and 25 MHz, the LOW and HIGH times are each respectively 13.33 ns, 15 ns, and 16 ns.
9. This information is for modeling purposes only for -1 option and is not guaranteed. Typical output impedance on CPU and PCI clocks is 25 ohms on the -1 device, 40 ohms on the -2, -3, and -3H devices. Output impedance is measured at 1.5V.

Switching Waveform

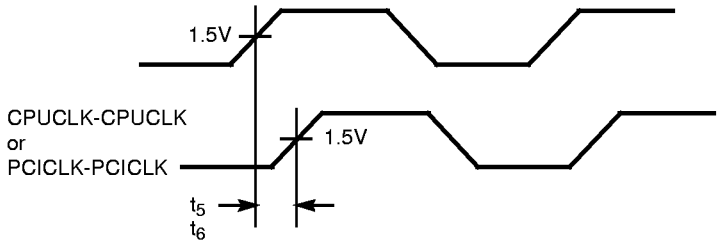
Duty Cycle Timing



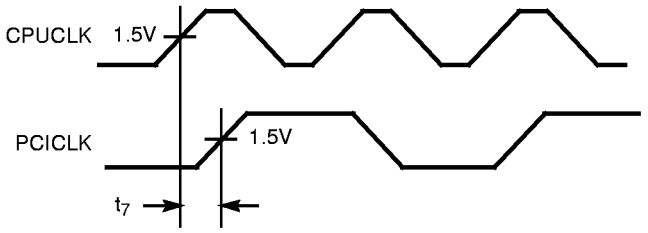
All Outputs Rise/Fall Time



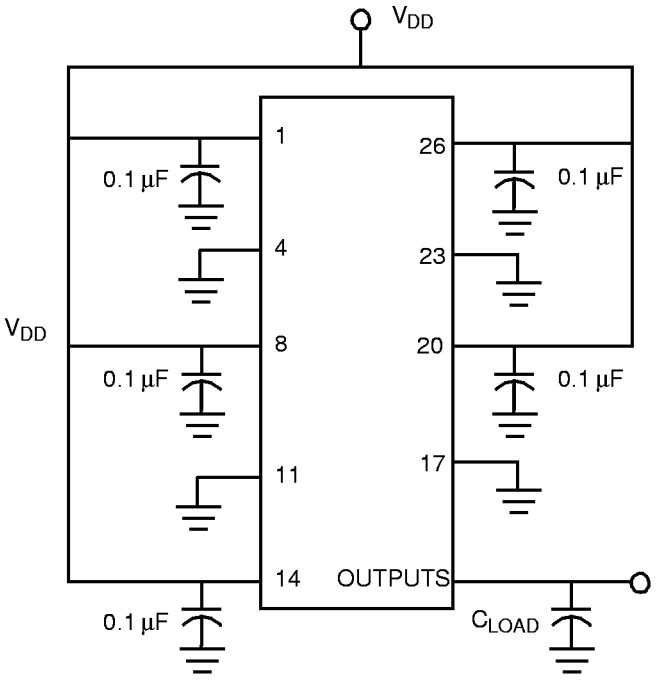
Clock Skew



CPU–PCI Clock Skew



Test Circuit



Note: All capacitors should be placed as close to each pin as possible.

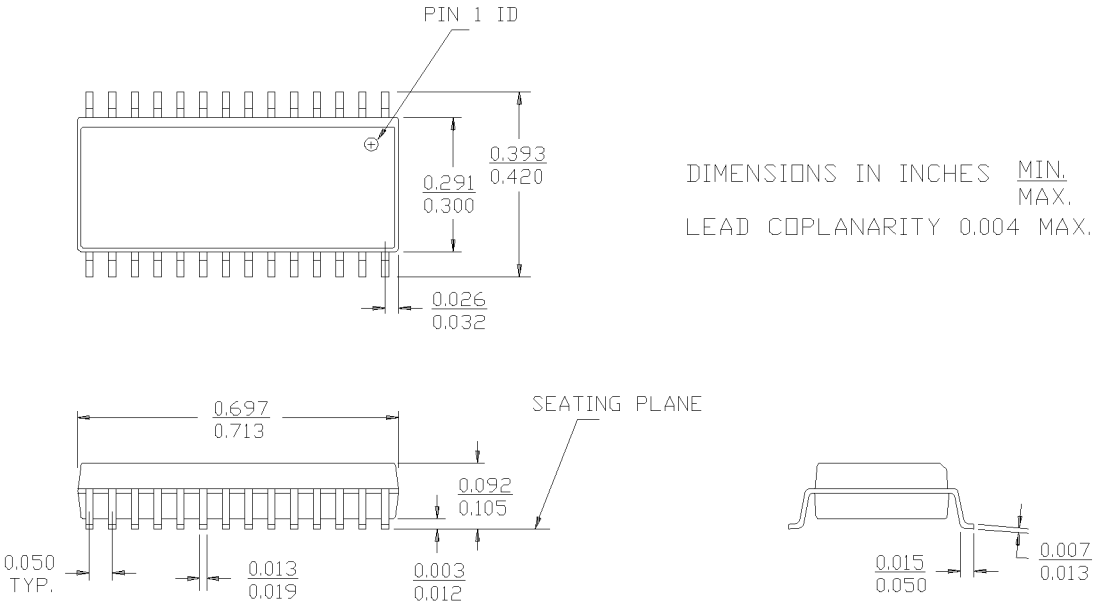
Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2260SC-1	S21	28-Pin SOIC	Commercial
CY2260SC-1H	S21	28-Pin SOIC	Commercial
CY2260SC-2	S21	28-Pin SOIC	Commercial
CY2260SC-3	S21	28-Pin SOIC	Commercial
CY2260SC-3H	S21	28-Pin SOIC	Commercial
CY2260PVC-1	O28	28-Pin SSOP	Commercial
CY2260PVC-2	O28	28-Pin SSOP	Commercial
CY2260PVC-3	O28	28-Pin SSOP	Commercial

Document #: 38-00476-E

Package Diagram

28-Lead (300-Mil) Molded SOIC S21



28-Lead Shrunk Small Outline Package O28