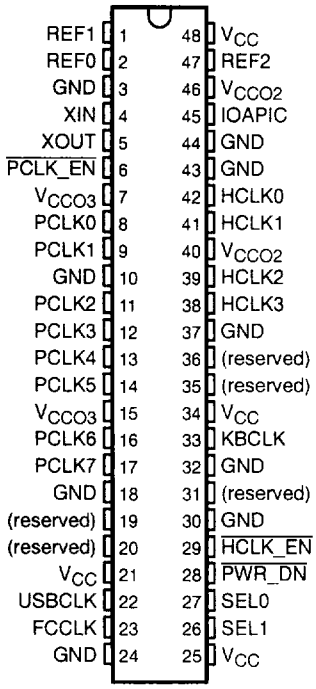
- **P6 Microprocessor Clock Generation With Mixed 2.5-V and 3.3-V Signaling**
- **Four 2.5-V CPU Clock Outputs With Programmable Frequency (60 MHz and 66 MHz)**
- **2.5-V IOAPIC Clock Output**
- **Eight 3.3-V PCI Clock Outputs**
- **3.3-V Serial Bus Clock at 48 MHz**
- **3.3-V Floppy Controller Clock at 24 MHz**
- **3.3-V Keyboard Controller Clock at 12 MHz**
- **Three 3.3-V Reference Clock Outputs at 14.318 MHz**
- **All Output Clock Frequencies Derived From a Single 14.31818-MHz Crystal Input**
- **Internal Loop Filters for Phase-Lock Loops (PLLs)**
- **Power-Down and Test-Mode Support**
- **Packaged in Plastic 300-mil Shrink Small-Outline Package**

**DL PACKAGE**
**(TOP VIEW)**




## description

The CDC9161 is an integrated clock synthesizer and driver specifically designed for use with microprocessors manufactured by Intel. The CDC9161 generates the necessary clock signals for a high-performance PC motherboard and provides both 2.5-V and 3.3-V signaling to support both processor/chipset clocks and PCI clocks.

The four host clock (HCLKn) outputs are programmable to 60 MHz or 66 MHz via the SEL control inputs. The eight PCI clock (PCLKn) outputs are one-half the HCLK frequency, and are offset 1 ns to 4 ns from the rising edge of the host clock. In addition, the CDC9161 generates a 48-MHz bus clock (SBCLK), a 24-MHz floppy controller clock (FCCLK), a 12-MHz keyboard controller clock (KBCLK), and three copies of the 14.318-MHz reference clock (REFn), and a 2.5-V IOAPIC clock at 14.318 MHz. All output frequencies are generated from a 14.31818-MHz crystal input.

A test clock can be driven over the XIN input in the test mode. The oscillator and PLLs are bypassed when operating in the test mode.

PLLs are used to generate the host clock and serial bus clock frequencies. On-chip loop filters and internal feedback eliminate the need for external components. The PCI clock frequency is derived from the base host clock frequency; FCCLK and KBCLK are derived from the serial bus clock frequency.

The host and PCI clock outputs provide low-skew/low-jitter clock signals for reliable clock operation. All outputs are 3 state and are disabled via the SEL inputs.

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## description (continued)

Low-power operation also is provided by the $\overline{\text{HCLK\_EN}}$, $\overline{\text{PCLK\_EN}}$, and $\overline{\text{PWR\_DN}}$ inputs. $\overline{\text{HCLK\_EN}}$, when low, places all host clocks in the logic low state; all other outputs operate normally. $\overline{\text{PCLK\_EN}}$, when low, places all PCI clocks in the logic low state; all other outputs operate normally. $\overline{\text{PWR\_DN}}$, when low, suspends all clock outputs and the internal oscillator and PLLs are disabled to a low-power mode.

Because the CDC9161 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at the XIN input, as well as following any changes to the SEL inputs or after the return to normal operation following a low-to-high transition of $\overline{\text{PWR\_DN}}$.

**FREQUENCY SELECT**

| SEL1 | SEL0 | XIN | HCLKn | PCLKn | REFn | IOAPIC | SBCLK | FCCLK | KBCLK |
|---|---|---|---|---|---|---|---|---|---|
| L | L | 14.31818 MHz† | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| L | H | 14.31818 MHz | 60 MHz | 30 MHz | 14.318 MHz | 14.318 MHz | 48 MHz | 24 MHz | 12 MHz |
| H | L | 14.31818 MHz | 66 MHz | 33 MHz | 14.318 MHz | 14.318 MHz | 48 MHz | 24 MHz | 12 MHz |
| H | H | TCLK‡ | TCLK/2 | TCLK/4 | TCLK | TCLK | TCLK/2 | TCLK/4 | TCLK/8 |

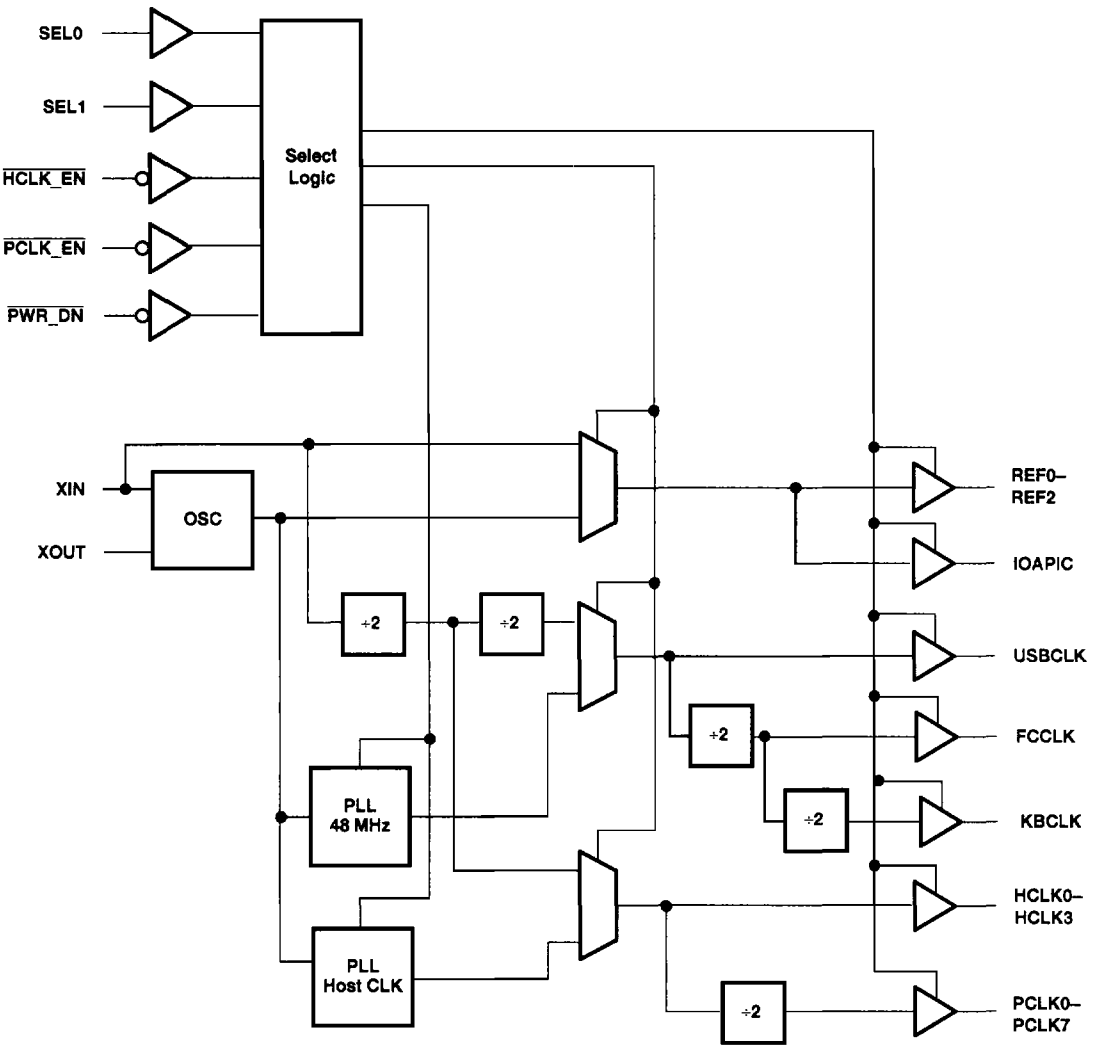
† The allowable reference frequency is minimum = 14.316 MHz, nominal = 14.31818 MHz, and maximum = 14.32 MHz.
‡ TCLK is a test clock at the XIN input during test mode.

**CLOCK ENABLE**

| $\overline{\text{PWR\_DN}}$ | $\overline{\text{HCLK\_EN}}$ | $\overline{\text{PCLK\_EN}}$ | HCLKn | PCLKn | All Other Clocks | VCOs |
|---|---|---|---|---|---|---|
| L | X | X | Static | Static | Static | Static |
| H | L | L | L | L | Active | Active |
| H | L | H | L | Active | Active | Active |
| H | H | L | Active | L | Active | Active |
| H | H | H | Active | Active | Active | Active |

PRODUCT PREVIEW

## functional block diagram

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## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| FCCLK | 23 | O | 3.3-V floppy controller clock output at 24 MHz |
| GND | 3, 10, 18, 24, 30, 32, 37, 43, 44 | GND | Ground |
| $\overline{\text{HCLK\_EN}}$ | 29 | I | Host (CPU) clock enable |
| HCLK0–HCLK3 | 38, 39, 41, 42 | O | 2.5-V host (CPU) clock outputs programmable to 60 MHz or 66 MHz |
| IOAPIC | 45 | O | 2.5-V IOAPIC clock output at 14.318 MHz |
| KBCLK | 33 | O | 3.3-V keyboard controller clock output at 12 MHz |
| $\overline{\text{PCLK\_EN}}$ | 6 | I | PCI clock enable |
| PCLK0–PCLK7 | 8, 9, 11, 12, 13, 14, 16, 17 | O | 3.3-V PCI clock outputs at one-half HCLK frequency |
| $\overline{\text{PWR\_DN}}$ | 28 | I | Power-down enable |
| Reserved | 19, 20, 31, 35, 36 | | Reserved for future use |
| REF0–REF2 | 1, 2, 47 | O | 3.3-V ISA reference clock output at 14.318 MHz |
| SEL0–SEL1 | 26, 27 | I | Clock frequency select inputs |
| USBCLK | 22 | O | 3.3-V universal serial bus clock output at 48 MHz |
| $V_{CC}$ | 21, 25, 34, 48 | Power | 3.3-V core power supply |
| $V_{CCO3}$ | 7, 15 | Power | 3.3-V output power supply |
| $V_{CCO2}$ | 40, 46 | Power | 2.5-V output power supply |
| XIN | 4 | I | Crystal input |
| XOUT | 5 | O | Crystal output |

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 4.6 V
$V_{CCO3}$ ..... −0.5 V to 4.6 V
$V_{CCO2}$ ..... −0.5 V to 3.6 V
Input voltage range, $V_I$ (see Note 1) ..... −0.5 V to 4.6 V
Voltage range applied to any output in the high state or power-off state, $V_O$ ..... −0.5 V to $V_{CC}$ + 0.5 V
Current into any output in the low state, $I_O$ ..... 24 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) ..... −18 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2) ..... 1.2 W
Storage temperature range, $T_{stg}$ ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCDA002.

## recommended operating conditions (see Note 3)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | 3.3-V core supply voltage | 3.135 | 3.465 | V |
| $V_{CCO3}$ | 3.3-V I/O supply voltage | 3.135 | 3.465 | V |
| $V_{CCO2}$ | 2.5-V I/O supply voltage | 2.375 | 2.9 | V |
| $V_{IH3}$ | High-level input voltage | 2.0 | $V_{CCO3}$+0.3 | V |
| $V_{IL3}$ | Low-level input voltage | –0.3 | 0.8 | V |
| $I_{OH}$ | High-level output current | | –12 | mA |
| $I_{OL}$ | Low-level output current | | 12 | mA |
| $T_A$ | Operating free-air temperature | 0 | 70 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 3.135 V, | $I_I$ = –18 mA | | | –1.2 | V |
| $V_{OH3}$ | $V_{CC}$ = 3.135 V, | $I_{OH}$ = –1 mA | | 2.4 | | V |
| $V_{OL3}$ | $V_{CC}$ = 3.135 V, | $I_{OL}$ = 1 mA | | | 0.4 | V |
| $V_{OH2}$ | $V_{CC}$ = 2.375 V | $I_{OH}$ = –1 mA | | 2 | | V |
| $V_{OL2}$ | $V_{CC}$ = 2.375 V | $I_{OL}$ = 1 mA | | | 0.4 | V |
| $I_I$ | $V_{CC}$ = 3.465 V, | $V_I$ = $V_{CC}$ or GND | | –5 | 5 | µA |
| $I_{OZ}$ | $V_{CC}$ = 3.465 V, | $V_O$ = 3.135 V or 0 | | | | µA |
| $I_{CC}$ | $V_{CC}$ = 3.465 V, $V_I$ = $V_{CC}$ or GND | $I_O$ = 0, | Outputs high | | | mA |
| | | | Outputs low | | | |
| | | | Outputs disabled | | | |
| $C_i$ | | | | | 5 | pF |
| $C_o$ | | | | | 6 | pF |
| $L_{pin}$ | | | | | 7 | nH |
| $C_{pd}$ | $V_I$ = 3.135 V or 0 | | | | | pF |

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 4)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Stabilization time† | After change to SEL0 or SEL1 | | 3 | ms |
| | After $\overline{PWR\_DWN}$ ↑ | | 3 | |
| | After power-up | | 3 | |

† Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at XIN.

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## switching characteristics (see Figures 1, 2, and 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 60 MHz | | 66MHz | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_c$† | | HCLKn | 16.7 | | 15 | | ns |
| $t_{p(H)}$† | | HCLKn | 6.0 | | 5.2 | | ns |
| $t_{p(L)}$† | | HCLKn | 5.8 | | 5.0 | | ns |
| $t_r$†‡ | | HCLKn | 0.4 | 1.6 | 0.4 | 1.6 | ns |
| $t_f$†‡ | | HCLKn | 0.4 | 1.6 | 0.4 | 1.6 | ps |
| Jitter† | | HCLKn | | | | ±250 | ps |
| Duty cycle† | | HCLKn | 45% | 55% | 45% | 55% | |
| $t_{skew}$† | | HCLKn | | 250 | | 250 | ps |
| $t_c$† | | PCKLn | 33.3 | | 30 | | ps |
| $t_{p(H)}$† | | PCKLn | 13.3 | | 12 | | ns |
| $t_{p(L)}$† | | PCKLn | 13.3 | | 12 | | ps |
| $t_r$†‡ | | PCKLn | 0.5 | 2.0 | 0.5 | 2.0 | ns |
| $t_f$†‡ | | PCKLn | 0.5 | 2.0 | 0.5 | 2.0 | ns |
| Jitter† | | PCKLn | | ±350 | | ±350 | ps |
| Duty cycle† | | PCKLn | 45% | 55% | 45% | 55% | |
| $t_{skew}$† | | PCKLn | | 500 | | 500 | ps |
| $t_{hpoffset}$† | HCLKn | PCLKn | 1 | 4 | 1 | 4 | ns |
| Clock enable latency | $\overline{PCLK\_EN}$ | PCLKn↑ | 1 | 4 | 1 | 4 | HCLK cycles |
| | $\overline{HCLK\_EN}$ | HCLKn↑ | 1 | 4 | 1 | 4 | |

† Specifications are applicable only after the PLL stabilization time has elapsed.
‡ Rise and fall times are characterized using the load circuits shown in Figure 1.

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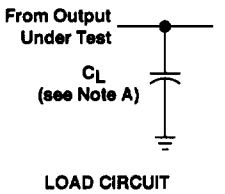
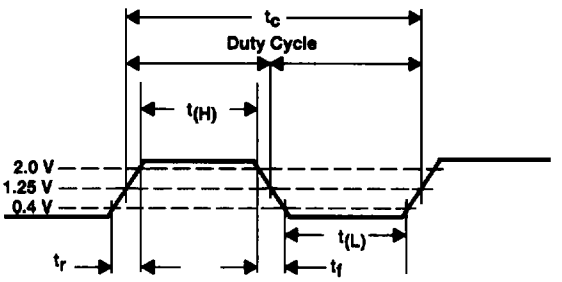
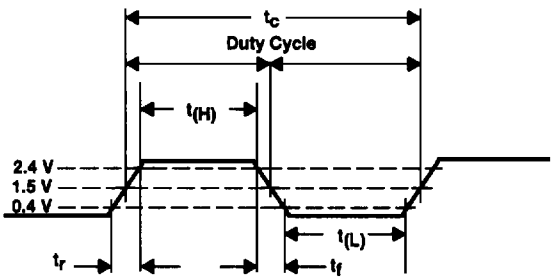
## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




2.5-V CLOCK WAVEFORMS




3.3-V CLOCK WAVEFORMS

NOTES: A. $C_L$ includes probe and jig capacitance.
- $C_L$ = 30pF for PCLK0–PCLK7
- $C_L$ = 45pF for REF0–REF2
- $C_L$ = 20pF for all other outputs

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns,$t_f$ ≤ 2.5 ns.
C. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION

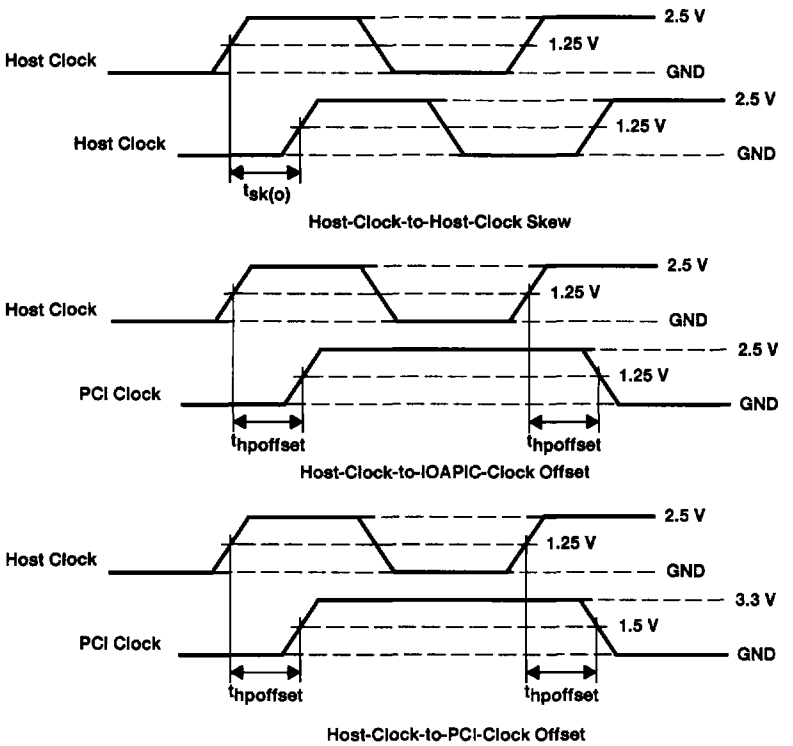



Figure 2. Waveforms for Calculation of $t_{sk(o)}$ and $t_{hpoffset}$

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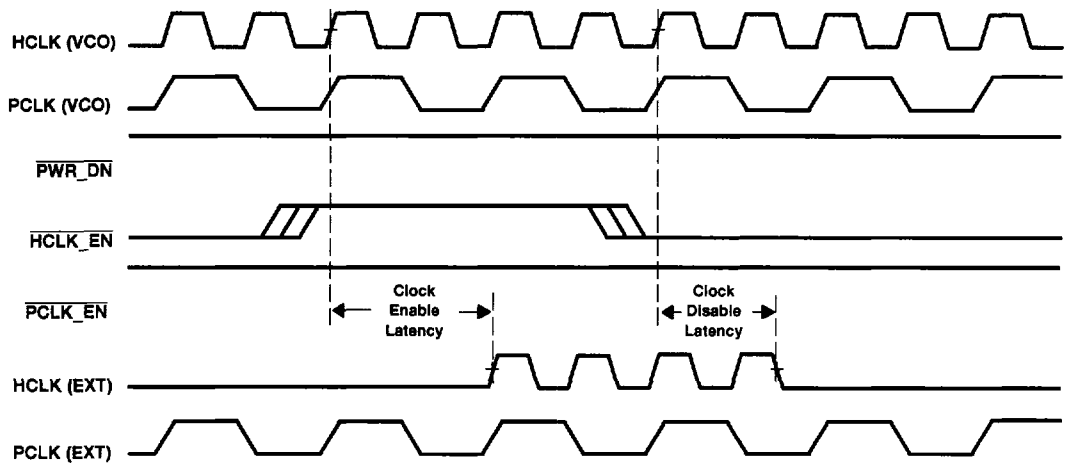
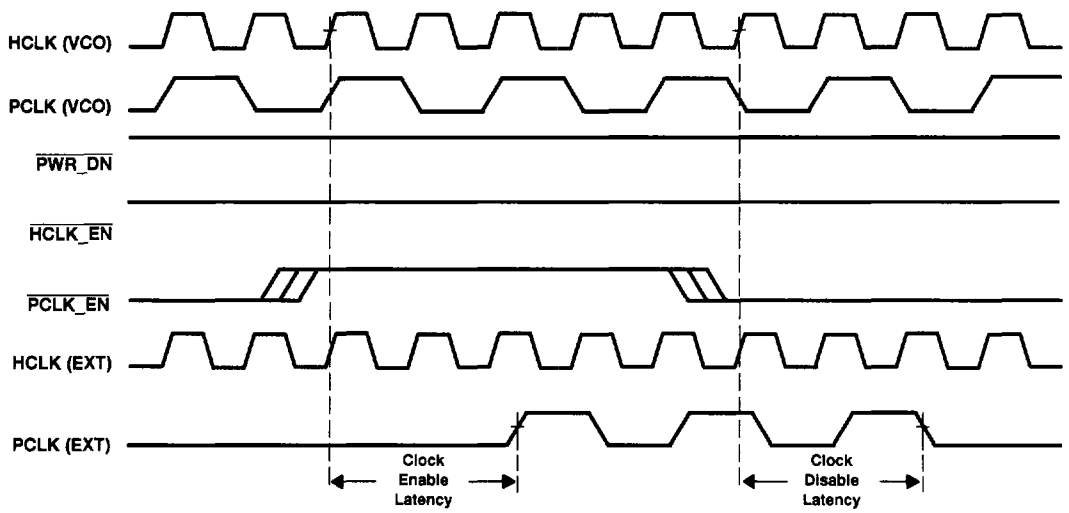
## PARAMETER MEASUREMENT INFORMATION




HCLK Enable Timing Diagram




HCLK Enable Timing Diagram

Figure 3. Timing Example

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## PARAMETER MEASUREMENT INFORMATION

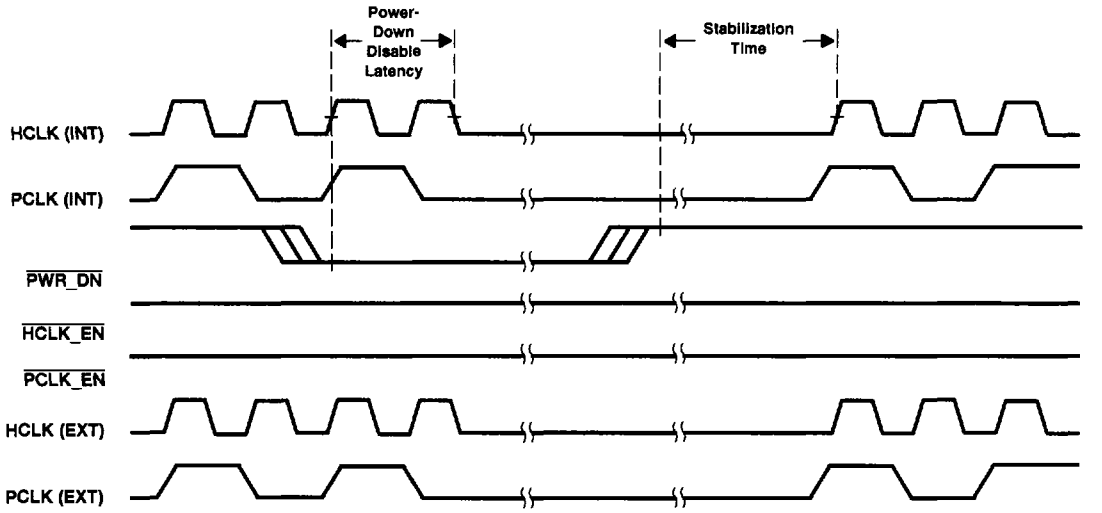


Figure 4. Power-Down Timing

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