

## High Speed CMOS Logic Quad D-Type Flip-Flop with Reset

August 1997 - Revised May 2000

### Features

- **Common Clock and Asynchronous Reset on Four D-Type Flip-Flops**
- **Positive Edge Pulse Triggering**
- **Complementary Outputs**
- **Buffered Inputs**
- **Typical  $f_{MAX} = 50\text{MHz}$  at  $V_{CC} = 5\text{V}$ ,  $C_L = 15\text{pF}$ ,  $T_A = 25^\circ\text{C}$**
- **Fanout (Over Temperature Range)**
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- **Wide Operating Temperature Range . . .  $-55^\circ\text{C}$  to  $125^\circ\text{C}$**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{V}$
- **HCT Types**
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8\text{V}$  (Max),  $V_{IH} = 2\text{V}$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu\text{A}$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The 'HC175 and 'HCT175 are high speed Quad D-type Flip-Flops with individual D-inputs and Q,  $\bar{Q}$  complementary outputs. The devices are fabricated using silicon gate CMOS technology. They have the low power consumption advantage of standard CMOS ICs and the ability to drive 10 LSTTL devices.

Information at the D input is transferred to the Q,  $\bar{Q}$  outputs on the positive going edge of the clock pulse. All four Flip-Flops are controlled by a common clock (CP) and a common reset (MR). Resetting is accomplished by a low voltage level independent of the clock. All four Q outputs are reset to a logic 0 and all four  $\bar{Q}$  outputs to a logic 1.

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC175F3A	-55 to 125	16 Ld CERDIP
CD74HC175E	-55 to 125	16 Ld PDIP
CD74HC175M	-55 to 125	16 Ld SOIC
CD54HCT175F3A	-55 to 125	16 Ld CERDIP
CD74HCT175E	-55 to 125	16 Ld PDIP
CD74HCT175M	-55 to 125	16 Ld SOIC
CD74HCT175W	-55 to 125	Wafer

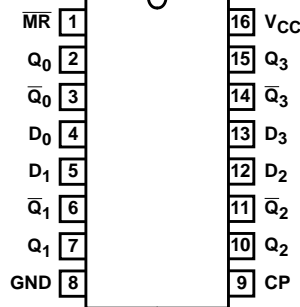
#### NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

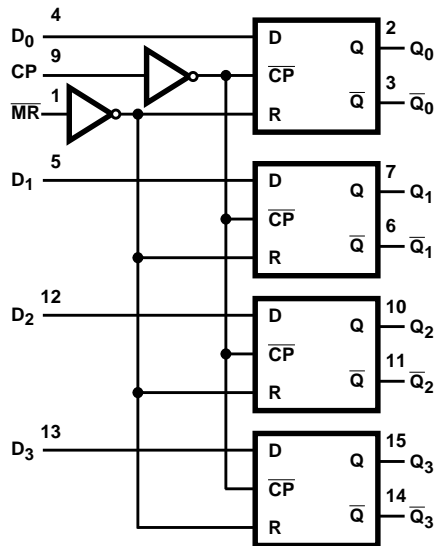
# CD54/74HC175, CD54/74HCT175

## Pinout

CD54HC175, CD54HCT175  
(CERDIP)  
CD74HC175, CD74HCT175  
(PDIP, SOIC)  
TOP VIEW



## Functional Diagram



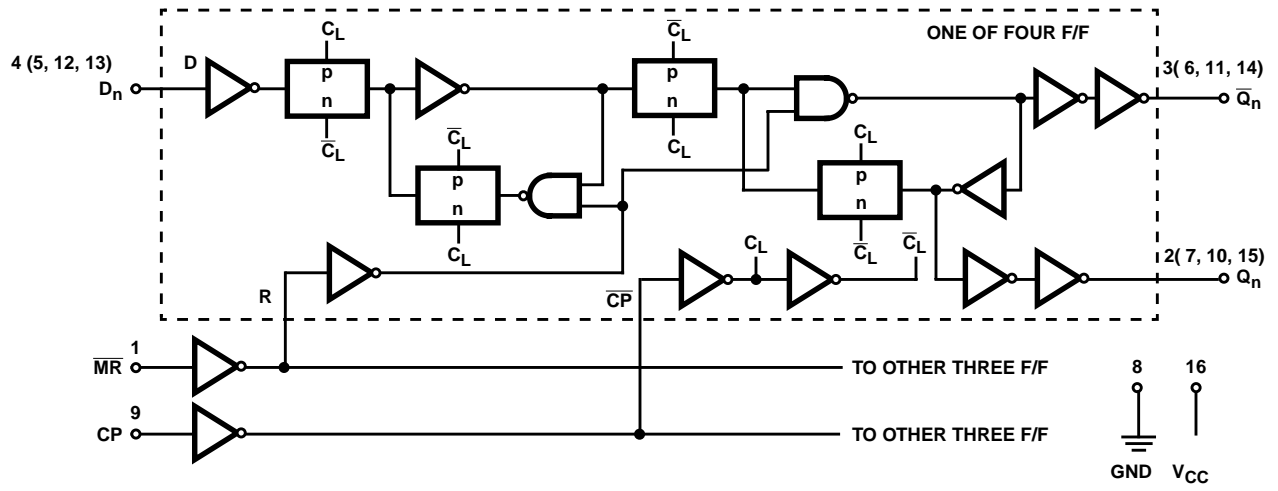
TRUTH TABLE

INPUTS			OUTPUTS	
RESET (MR)	CLOCK CP	DATA D <sub>n</sub>	Q <sub>n</sub>	Q̄ <sub>n</sub>
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q <sub>0</sub>	Q̄ <sub>0</sub>

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition from Low to High Level, Q<sub>0</sub> = Level Before the Indicated Steady-State Input Conditions Were Established.

CD54/74HC175, CD54/74HCT175

Logic Diagram



## CD54/74HC175, CD54/74HCT175

### Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ .....	$\pm 50mA$

### Thermal Information

Thermal Resistance (Typical, Note 3)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package .....	90
SOIC Package .....	110
Maximum Junction Temperature .....	$150^{\circ}C$
Maximum Storage Temperature Range .....	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	$300^{\circ}C$ (SOIC - Lead Tips Only)

### Operating Conditions

Temperature Range ( $T_A$ ) .....	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types .....	.2V to 6V
HCT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I$ , $V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

### DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO +85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
-0.02			6	5.9	-	-	5.9	-	5.9	-	V	
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
-5.2			6	5.48	-	-	5.34	-	5.2	-	V	
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
0.02			6	-	-	0.1	-	0.1	-	0.1	V	
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	6	-	-	8	-	80	-	160	$\mu A$

**CD54/74HC175, CD54/74HCT175**

**DC Electrical Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO +85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> to GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4)	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

**NOTES:**

- For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.
- Die for this part number is available which meets all electrical specifications.

**HCT Input Loading Table**

INPUT	UNIT LOADS
MR	1
CP	0.60
D	0.15

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications table, e.g. 360μA max at 25°C.

**Prerequisite For Switching Specifications**

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Clock Pulse Width	t <sub>w</sub>	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
MR Pulse Width	t <sub>w</sub>	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns

**CD54/74HC175, CD54/74HCT175**

**Prerequisite For Switching Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Setup Time, Data to Clock	t <sub>SU</sub>	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
Hold Time, Data to Clock	t <sub>H</sub>	-	2	5	-	-	5	-	5	-	ns
			4.5	5	-	-	5	-	5	-	ns
			6	5	-	-	5	-	5	-	ns
Removal Time, $\overline{MR}$ to Clock	t <sub>REM</sub>	-	2	5	-	-	5	-	5	-	ns
			4.5	5	-	-	5	-	5	-	ns
			6	5	-	-	5	-	5	-	ns
Clock Frequency	f <sub>MAX</sub>	-	2	6	-	-	5	-	4	-	MHz
			4.5	30	-	-	25	-	20	-	MHz
			6	35	-	-	29	-	23	-	MHz

**HCT TYPES**

Clock Pulse Width	t <sub>w</sub>	-	4.5	20	-	-	25	-	30	-	ns
$\overline{MR}$ Pulse Width	t <sub>w</sub>	-	4.5	20	-	-	25	-	30	-	ns
Setup Time Data to Clock	t <sub>SU</sub>	-	4.5	20	-	-	25	-	30	-	ns
Hold Time Data to Clock	t <sub>H</sub>	-	4.5	5	-	-	5	-	5	-	ns
Removal Time $\overline{MR}$ to Clock	t <sub>REM</sub>	-	4.5	5	-	-	5	-	5	-	ns
Clock Frequency	f <sub>MAX</sub>	-	4.5	25	-	-	20	-	16	-	MHz

**Switching Specifications** Input t<sub>r</sub>, t<sub>f</sub> = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS		
				TYP	MAX	MAX	MAX			
Propagation Delay, Clock to Q or $\overline{Q}$	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	175	220	265	ns		
			4.5	-	35	44	53	ns		
			6	-	30	37	45	ns		
		C <sub>L</sub> = 15pF	5	14	-	-	-	ns		
			Propagation Delay, $\overline{MR}$ to Q or $\overline{Q}$	C <sub>L</sub> = 50pF	2	-	175	220	265	ns
					4.5	-	35	44	53	ns
6	-	30			37	45	ns			
C <sub>L</sub> = 15pF	5	14	-	-	-	ns				
	Output Transition Times	C <sub>L</sub> = 50pF	2	-	75	95	110	ns		
			4.5	-	15	19	22	ns		
6			-	13	16	19	ns			
Input Capacitance	C <sub>IN</sub>	-	-	-	10	10	10	pF		
Power Dissipation Capacitance (Notes 6, 7)	C <sub>PD</sub>	-	5	65	-	-	-	pF		

## CD54/74HC175, CD54/74HCT175

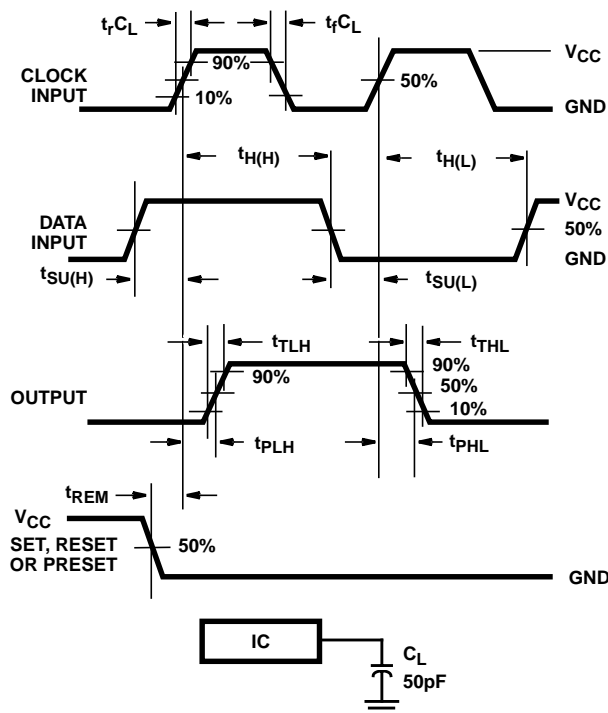
### Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
<b>HCT TYPES</b>								
Propagation Delay, Clock to Q or $\bar{Q}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	33	41	50	ns
		$C_L = 15\text{pF}$	5	13	-	-	-	ns
Propagation Delay, MR to Q or $\bar{Q}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	35	44	53	ns
		$C_L = 15\text{pF}$	5	17	-	-	-	ns
Output Transition Times	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	15	19	22	ns
Input Capacitance	$C_{IN}$	-	-	-	10	10	10	pF
Power Dissipation Capacitance (Notes 6, 7)	$C_{PD}$	-	5	67	-	-	-	pF

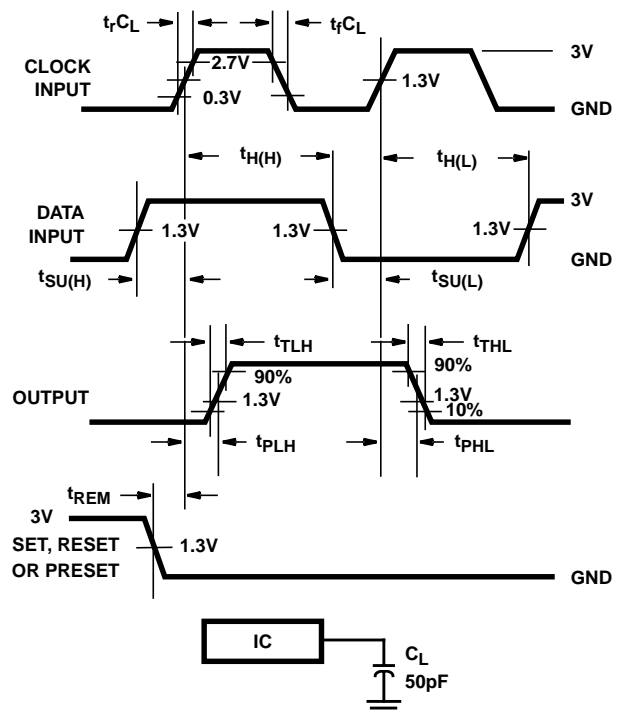
**NOTES:**

6.  $C_{PD}$  is used to determine the dynamic power consumption, per flip-flop.
7.  $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2 + f_O)$  where  $f_i$  = Input Frequency,  $f_O$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

### Test Circuits and Waveforms



**FIGURE 1. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**



**FIGURE 2. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**

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PRODUCT SUPPORT: [TRAINING](#)

## CD54HC175, High Speed CMOS Logic Quad D-Type Flip-Flops with Reset

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	CD54HC175
Voltage Nodes (V)	6, 5, 2

### FEATURES

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- Common Clock and Asynchronous Reset on Four D-Type Flip-Flops
- Positive Edge Pulse Triggering
- Complementary Outputs
- Buffered Inputs
- Typical  $f_{MAX} = 50\text{MHz}$  at  $V_{CC} = 5\text{V}$ ,  $C_L = 15\text{pF}$ ,  $T_A = 25^\circ\text{C}$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ\text{C}$  to  $125^\circ\text{C}$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{V}$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8\text{V}$  (Max),  $V_{IH} = 2\text{V}$  (Min)
  - CMOS Input Compatibility,  $I_1 \leq 1\mu\text{A}$  at  $V_{OL}$ ,  $V_{OH}$

### DESCRIPTION

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The 'HC175 and 'HCT175 are high speed Quad D-type Flip-Flops with individual D-inputs and Q,  $\bar{Q}$  complementary outputs. The devices are fabricated using silicon gate CMOS technology. They have the low power consumption advantage of standard CMOS ICs and the ability to drive 10 LSTTL devices.

Information at the D input is transferred to the Q,  $\bar{Q}$  outputs on the positive going edge of the clock pulse. All four Flip-Flops are controlled by a common clock (CP) and a common reset (MR). Resetting is accomplished by a low voltage level independent of the clock. All four Q outputs are reset to a logic 0 and all four  $\bar{Q}$  outputs to a logic 1.

### TECHNICAL DOCUMENTS

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To view the following documents, [Acrobat Reader 4.0](#) is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

### DATASHEET

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Full datasheet in Acrobat PDF: [cd54hc175.pdf](#) (44 KB, Rev. A) (Updated: 05/19/2000)

### APPLICATION NOTES

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View Application Notes for [Digital Logic](#)

- [CMOS Power Consumption and CPD Calculation \(Rev. B\)](#) (SCAA035B - Updated: 06/01/1997)
- [Designing With Logic \(Rev. C\)](#) (SDYA009C - Updated: 06/01/1997)

- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Implications of Slow or Floating CMOS Inputs \(Rev. C\)](#) (SCBA004C - Updated: 02/01/1998)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)
- [SN54/74HCT CMOS Logic Family Applications and Restrictions](#) (SCLA011 - Updated: 05/01/1996)
- [Selecting the Right Texas Instruments Signal Switch](#) (SZZA030 - Updated: 09/07/2001)
- [TI IBIS File Creation, Validation, and Distribution Processes](#) (SZZA034 - Updated: 08/29/2002)
- [Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh \(Rev. A\)](#) (SZZA036A - Updated: 02/27/2003)
- [Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc](#) (SCLA008 - Updated: 04/01/1996)

**MORE LITERATURE**

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- [Enhanced Plastic Portfolio Brochure](#) (SGZB004, 387 KB - Updated: 08/19/2002)
- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [Military Brief](#) (SGYN138, 803 KB - Updated: 10/10/2000)
- [Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet \(Rev. A\)](#) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- [Palladium Lead Finish User's Manual](#) (SDYV001, 2041 KB - Updated: 11/01/1996)
- [QML Class V Space Products Military Brief \(Rev. A\)](#) (SGZN001A, 257 KB - Updated: 10/07/2002)

**USER GUIDES**

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- [LOGIC Pocket Data Book](#) (SCYD013, 4837 KB - Updated: 12/05/2002)
- [Signal Switch Data Book](#) (SCDD003, 10259 KB - Updated: 03/19/2001)

**PRICING/AVAILABILITY/PKG**

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DEVICE INFORMATION Updated Daily								TI INVENTORY STATUS As Of 08:00 AM GMT, 17 Apr 2003			REPORTED DISTRIBUTOR INVENTORY As Of 08:00 AM GMT, 17 Apr 2003		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE   PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY   SUS	STD PACK QTY	IN STOCK	IN PROGRESS QTY   DATE	LEAD TIME	DISTRIBUTOR COMPANY   REGION	IN STOCK	PURCHASE
8408901EA	ACTIVE	<a href="#">CDIP (J)</a>   16	-55 TO 125		<a href="#">View Contents</a>	1KU   1.86	1	403*	>10k   20 May	8 WKS	<a href="#">Avnet</a>   Americas	267	<a href="#">BUY NOW</a>
CD54HC175F3A	ACTIVE	<a href="#">CDIP (J)</a>   16	-55 TO 125	8408901EA	<a href="#">View Contents</a>	1KU   1.86	1	211*	>10k   20 May	8 WKS	<a href="#">EBV Elektronik</a>   Europe	50	<a href="#">BUY NOW</a>
											None Reported <a href="#">View Distributors</a>		

Table Data Updated on: 4/17/2003

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PRODUCT SUPPORT: [TRAINING](#)

## CD54HCT175, High Speed CMOS Logic Quad D-Type Flip-Flops with Reset

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	CD54HCT175
Voltage Nodes (V)	5

### FEATURES

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- Common Clock and Asynchronous Reset on Four D-Type Flip-Flops
- Positive Edge Pulse Triggering
- Complementary Outputs
- Buffered Inputs
- Typical  $f_{MAX} = 50\text{MHz}$  at  $V_{CC} = 5\text{V}$ ,  $C_L = 15\text{pF}$ ,  $T_A = 25^\circ\text{C}$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ\text{C}$  to  $125^\circ\text{C}$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{V}$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8\text{V (Max)}$ ,  $V_{IH} = 2\text{V (Min)}$
  - CMOS Input Compatibility,  $I_1 \leq 1\mu\text{A}$  at  $V_{OL}$ ,  $V_{OH}$

### DESCRIPTION

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The 'HC175 and 'HCT175 are high speed Quad D-type Flip-Flops with individual D-inputs and Q,  $\bar{Q}$  complementary outputs. The devices are fabricated using silicon gate CMOS technology. They have the low power consumption advantage of standard CMOS ICs and the ability to drive 10 LSTTL devices.

Information at the D input is transferred to the Q,  $\bar{Q}$  outputs on the positive going edge of the clock pulse. All four Flip-Flops are controlled by a common clock (CP) and a common reset (MR). Resetting is accomplished by a low voltage level independent of the clock. All four Q outputs are reset to a logic 0 and all four  $\bar{Q}$  outputs to a logic 1.

### TECHNICAL DOCUMENTS

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To view the following documents, [Acrobat Reader 4.0](#) is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

### DATASHEET

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Full datasheet in Acrobat PDF: [cd54hct175.pdf](#) (44 KB, Rev.A) (Updated: 05/19/2000)

### APPLICATION NOTES

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View Application Notes for [Digital Logic](#)

- [CMOS Power Consumption and CPD Calculation \(Rev. B\)](#) (SCAA035B - Updated: 06/01/1997)
- [Designing With Logic \(Rev. C\)](#) (SDYA009C - Updated: 06/01/1997)

- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Implications of Slow or Floating CMOS Inputs \(Rev. C\)](#) (SCBA004C - Updated: 02/01/1998)
- [SN54/74HCT CMOS Logic Family Applications and Restrictions](#) (SCLA011 - Updated: 05/01/1996)
- [TI IBIS File Creation, Validation, and Distribution Processes](#) (SZZA034 - Updated: 08/29/2002)
- [Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sheet \(Rev. A\)](#) (SZZA036A - Updated: 02/27/2003)
- [Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc](#) (SCLA008 - Updated: 04/01/1996)

**MORE LITERATURE**

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- [Enhanced Plastic Portfolio Brochure](#) (SGZB004, 387 KB - Updated: 08/19/2002)
- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [Military Brief](#) (SGYN138, 803 KB - Updated: 10/10/2000)
- [Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet \(Rev. A\)](#) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- [Palladium Lead Finish User's Manual](#) (SDYV001, 2041 KB - Updated: 11/01/1996)
- [QML Class V Space Products Military Brief \(Rev. A\)](#) (SGZN001A, 257 KB - Updated: 10/07/2002)

**USER GUIDES**

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- [LOGIC Pocket Data Book](#) (SCYD013, 4837 KB - Updated: 12/05/2002)
- [Signal Switch Data Book](#) (SCDD003, 10259 KB - Updated: 03/19/2001)

**PRICING/AVAILABILITY/PKG**

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DEVICE INFORMATION Updated Daily								TI INVENTORY STATUS As Of 08:00 AM GMT, 17 Apr 2003			REPORTED DISTRIBUTOR INVENTORY As Of 08:00 AM GMT, 17 Apr 2003		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE   PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY   SUS	STD PACK QTY	IN STOCK	IN PROGRESS QTY   DATE	LEAD TIME	DISTRIBUTOR COMPANY   REGION	IN STOCK	PURCHASE
5962-8970101EA	ACTIVE	<a href="#">CDIP (J)</a>   16	-55 TO 125		<a href="#">View Contents</a>	1KU   4.18	1	79*	>10k   20 May	8 WKS	<a href="#">EBV Elektronik</a>   Europe	50	<a href="#">BUY NOW</a>
CD54HCT175F3A	ACTIVE	<a href="#">CDIP (J)</a>   16	-55 TO 125	5962-8970101EA	<a href="#">View Contents</a>	1KU   4.16	1	2*	>10k   20 May	8 WKS	None Reported <a href="#">View Distributors</a>		

Table Data Updated on: 4/17/2003