SIEMENS

1M x 16-Bit Dynamic RAM
1k & 4k Refresh
(Fast Page Mode)

HYB5116160BSJ-50/-60
HYB5116160BSJ-50/-60
HYB3116160BSJ/BST(L)-50/-60
HYB3118160BSJ/BST(L)-50/-60

Advanced Information

- 1 048 576 words by 16-bit organization
- 0 to 70 °C operating temperature
- Fast Page Mode operation
- Performance:

		-50	-60	
t_{RAC}	$\overline{RAS}$ access time	50	60	ns
t_{CAC}	$\overline{CAS}$ access time	13	15	ns
t_{AA}	Access time from address	25	30	ns
t_{RC}	Read/Write cycle time	84	104	ns
t_{PC}	Fast page mode cycle time	35	40	ns

- Power Dissipation, Refresh & Addressing:

	HYB5116160		HYB3116160		HYB5118160		HYB3118160		
	-50	-60	-50	-60	-50	-60	-50	-60	
Power Supply	5V ± 10%		3.3V± 0.3V		5V ± 10%		3.3V± 0.3V		
Addressing	12/8		12/8		10/10		10/10		
Refresh	4096 cycles / 64 ms				1024 cycles / 16 ms				
L-version	4096 cycles / 128 ms				1024 cycles / 128 ms				
Active	330	220	216	144	715	632	468	414	mW
TTL Standby	11		7,2		11		7,2		mW
CMOS Standby	5,5		3,6		5,5		3,6		mW
CMOS Standby (L-version)	1,1		0,72		1,1		0,72		mW

- Read, write, read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh and Self Refresh (on L-versions only).
- All inputs, outputs and clocks fully TTL (5V versions) and LV-TTL (3.3V version)-compatible
- Plastic Package: P-SOJ-42 400 mil
  P-TSOPII-50/44 400 mil

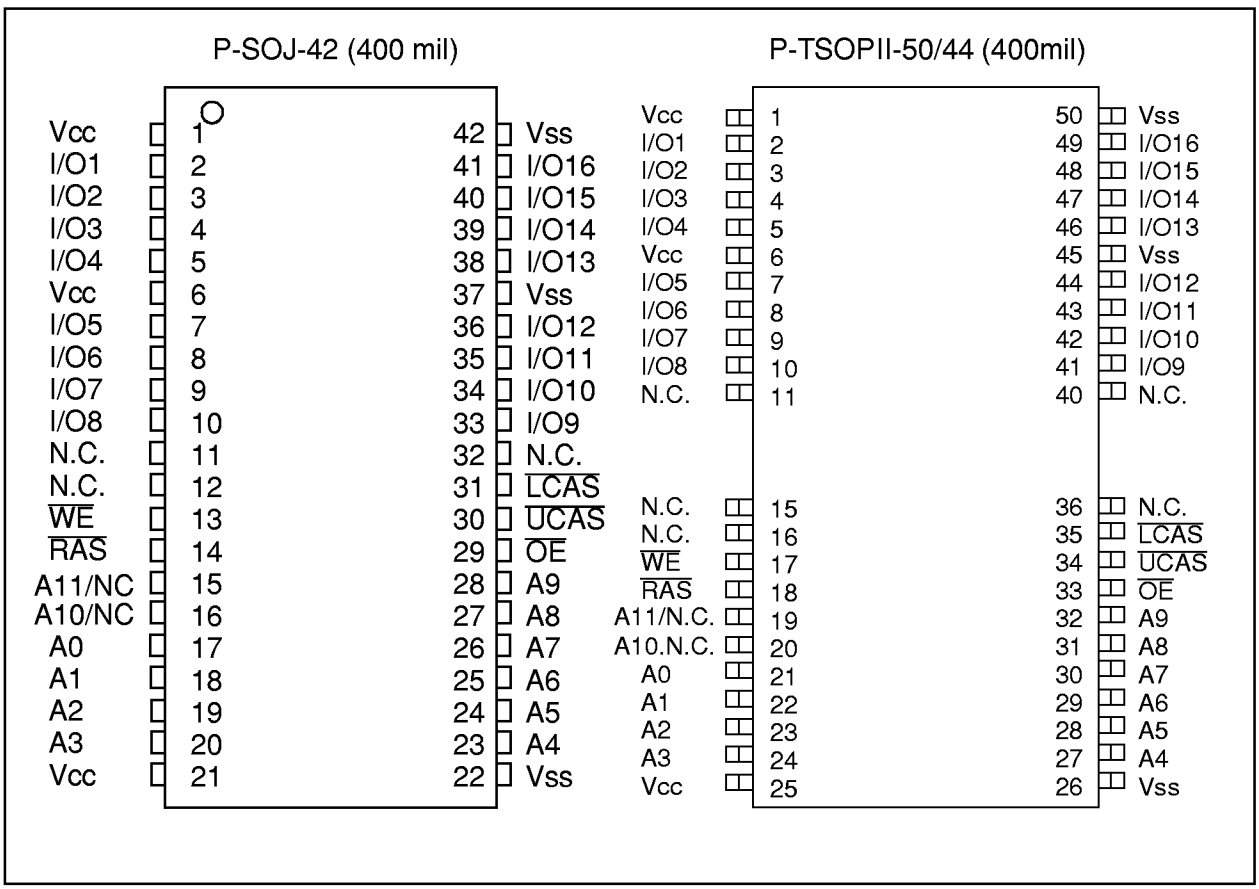
The HYB5(3)116(8)160 are 16 MBit dynamic RAMs based on die revisions „G“ & „F“ and organized as 1 048 576 words by 16-bits. The HYB 5(3)116(8)160 utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the The HYB 5(3)116(8)160 to be packaged in a standard SOJ 42 and TSOPII -50/44 plastic package with 400 mil width. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. The HYB3116(8)160BSTL („L-versions“) have a very low power „sleep mode“ supported by Self Refresh.

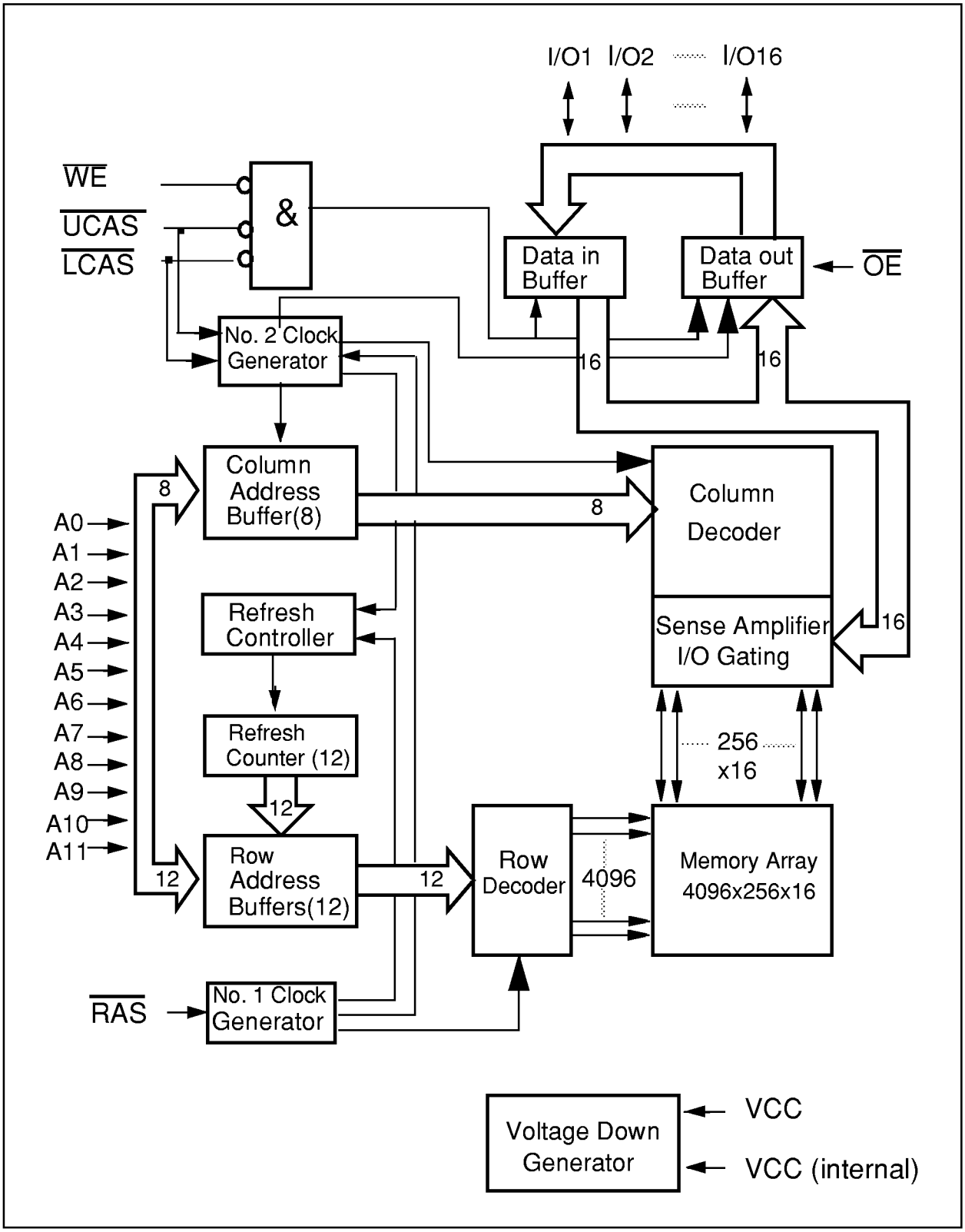
Ordering Information

Type	Ordering Code	Package	Descriptions
1k - Refresh Versions:			
HYB 5118160BSJ-50	Q67100-	P-SOJ-42 400 mil	5V 50ns FPM-DRAM
HYB 5118160BSJ-60	Q67100-	P-SOJ-42 400 mil	5V 60ns FPM-DRAM
HYB 3118160BSJ-50	Q67100-	P-SOJ-42 400 mil	3.3V 50ns FPM-DRAM
HYB 3118160BSJ-60	Q67100-	P-SOJ-42 400 mil	3.3V 60ns FPM-DRAM
HYB 3118160BST-50	Q67100-	P-TSOPII-50/44 400 mil	3.3V 50ns FPM-DRAM
HYB 3118160BST-60	Q67100-	P-TSOPII-50/44 400 mil	3.3V 60ns FPM-DRAM
HYB 3118160BSTL-50	Q67100-	P-TSOPII-50/44 400 mil	3.3V 50ns LP-FPM-DRAM
HYB 3118160BSTL-60	Q67100-	P-TSOPII-50/44 400 mil	3.3V 60ns LP-FPM-DRAM
4k - Refresh Versions:			
HYB 5116160BSJ-50	Q67100-	P-SOJ-42 400 mil	5V 50ns FPM-DRAM
HYB 5116160BSJ-60	Q67100-	P-SOJ-42 400 mil	5V 60ns FPM-DRAM
HYB 3116160BSJ-50	Q67100-	P-SOJ-42 400 mil	3.3V 50ns FPM-DRAM
HYB 3116160BSJ-60	Q67100-	P-SOJ-42 400 mil	3.3V 60ns FPM-DRAM
HYB 3116160BST-50	Q67100-	P-TSOPII-50/44 400 mil	3.3V 50ns FPM-DRAM
HYB 3116160BST-60	Q67100-	P-TSOPII-50/44 400 mil	3.3V 60ns FPM-DRAM
HYB 3116160BSTL-50	Q67100-	P-TSOPII-50/44 400 mil	3.3V 50ns LP-FPM-DRAM)
HYB 3116160BSTL-60	Q67100-	P-TSOPII-50/44 400 mil	3.3V 60ns LP FPM-DRAM

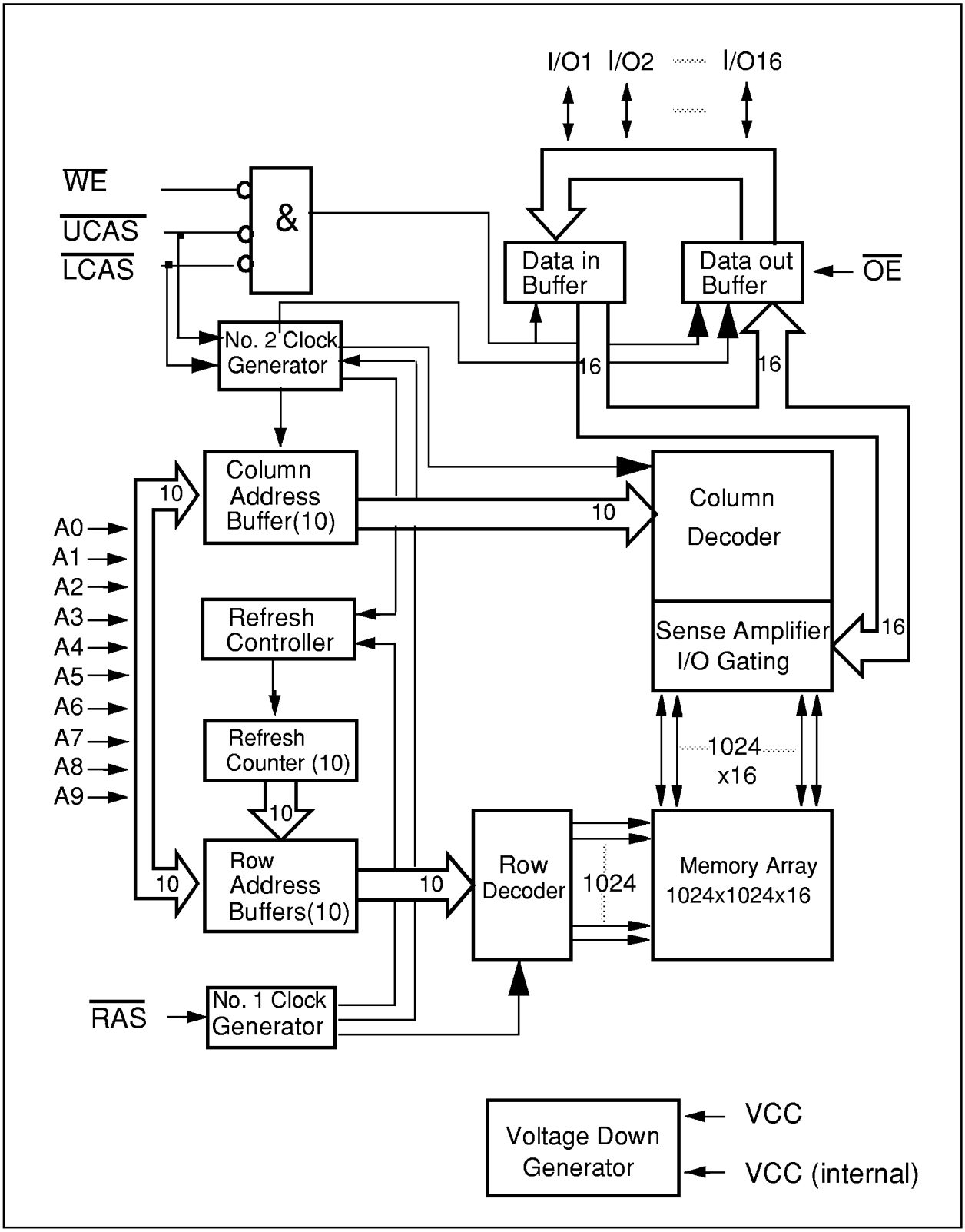
Pin Names and Configuration:

	HYB5(3)116160 4k-refresh	HYB5(3)118160 1k-refresh
Row Address Inputs	A0 - A11	A0 - A9
Column Address Inputs	A0 - A7	A0 - A9
Row Address Strobe	$\overline{RAS}$	
Upper Column Address Strobe	$\overline{UCAS}$	
Lower Column Address Strobe	$\overline{LCAS}$	
Output Enable	$\overline{OE}$	
Data Input/Output	I/O1-I/O16	
Read/Write Input	$\overline{WE}$	
Power Supply	V_{CC}	
Ground (0 V)	V_{SS}	
not connected		N.C.





Block Diagram for HYB 5116160BSJ



Block Diagram for HYB 5118160BSJ

Absolute Maximum Ratings :

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to 150 °C
Input/output voltage (5V versions) ..... -0.5 to min (Vcc+0.5,7.0) V
Input/output voltage (3.3V versions) ..... -0.5 to min (Vcc+0.5,4.6) V
Power supply voltage (5V versions) ..... -1.0V to 7.0 V
Power supply voltage (3.3V versions) ..... -1.0V to 4.6 V
Power dissipation(5V versions) ..... 1.0 W
Power dissipation (3.3V versions) ..... 0.5 W
Data out current (short circuit) ..... 50 mA

Note:

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, t_T = 2 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
5V versions:					
Power supply voltage	V_{CC}	4.5	5.5	V	
Input high voltage	V_{IH}	2.4	Vcc+0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	1)
3.3V versions:					
Power supply voltage	V_{CC}	3.0	3.6	V	
Input high voltage	V_{IH}	2.0	Vcc+0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
TTL Output high voltage (I_{OUT} = – 2 mA)	V_{OH}	2.4	–	V	1)
TTL Output low voltage (I_{OUT} = 2 mA)	V_{OL}	–	0.4	V	1)
CMOS Output high voltage (I_{OUT} = –100 uA)	V_{OH}	VCC-0.2	–	V	
CMOS Output low voltage (I_{OUT} = 100 uA)	V_{OL}	–	0.2	V	

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, t_T = 2 ns

Parameter	Symbol	Limit Values			Unit	Notes
		min.	max.			
			1k	4k		
Common Parameters:						
Input leakage current (0 V ≤ V_{IH} ≤ Vcc + 0.3V, all other pins = 0 V)	$I_{I(L)}$	– 10	10		µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ Vcc + 0.3V)	$I_{O(L)}$	– 10	10		µA	1)
Average V_{CC} supply current: -50 ns version -60 ns version (RAS, CAS, address cycling: t_{RC} = t_{RC} min.)	I_{CC1}	 – –	 130 115	 50 40	 mA mA	 2) 3) 4) 2) 3) 4)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2		mA	–
Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles: -50 ns version -60 ns version ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)	I_{CC3}	 – –	 130 115	 50 40	 mA mA	 2) 4) 2) 4)
Average V_{CC} supply current,during fast page mode : -50 ns version -60 ns version ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling:t_{PC} = t_{PC} min.)	I_{CC4}	 – –	 40 30	 25 20	 mA mA	 2) 3) 4) 2) 3) 4)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1 200		mA µA	1) L-Version
Average V_{CC} supply current, during $\overline{CAS}$-before-RAS refresh mode: -50 ns version -60 ns version ($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = t_{RC} min.)	I_{CC6}	 – –	 130 115	 50 40	 mA mA	 2) 4) 2) 4)
Average Self Refresh Current (CBR cycle with tRAS>TRASSmin., $\overline{CAS}$ held low, $\overline{WE}$=Vcc-0.2V, Address and Din=Vcc - 0.2V or 0.2V)	I_{CC7}	–	250		µA	L-Version only

Capacitance

T_A = 0 to 70 °C, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$,$\overline{WE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1-I/O16)	C_{IO}	–	7	pF

AC Characteristics [5)6)]

16FP/FG

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 % / V_{CC} =3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
common parameters							
Random read or write cycle time	t_{RC}	90	–	110	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	–	40	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10k	15	10k	ns	
Row address setup time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	8	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	10	–	15	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	37	20	45		
$\overline{RAS}$ to column address delay time	t_{RAD}	13	25	15	30	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	ns	
Transition time (rise and fall)	t_T	3	50	3	50	ns	7
Refresh period for 1k refresh version	t_{REF}	–	16	–	16	ms	
Refresh period for 4k refresh version	t_{REF}	–	64	–	64	ms	
Refresh period for L-version		–	128	–	128	ms	
Read Cycle							
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	–	13	–	15	ns	8, 9
Access time from column address	t_{AA}	–	25	–	30	ns	8,10
$\overline{OE}$ access time	t_{OEA}	–	13	–	15	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	11
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	11
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	–	0	–	ns	8

AC Characteristics *(cont'd)* 5)6) 16FP/FG

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 % / V_{CC} =3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	12
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	12
Data to $\overline{OE}$ low delay	t_{DZO}	0	–	0	–	ns	13
$\overline{CAS}$ high to data delay	t_{CDD}	13	–	15	–	ns	14
$\overline{OE}$ high to data delay	t_{ODD}	13	–	15	–	ns	14
Write Cycle							
Write command hold time	t_{WCH}	8	–	10	–	ns	
Write command pulse width	t_{WP}	8	–	10	–	ns	
Write command setup time	t_{WCS}	0	–	0	–	ns	15
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	–	15	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13	–	15	–	ns	
Data setup time	t_{DS}	0	–	0	–	ns	16
Data hold time	t_{DH}	10	–	10	–	ns	16
Data to $\overline{CAS}$ low delay	t_{DZC}	0	–	0	–	ns	13
Read-Modify-Write Cycle							
Read-write cycle time	t_{RWC}	126	–	150	–	ns	
$\overline{RAS}$ to WE delay time	t_{RWD}	68	–	80	–	ns	15
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	31	–	35	–	ns	15
Column address to $\overline{WE}$ delay time	t_{AWD}	43	–	50	–	ns	15
$\overline{OE}$ command hold time	t_{OEH}	13	–	15	–	ns	
Fast Page Mode Cycle							
Fast page mode cycle time	t_{PC}	35	–	40	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	30	–	35	ns	7
$\overline{RAS}$ pulse width	t_{RAS}	50	200k	60	200k	ns	
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHPC}	30	–	35	–	ns	

AC Characteristics *(cont'd)* 5)6) 16FP/FG

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 % / V_{CC} =3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
Fast Page Mode Read-Modify-Write Cycle							
Fast page mode read-write cycle time	t_{PRWC}	71	–	80	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$	t_{CPWD}	48	–	55	–	ns	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle							
$\overline{CAS}$ setup time	t_{CSR}	10	–	10	–	ns	
$\overline{CAS}$ hold time	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	ns	
Write to $\overline{RAS}$ precharge time	t_{WRP}	10	–	10	–	ns	
Write hold time referenced to $\overline{RAS}$	t_{WRH}	10	–	10	–	ns	
$\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle							
$\overline{CAS}$ precharge time	t_{CPT}	35	–	40	–	ns	
Self Refresh Cycle							
$\overline{RAS}$ pulse width	t_{RASS}	100k	_	100k	_	ns	17
$\overline{RAS}$ precharge time	t_{RPS}	95	_	110	_	ns	17
$\overline{CAS}$ hold time	t_{CHS}	-50	_	-50	_	ns	17

Notes:

1) All voltages are referenced to VSS.

2) ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.

3) ICC1 and ICC4 depend on output loading. Specified values are measured with the output open.

4) Address can be changed once or less while $\overline{RAS}$ = VIL. In the case of ICC4 it can be changed once or less during a fast page mode cycle (tPC).

5) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6) AC measurements assume tT = 5 ns.

7) VIH (min.) and VIL (max.) are reference levels for measuring timing of input signals. Transition times are also measured between VIH and VIL.

8) Measured with a load equivalent to 100 pF and at Voh=2.0 V (Ioh = -2mA) , Vol=0.8V (Iol=2mA).

9) Operation within the tRCD (max.) limit ensures that tRAC (max.) can be met. tRCD (max.) is specified as a reference point only: If tRCD is greater than the specified tRCD (max.) limit, then access time is controlled by tCAC.

10) Operation within the tRAD (max.) limit ensures that tRAC (max.) can be met. tRAD (max.) is specified as a reference point only: If tRAD is greater than the specified tRAD (max.) limit, then access time is controlled by tAA.

11) Either tRCH or tRRH must be satisfied for a read cycle.

12) tOFF (max.) and tOEZ (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.

13) Either tDZC or tDZO must be satisfied.

14) Either tCDD or tODD must be satisfied.

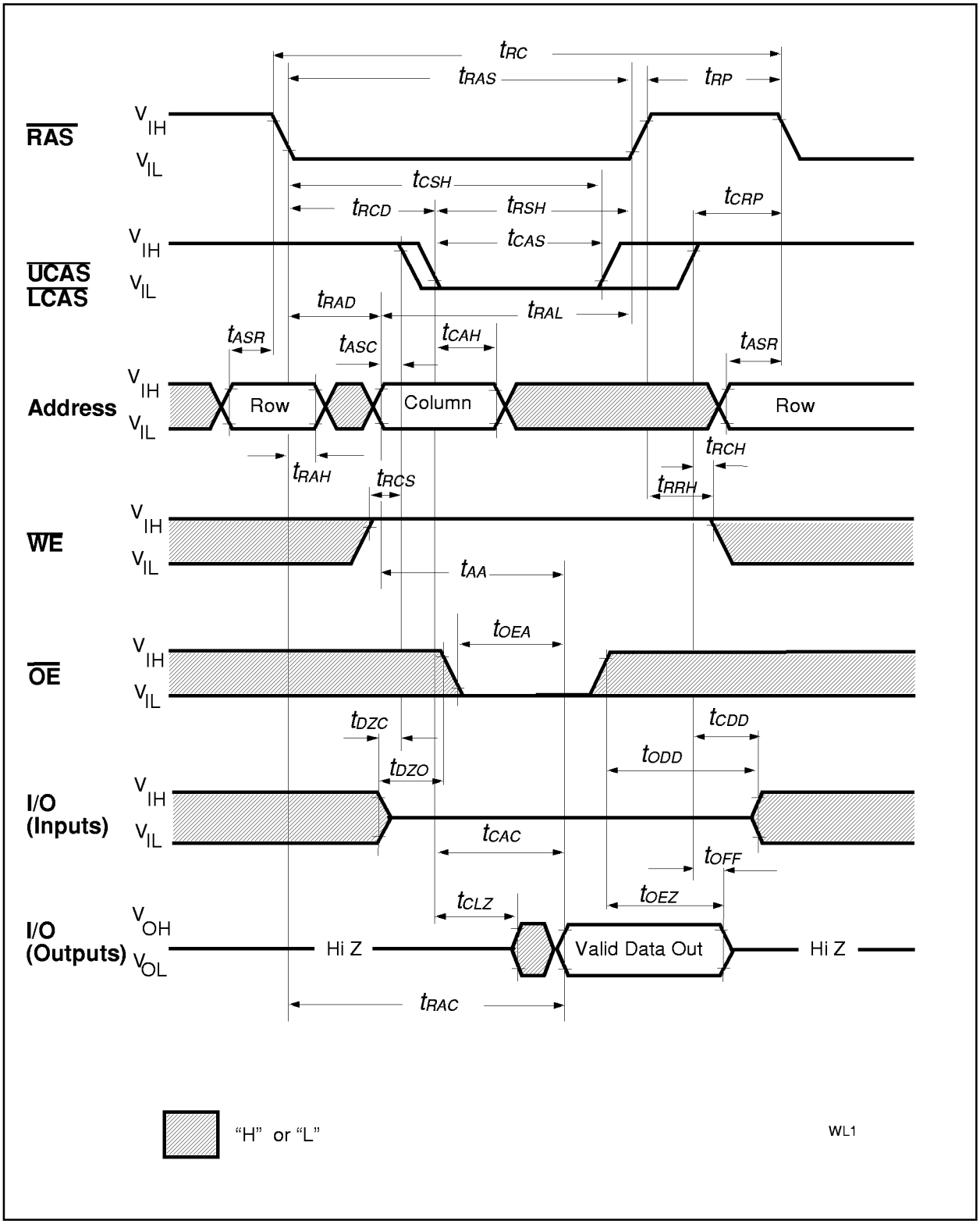
15) tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS > tWCS (min.), the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if tRWD > tRWD (min.), tCWD > tCWD (min.), tAWD > tAWD (min.) and tCPWD > tCPWD (min.) , the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.

16) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.

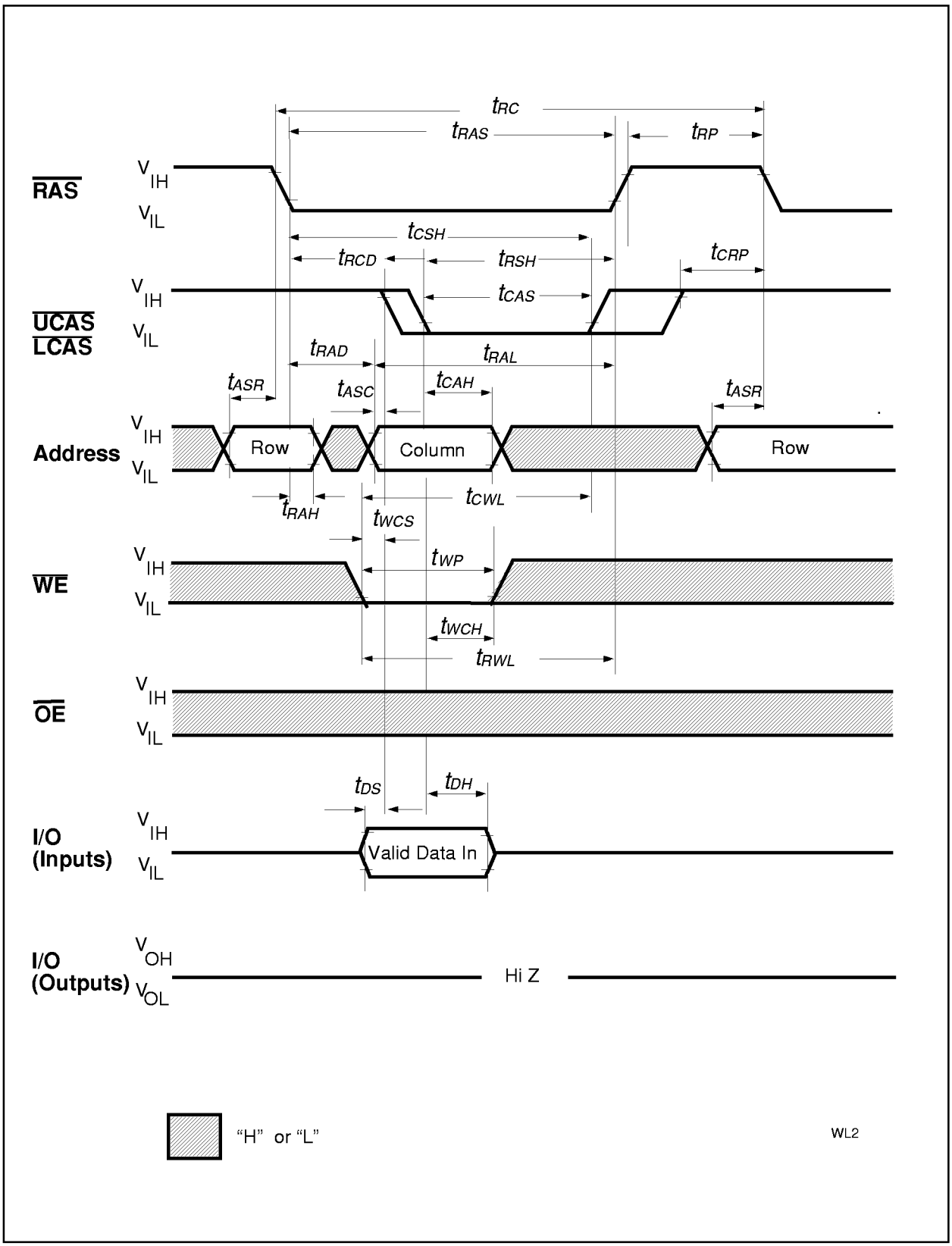
17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

    If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

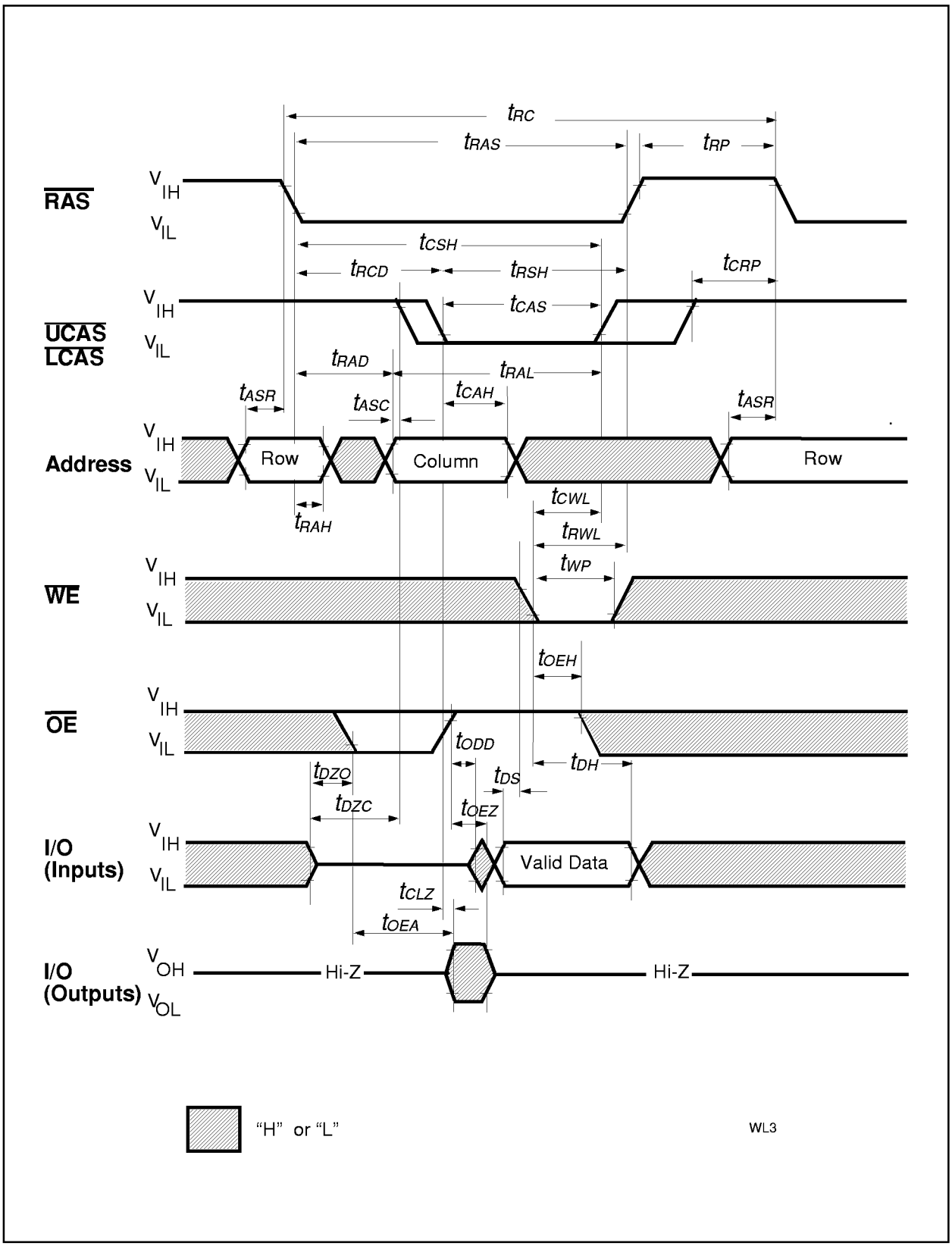
    If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
tCAS
UCAS
LCAS
tRAD
tRAL
tASR
tASC
tCAH
tASR
Address
Row
Column
Row
tRCH
tRAH
tRCS
tRRH
WE
tAA
tOEA
OE
tDZC
tCDD
tDZO
tODD
I/O
(Inputs)
tCAC
tOFF
tOEZ
tCLZ
I/O
(Outputs)
VOH
VOL
Hi Z
Valid Data Out
Hi Z
tRAC
"H" or "L"
WL1

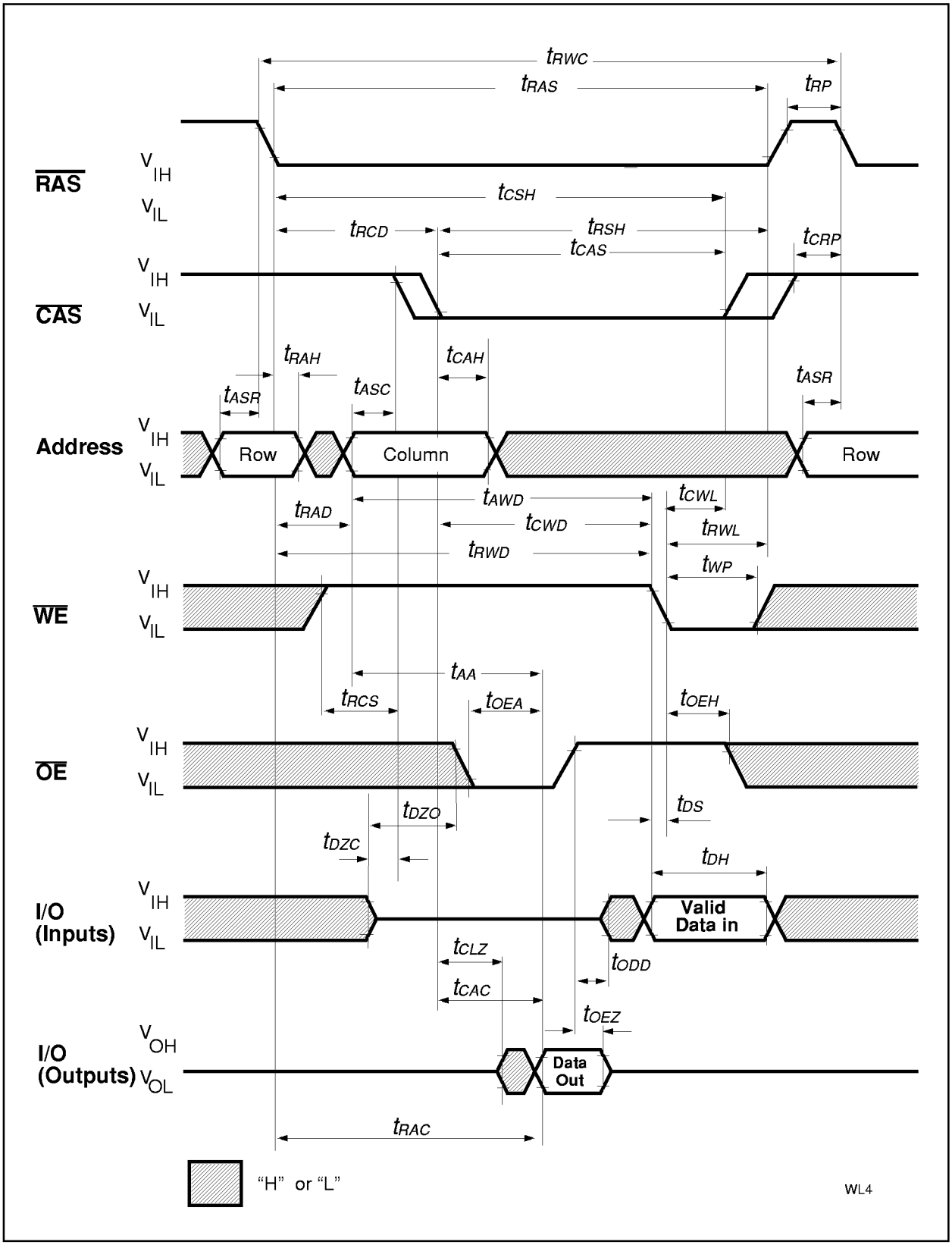
Read Cycle



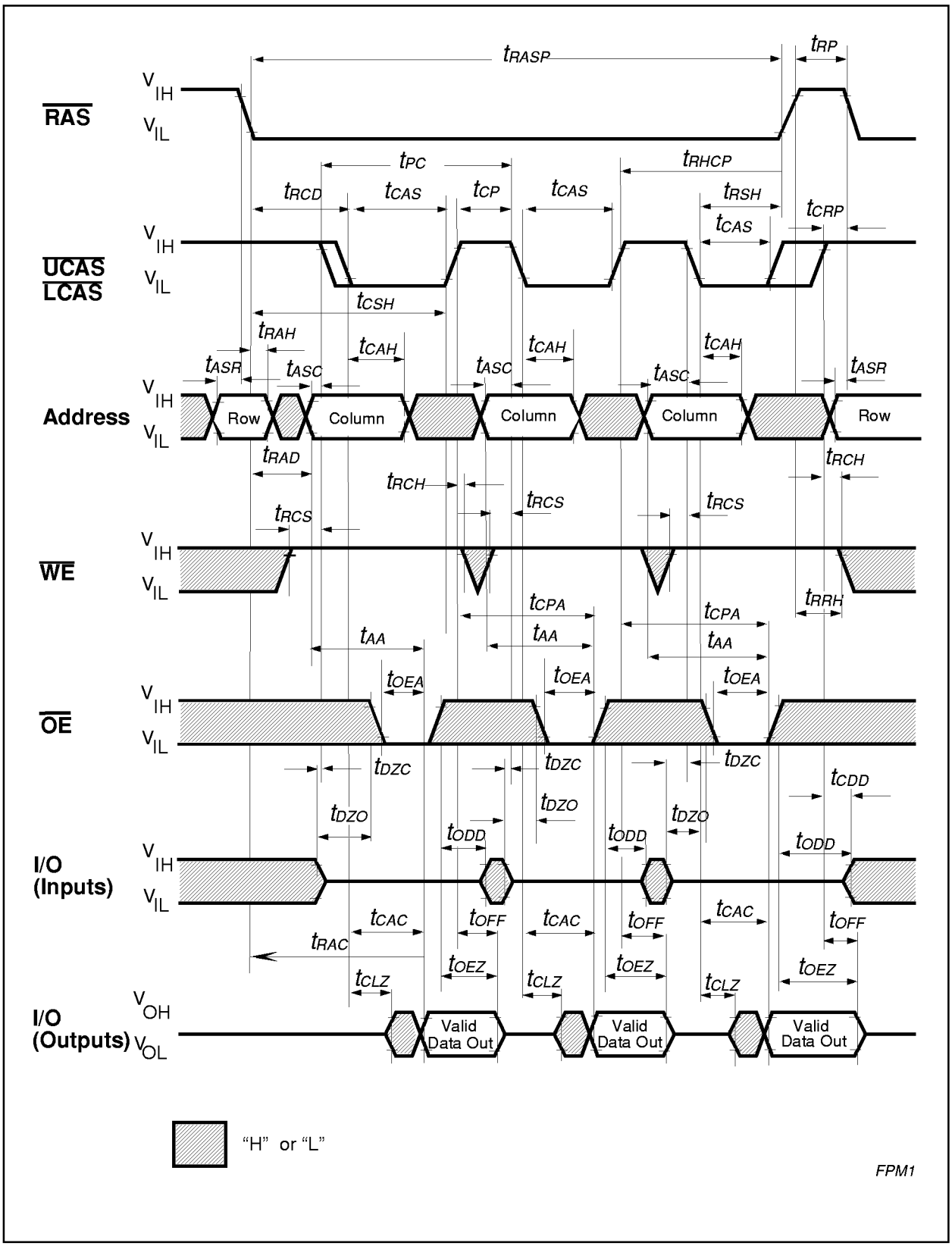
Write Cycle (Early Write)



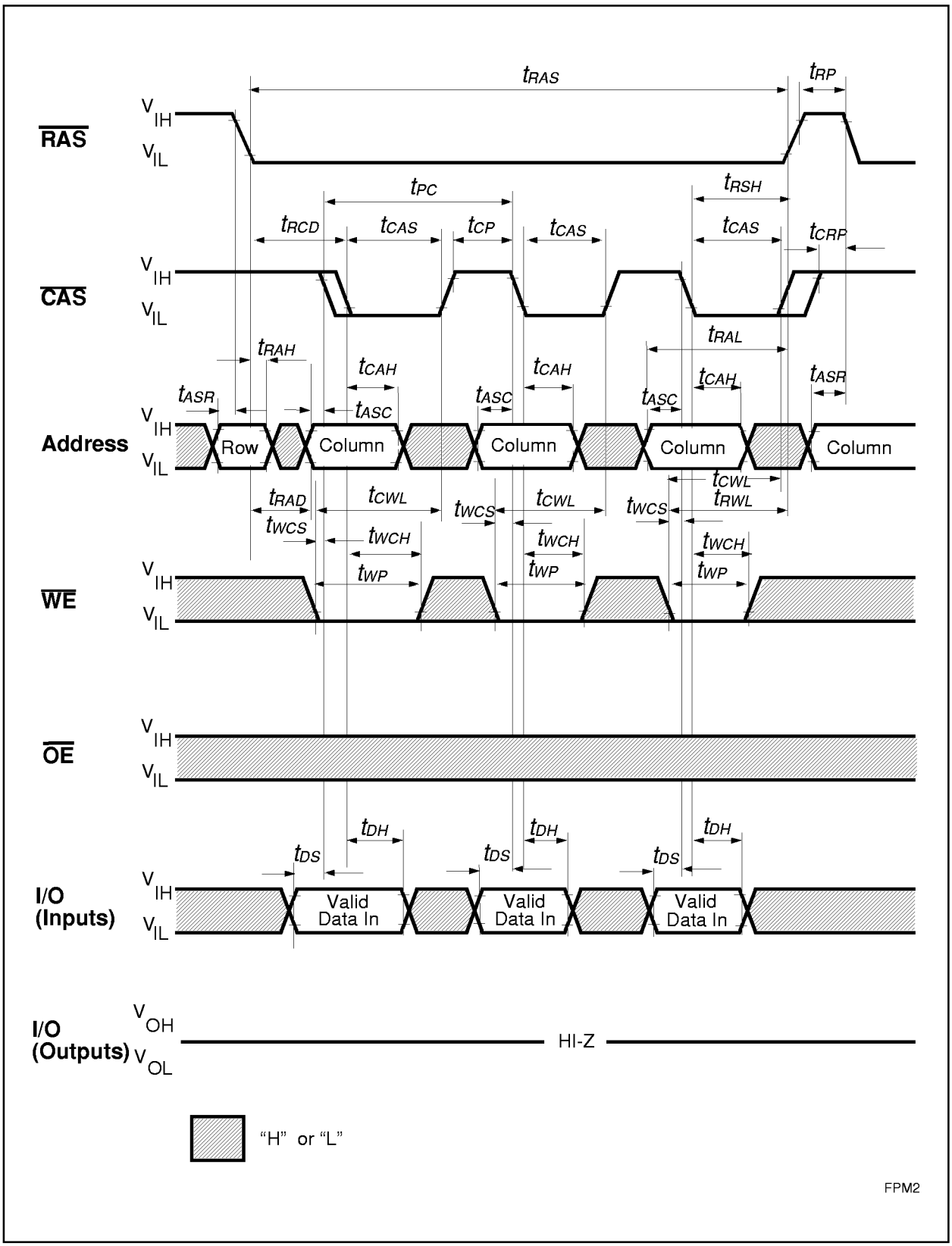
Write Cycle ($\overline{OE}$ Controlled Write)



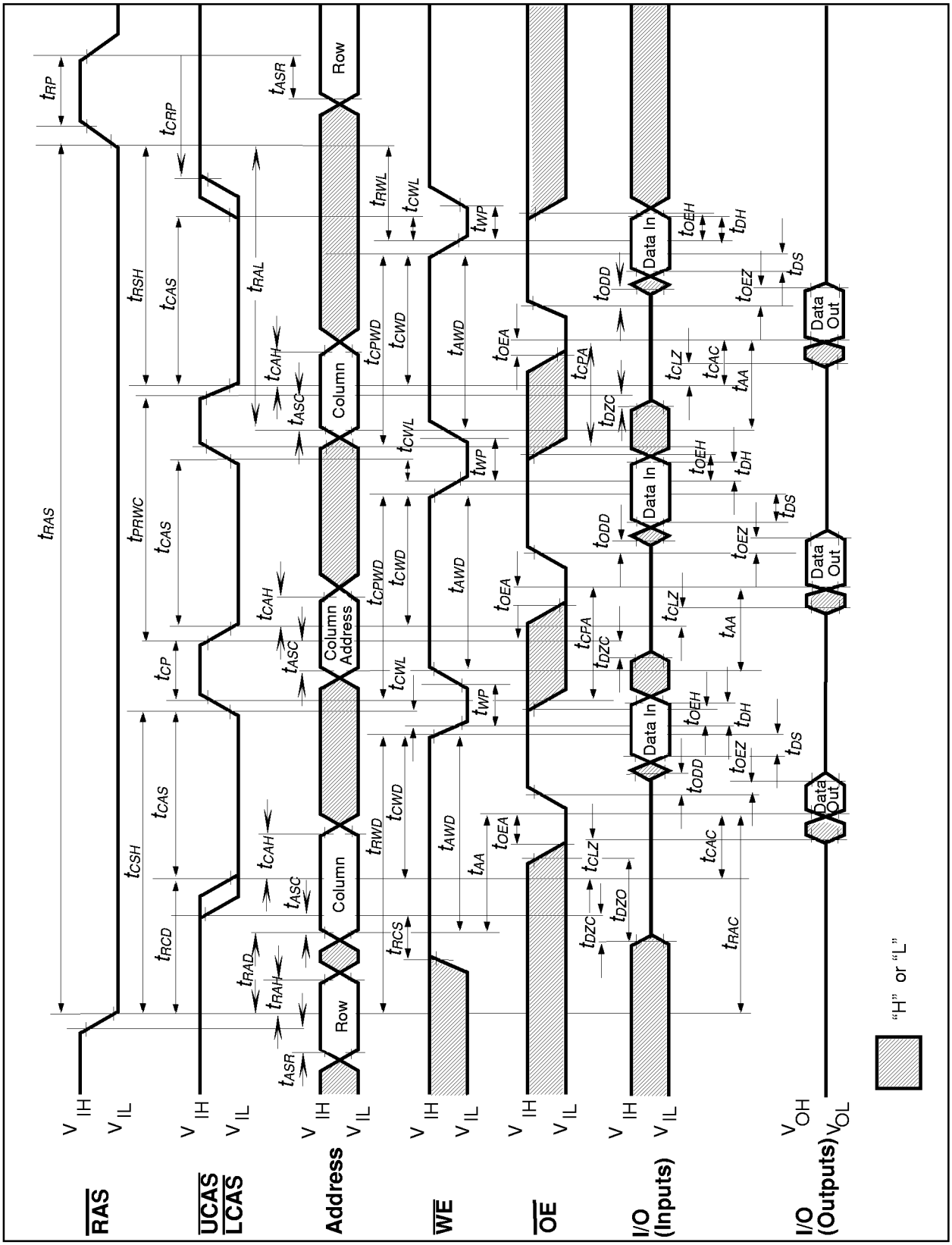
Read-Write (Read-Modify-Write) Cycle



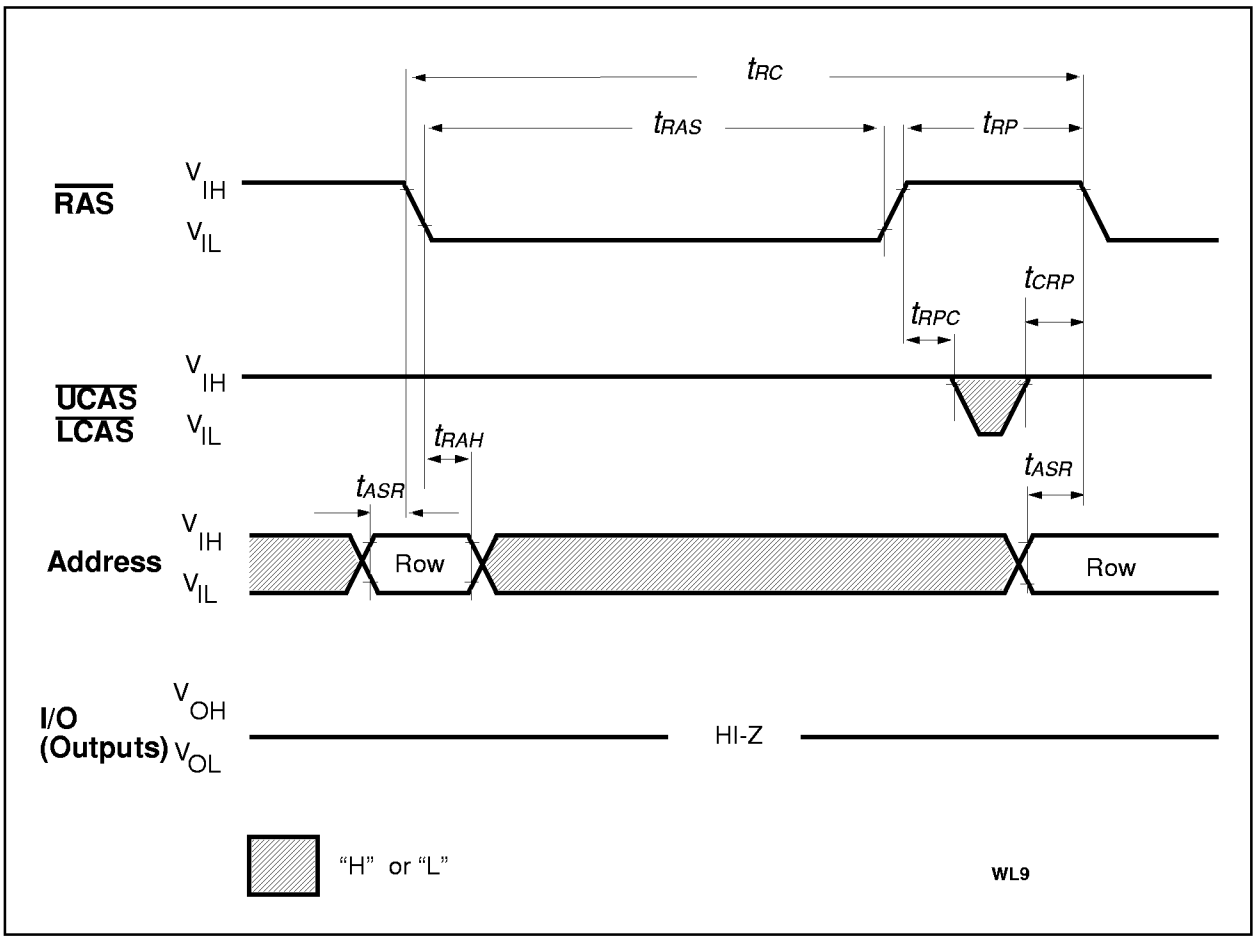
Fast Page Mode Read Cycle



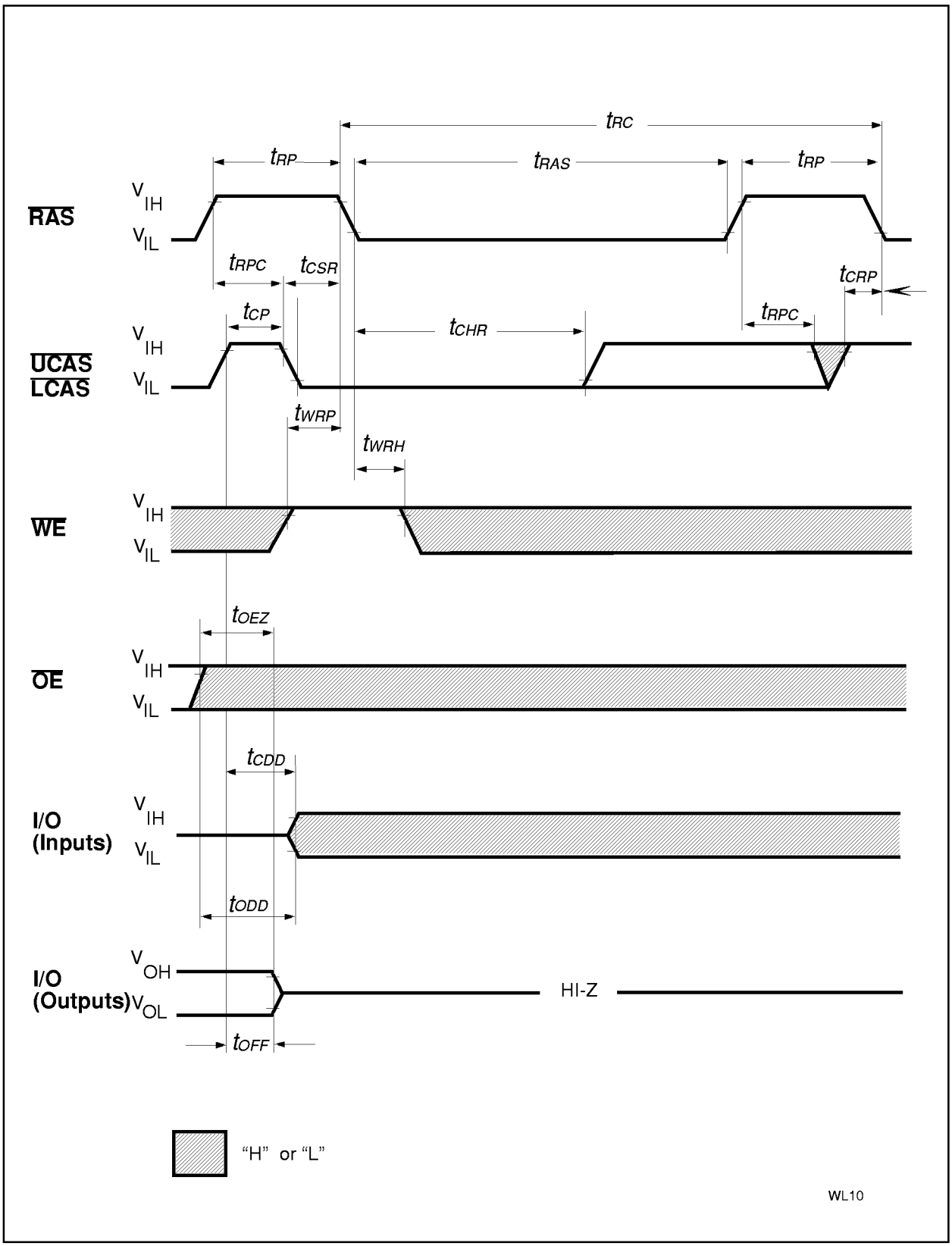
Fast Page Mode Early Write Cycle



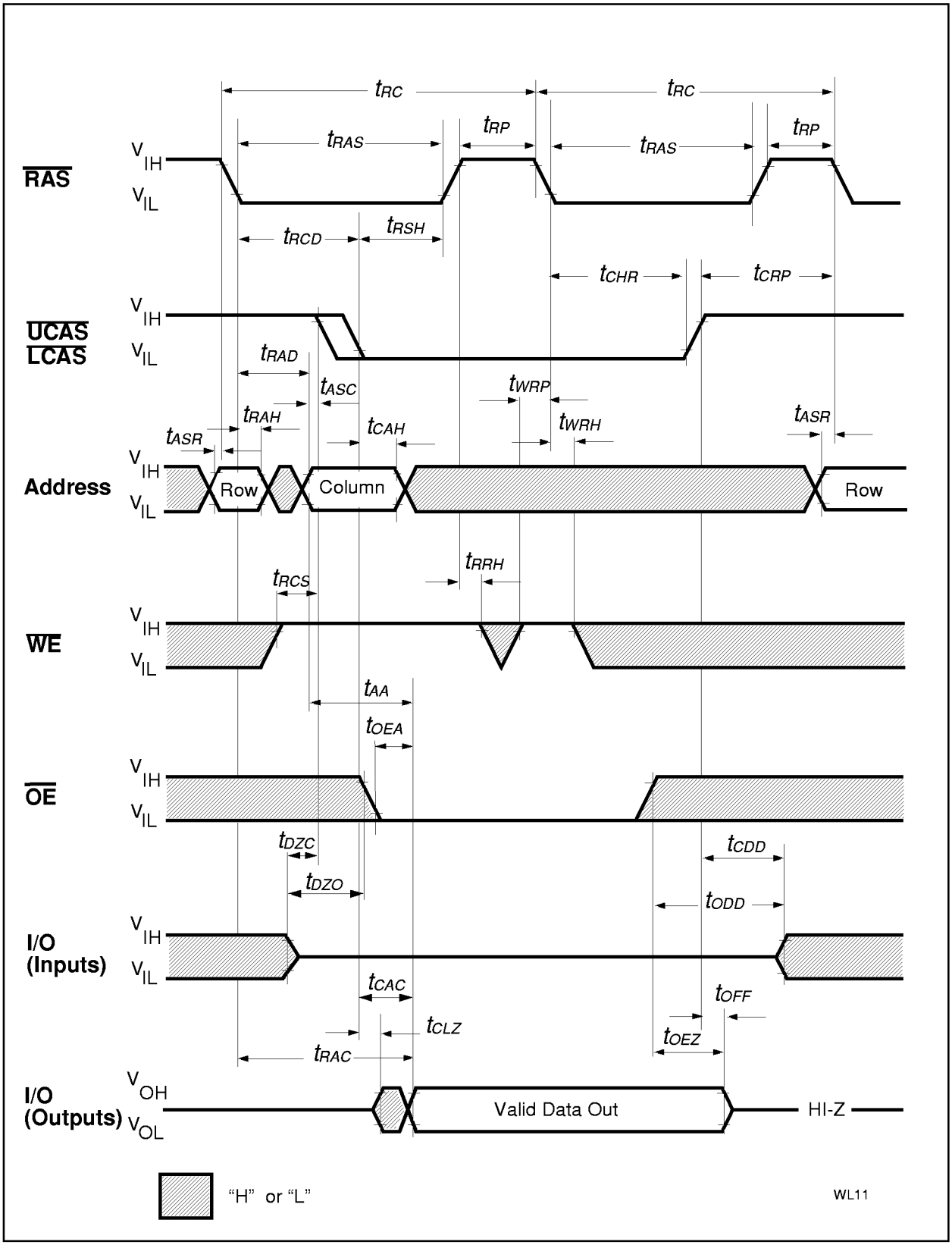
Fast Page Mode Late Write and Read-Modify Write Cycle



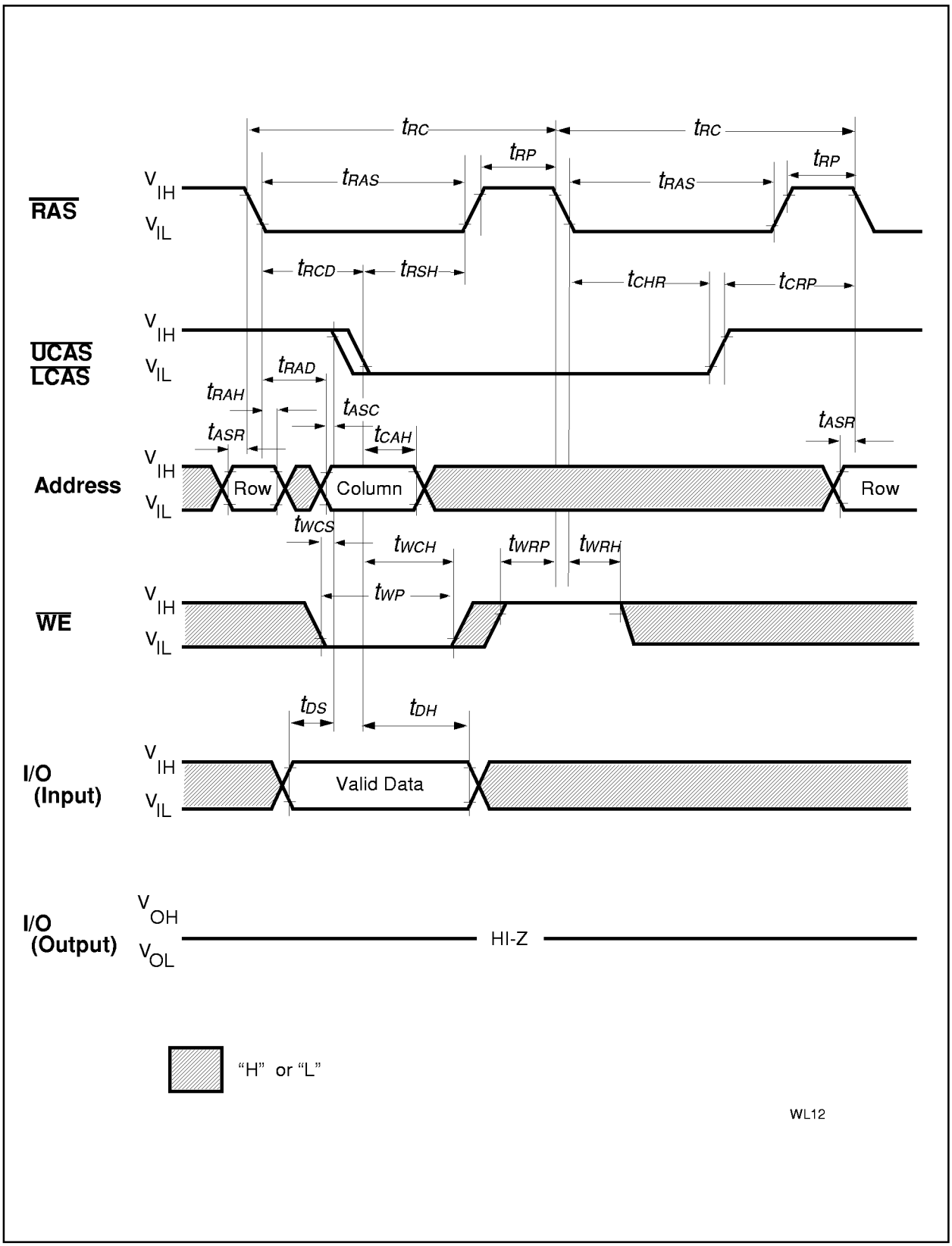
RAS-Only Refresh Cycle



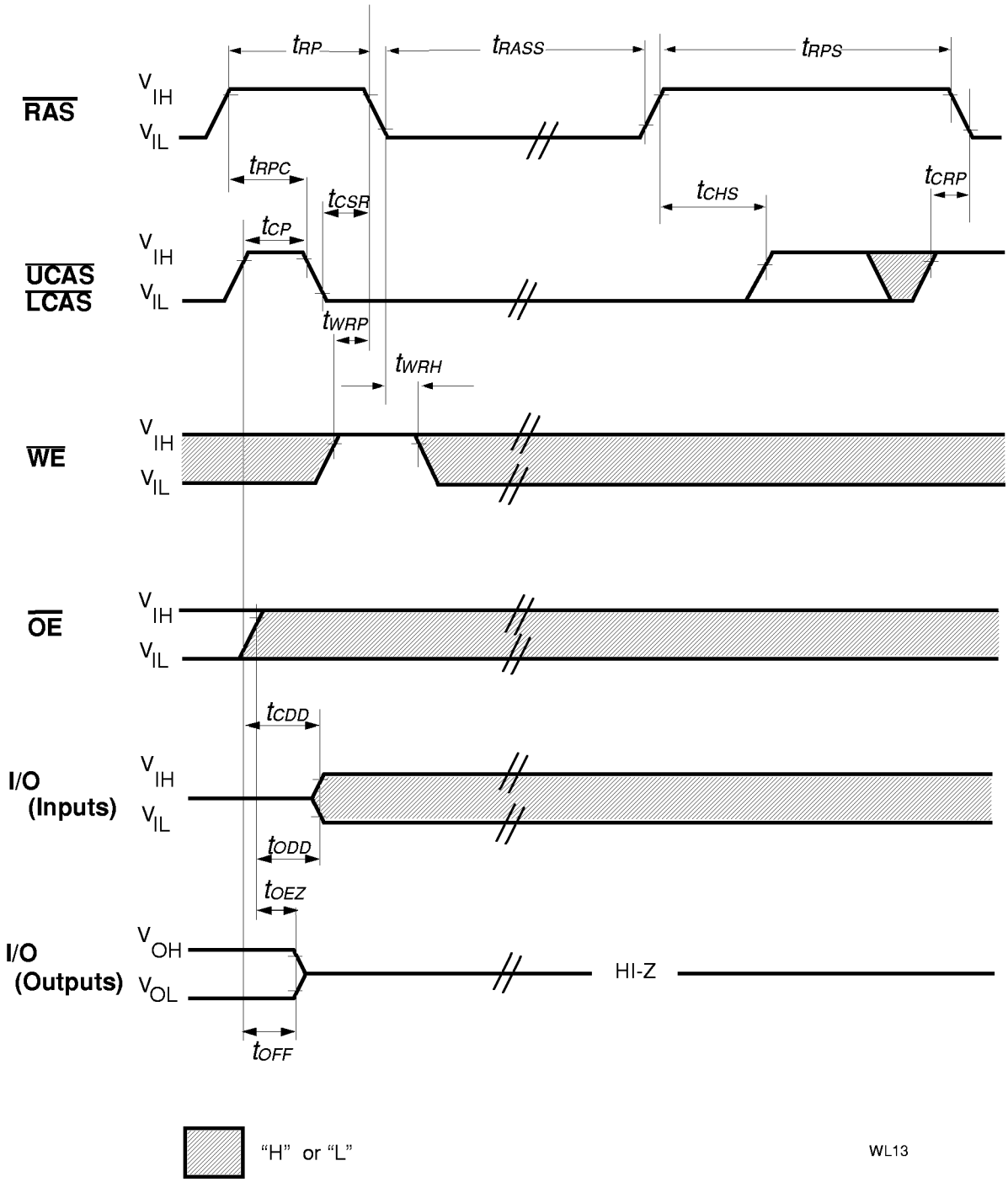
CAS-Before-RAS Refresh Cycle



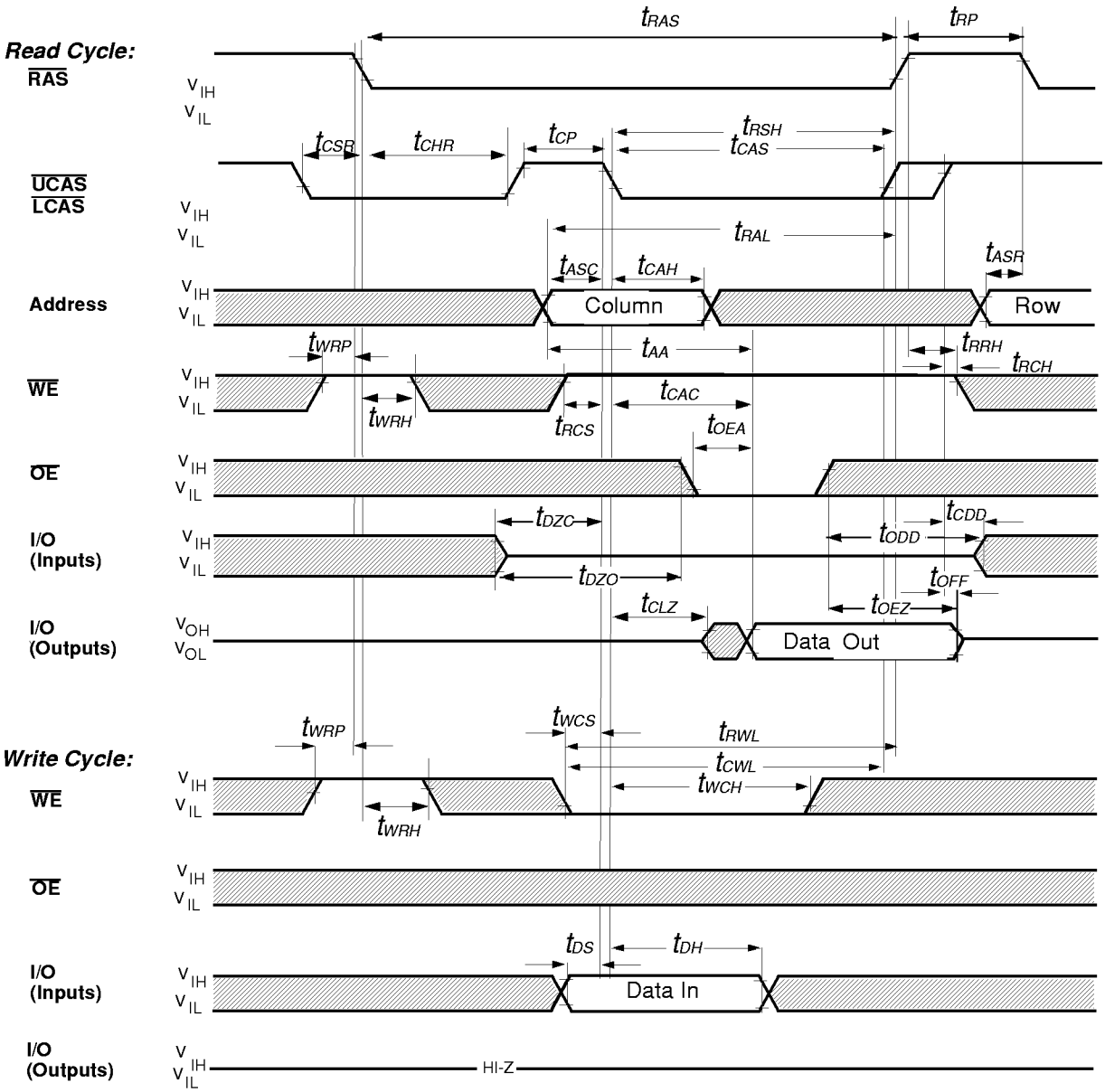
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Early Write)



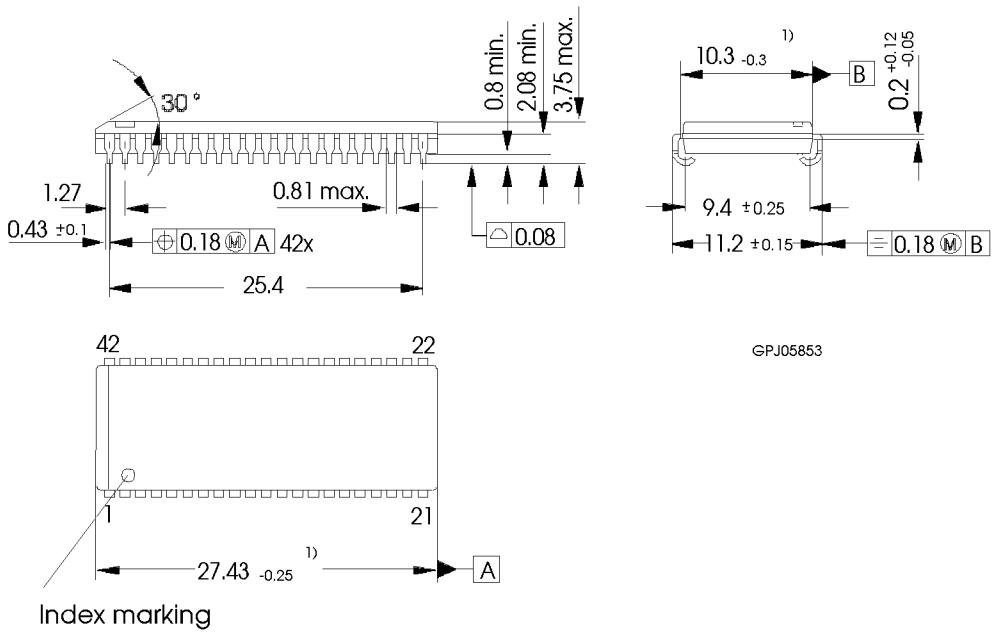
CAS before RAS Self Refresh Cycle



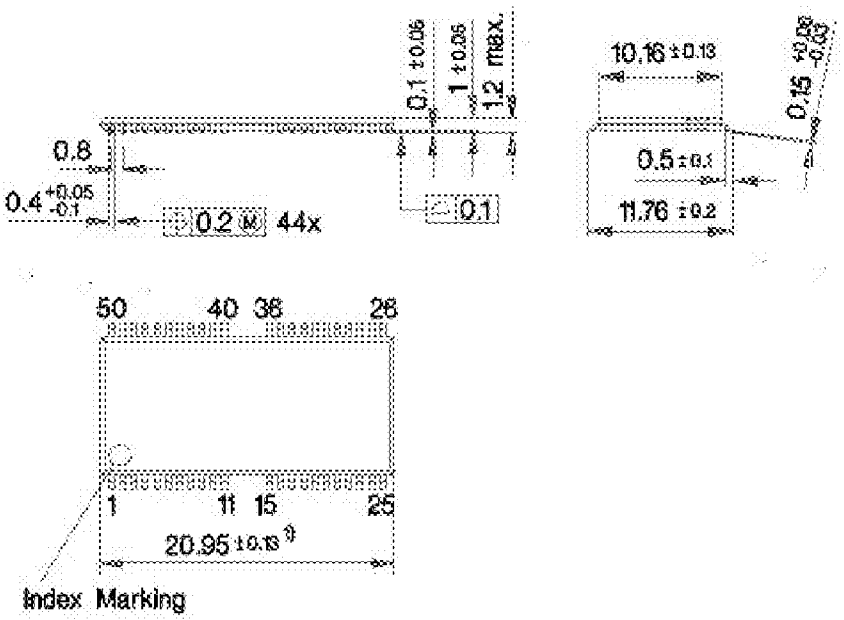
CAS-Before-RAS Refresh Counter Test Cycle

Package Outlines:

Plastic Package P-SOJ-42 (400mil)
(Small Outline J-leaded Package)



Plastic Package P-TSOPII-50/44 (400mil)
(Thin Small Outline Package, SMD)



1) Does not include plastic or metal protrusion of 0.25 max. per side