

RADIATION HARDENED POWER MOSFET THRU-HOLE (TO-204AA/AE)

IRH7250SE 200V, N-CHANNEL RAD Hard™ HEXFET® TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	ID
IRH7250SE	100K Rads (Si)	0.10Ω	26A



International Rectifier's RADHard™ HEXFET® MOSFET technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features:

- Single Event Effect (SEE) Hardened
- Ultra Low RDS(on)
- Low Total Gate Charge
- Proton Tolerant
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Light Weight

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
ID @ VGS = 12V, TC = 25°C	Continuous Drain Current	26	A
ID @ VGS = 12V, TC = 100°C	Continuous Drain Current	16	
IDM	Pulsed Drain Current ①	104	
PD @ TC = 25°C	Max. Power Dissipation	150	W
	Linear Derating Factor	1.2	W/°C
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy ②	500	mJ
IAR	Avalanche Current ①	26	A
EAR	Repetitive Avalanche Energy ①	15	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.9	V/ns
TJ	Operating Junction	-55 to 150	°C
TSTG	Storage Temperature Range		
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10 sec.)	
	Weight	11.5 (Typical)	g

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BVDSS	Drain-to-Source Breakdown Voltage	200	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBVDSS/ΔT _J	Temperature Coefficient of Breakdown Voltage	—	0.26	—	V/°C	Reference to 25°C, I _D = 1.0mA
RDS(on)	Static Drain-to-Source On-State Resistance	—	—	0.10	Ω	V _{GS} = 12V, I _D = 16A ④
		—	—	0.105		V _{GS} = 12V, I _D = 26A
VGS(th)	Gate Threshold Voltage	2.5	—	4.5	V	V _{DS} = V _{GS} , I _D = 1.0mA
gfs	Forward Transconductance	7.5	—	—	S (τ)	V _{DS} > 15V, I _{DS} = 16A ④
IDSS	Zero Gate Voltage Drain Current	—	—	25	μA	V _{DS} = 160V, V _{GS} = 0V
		—	—	250		V _{DS} = 160V, V _{GS} = 0V, T _J = 125°C
IGSS	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
IGSS	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Qg	Total Gate Charge	—	—	180	nC	V _{GS} = 12V, I _D = 26A V _{DS} = 100V
Qgs	Gate-to-Source Charge	—	—	35		
Qgd	Gate-to-Drain ('Miller') Charge	—	—	83		
td(on)	Turn-On Delay Time	—	—	33	ns	V _{DD} = 100V, I _D = 26A, V _{GS} = 12V, R _G = 2.35Ω
tr	Rise Time	—	—	140		
td(off)	Turn-Off Delay Time	—	—	140		
tf	Fall Time	—	—	140		
LS + LD	Total Inductance	—	10	—	nH	Measured from drain lead (6mm/0.25in. from package) to source lead (6mm/0.25in. from package)
Ciss	Input Capacitance	—	3100	—	pF	V _{GS} = 0V, V _{DS} = 25V f = 1.0MHz
Coss	Output Capacitance	—	990	—		
Crss	Reverse Transfer Capacitance	—	380	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
IS	Continuous Source Current (Body Diode)	—	—	26	A	
ISM	Pulse Source Current (Body Diode) ①	—	—	104		
VSD	Diode Forward Voltage	—	—	1.9	V	T _J = 25°C, I _S = 26A, V _{GS} = 0V ④
trr	Reverse Recovery Time	—	—	550	nS	T _J = 25°C, I _F = 26A, di/dt ≤ 100A/μs
QRR	Reverse Recovery Charge	—	—	8.8	μC	V _{DD} ≤ 50V ④
ton	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by LS + LD.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
RthJC	Junction-to-Case	—	—	0.83	°C/W	Typical socket mount
RthCS	Case-to-Sink	—	0.12	—		
RthJA	Junction-to-Ambient	—	—	30		

Note: Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	100K Rads (Si)		Units	Test Conditions ⑧
		Min	Max		
BVDSS	Drain-to-Source Breakdown Voltage	200	—	V	V _{GS} = 0V, I _D = 1.0mA
V _{GS(th)}	Gate Threshold Voltage	2.0	4.5		V _{GS} = V _{DS} , I _D = 1.0mA
I _{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	-100		V _{GS} = -20V
I _{DSS}	Zero Gate Voltage Drain Current	—	50	μA	V _{DS} = 160V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance	—	0.10	Ω	V _{GS} = 12V, I _D = 16A
V _{SD}	Diode Forward Voltage ④	—	1.9	V	V _{GS} = 0V, I _D = 26A

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET MeV/(mg/cm ²)	Energy (MeV)	Range (μm)	V _{DS} (V)				
				@V _{GS} =0V	@V _{GS} =-5V	@V _{GS} =-10V	@V _{GS} =-15V	@V _{GS} =-20V
Cu	28	285	43	200	200	200	200	200
Br	36.8	305	39	200	200	200	180	140

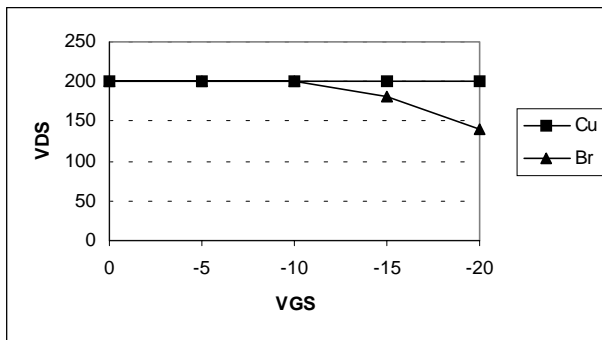


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

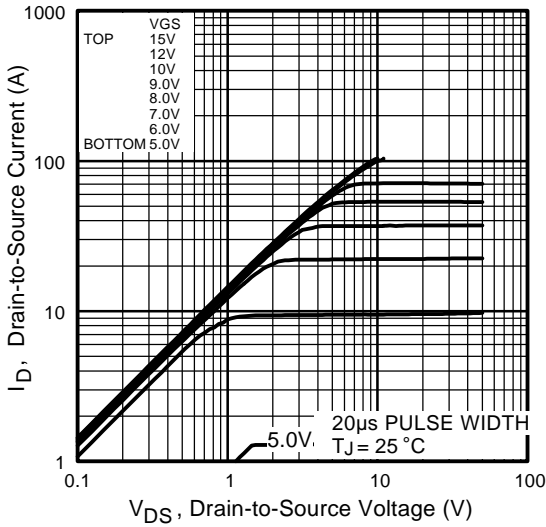


Fig 1. Typical Output Characteristics

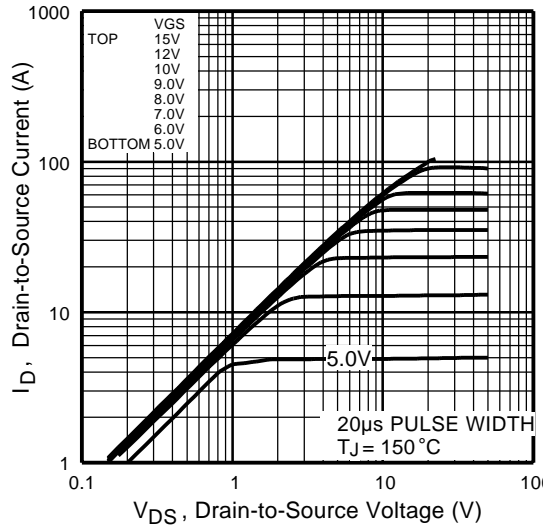


Fig 2. Typical Output Characteristics

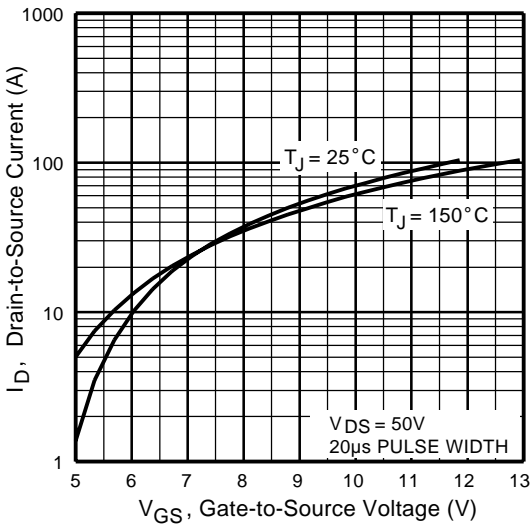


Fig 3. Typical Transfer Characteristics

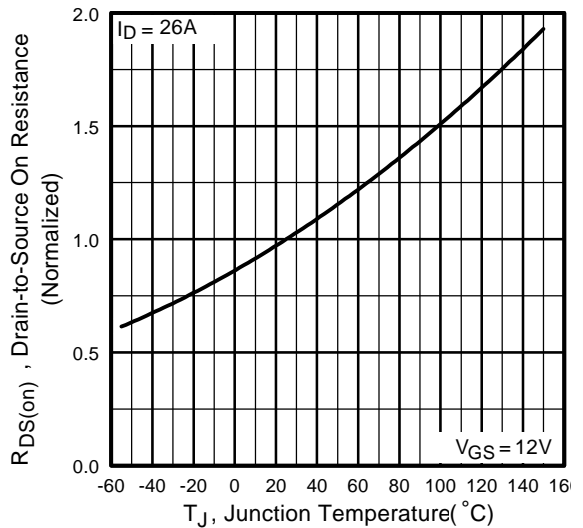


Fig 4. Normalized On-Resistance Vs. Temperature

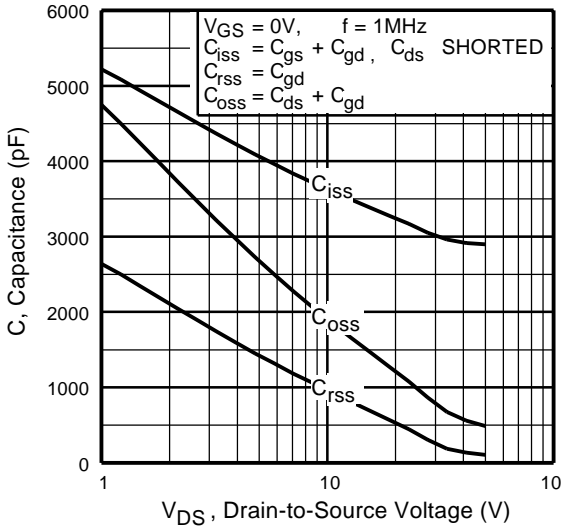


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

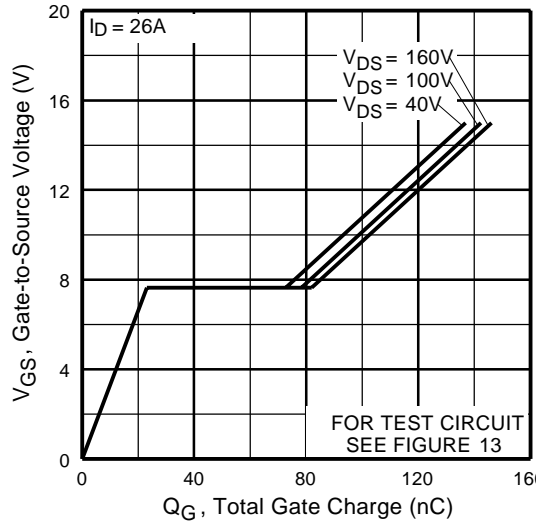


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

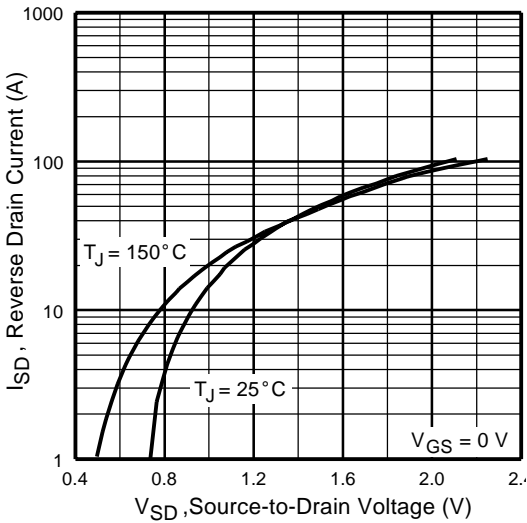


Fig 7. Typical Source-Drain Diode Forward Voltage

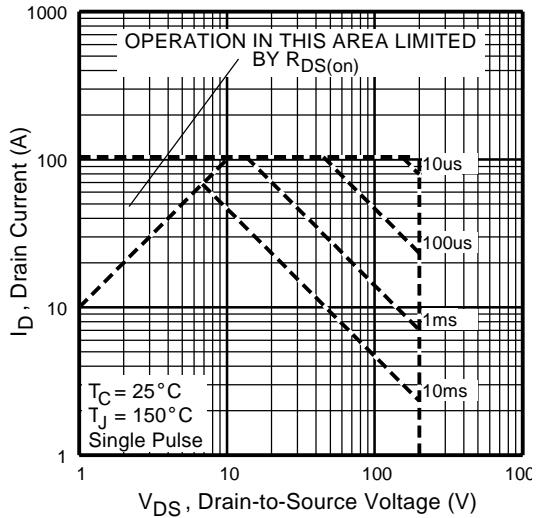


Fig 8. Maximum Safe Operating Area

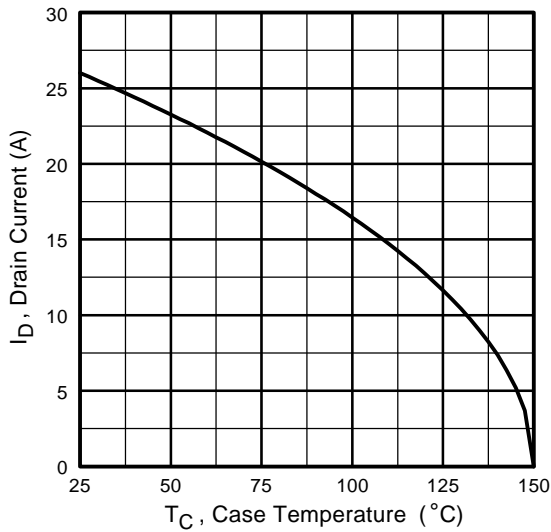


Fig 9. Maximum Drain Current Vs. Case Temperature

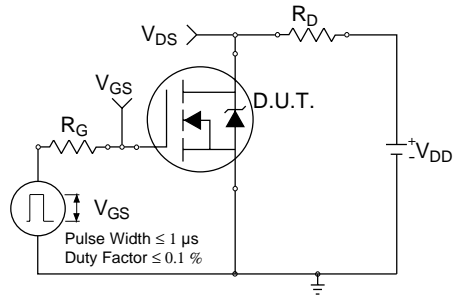


Fig 10a. Switching Time Test Circuit

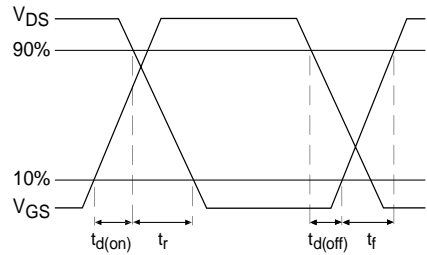


Fig 10b. Switching Time Waveforms

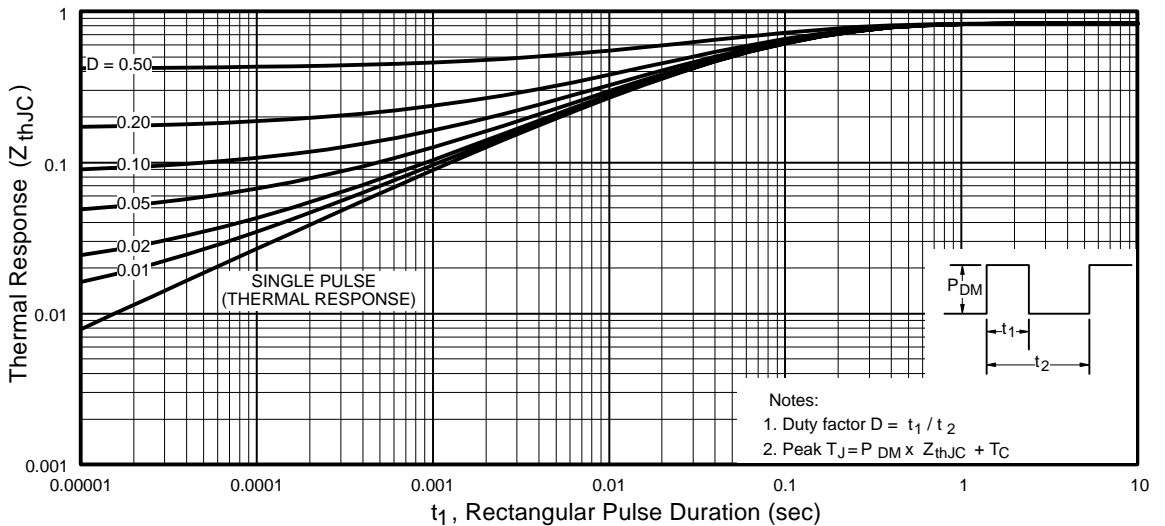


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

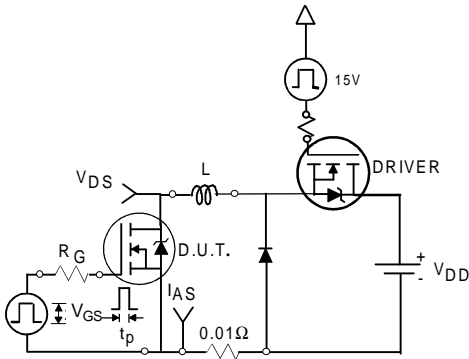


Fig 12a. Unclamped Inductive Test Circuit

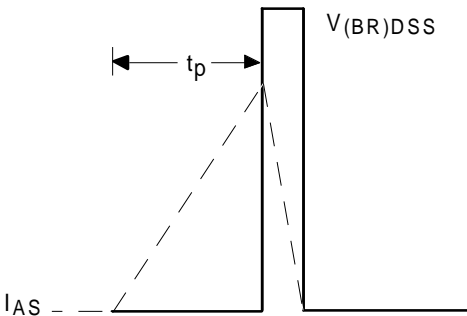


Fig 12b. Unclamped Inductive Waveforms

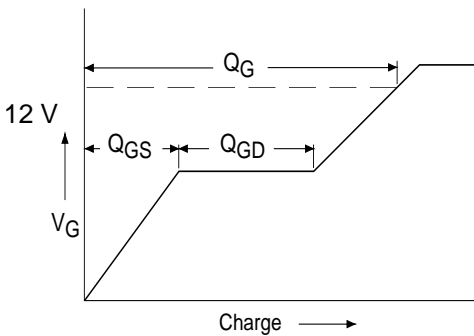


Fig 13a. Basic Gate Charge Waveform

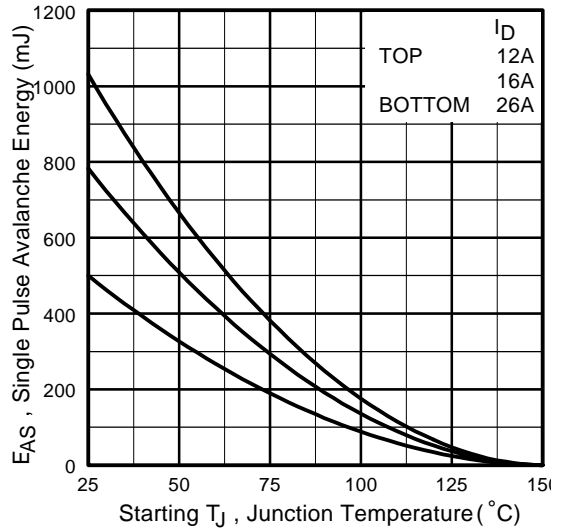


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

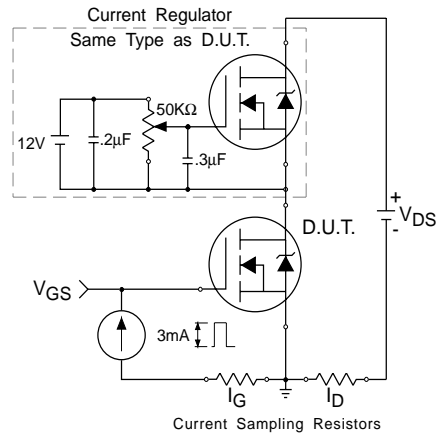
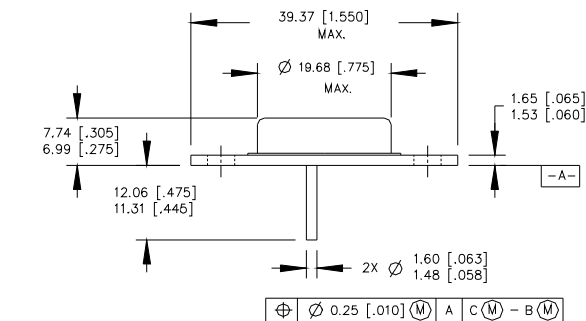


Fig 13b. Gate Charge Test Circuit

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 50V$, starting $T_J = 25^\circ C$, $L = 1.5\text{ mH}$
Peak $I_L = 26A$, $V_{GS} = 12V$
- ③ $I_{SD} \leq 26A$, $di/dt \leq 400A/\mu s$,
 $V_{DD} \leq 200V$, $T_J \leq 150^\circ C$
- ④ Pulse width $\leq 300\ \mu s$; Duty Cycle $\leq 2\%$
- ⑤ **Total Dose Irradiation with V_{GS} Bias.**
12 volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.
- ⑥ **Total Dose Irradiation with V_{DS} Bias.**
160volt V_{DS} applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions —TO-204AE (Modified TO-3)

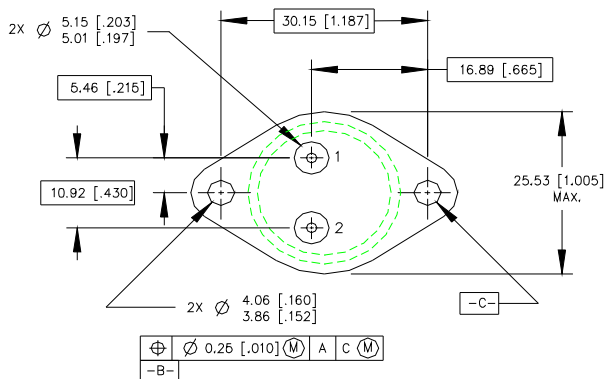


PIN ASSIGNMENTS

- 1 - SOURCE
- 2 - GATE
- 3 - DRAIN (CASE)

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.6M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-204AE.



International
IR Rectifier

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