Am99C88/Am99CL88

8K x 8 CMOS Static Random-Access Memory

DISTINCTIVE CHARACTERISTICS

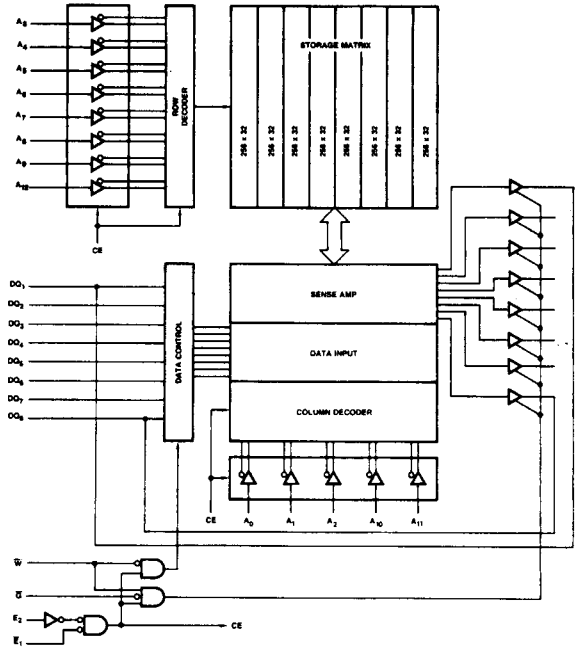
- High speed – access times 70/100/120/150 ns
- Low-power requirements:
  - Am99C88
    - Operating: 330 mW Max.
    - Standy: 16.5 mW Max.
  - Am99CL88
    - Operating: 220 mW Max.
    - Standby: 550 μW Max.
- Battery backed-up operation (2 V data retention)
- Fully static storage and interface (no clocks or timing signals required)
- TTL compatible interface levels
- Industry standard package (28-pin 0.6 in dual-in-line)
- Two chip enables ($\overline{E_1}$ and E_2) for ease of expansion and automatic power down
- Pin compatible with 2764 type programmable ROM

GENERAL DESCRIPTION

The Am99C88/Am99CL88 is a high-performance, low power CMOS static RAM organized as 8192 words of 8 bits each. In addition to 13 address inputs and 8 common data inputs and outputs, the device utilizes 4 control pins. Two of them, $\overline{E_1}$ and E_2, perform chip enable functions and automatically power down the device when proper polarity of logic levels are applied. The other control pins, $\overline{G}$ and $\overline{W}$, facilitate read and write operations, respectively. These control inputs, along with three-state data inputs/outputs, allow similar devices to be connected to a common bus.

The data read out is non-destructive and has the same polarity as the data stored. The data is retained by the device even at V_{DD} as low as 2 V. Am99C88/Am99CL88 requires a single 5 V power supply and dissipates 330 mW/220 mW maximum in operating mode and 16.5 mW/550 μW maximum in standby mode. The devices are packaged in industry-standard, 28-pin, 0.6-inch wide dual-in-line packages.

BLOCK DIAGRAM



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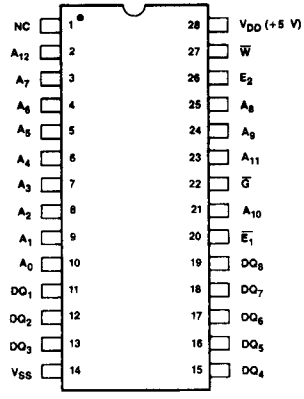
PRODUCT SELECTOR GUIDE

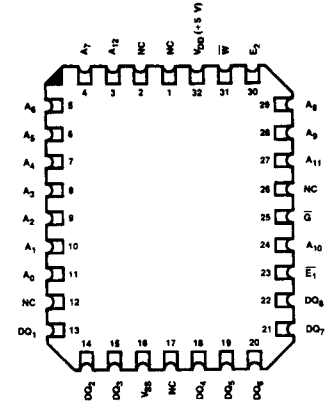
		Am99CS88					Am99C88					Am99CL88			
		-70	-10	-12	-15	-20	-70	-10	-12	-15	-20	-70	-10	-12	-15
Access Time Max (ns)		70	100	120	150	200	70	100	120	150	200	70	100	120	150
0 to 70°C	I_{DD1} Max (mA)	–	–	–	–	–	60	60	60	60	–	40	40	40	40
	I_{SB} Max (mA)	–	–	–	–	–	5	5	5	5	–	1	1	1	1
	$I_{SB1,2}$ Max (μA)	–	–	–	–	–	3000	3000	3000	3000	–	100	100	100	100
	I_{DDR} 2 V (μA)	–	–	–	–	–	1000	1000	1000	1000	–	50	50	50	50
−55 to +125°C	I_{DD1} Max. (mA)	60	60	60	60	60	60	60	60	60	60	–	–	–	–
	I_{SB} Max. (mA)	10	10	10	10	10	5	5	5	5	5	–	–	–	–
	$I_{SB1,2}$ Max. (μA)	10000	10000	10000	10000	10000	5000	5000	5000	5000	5000	–	–	–	–
	I_{DDR} 2 V (μA)	5000	5000	5000	5000	5000	1000	1000	1000	1000	1000	–	–	–	–

CONNECTION DIAGRAMS

Top View



CD009132



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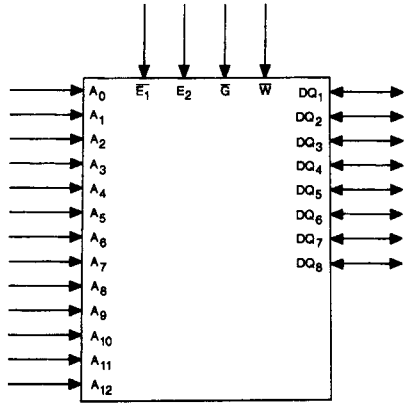
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



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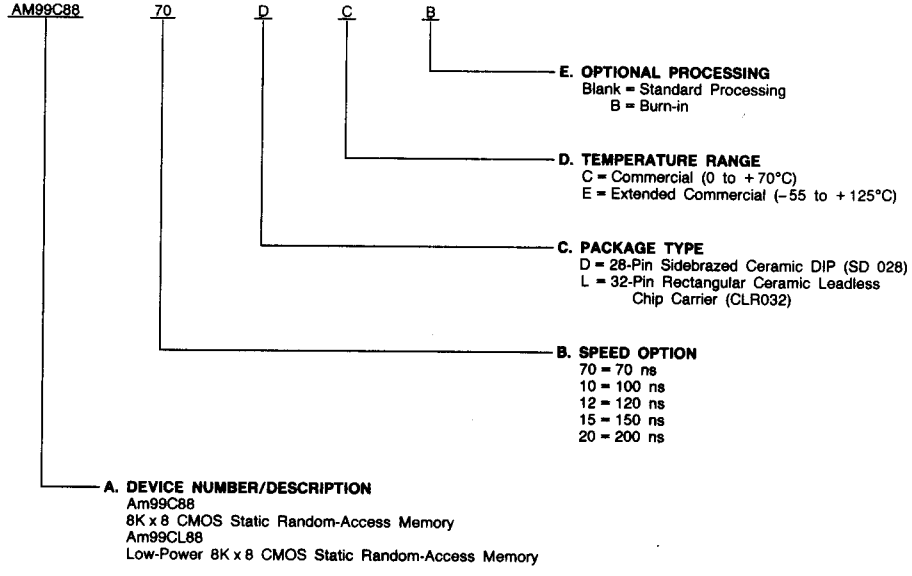
ADDRESS DESIGNATORS

External	Internal	Pin Number DIP Package
A_9	AX_0	24
A_3	AX_1	7
A_4	AX_2	6
A_5	AX_3	5
A_6	AX_4	4
A_7	AX_5	3
A_{12}	AX_6	2
A_8	AX_7	25
A_{11}	AY_0	23
A_{10}	AY_1	21
A_0	AY_2	10
A_1	AY_3	9
A_2	AY_4	8

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM99C88-70 AM99C88-10 AM99C88-12 AM99C88-15	DC, DCB, LC, LCB DE, DEB, LE, LEB
AM99C88-20	DE, DEB, LE, LEB
AM99CL88-70 AM99CL88-10 AM99CL88-12 AM99CL88-15	DC, DCB, LC, LCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

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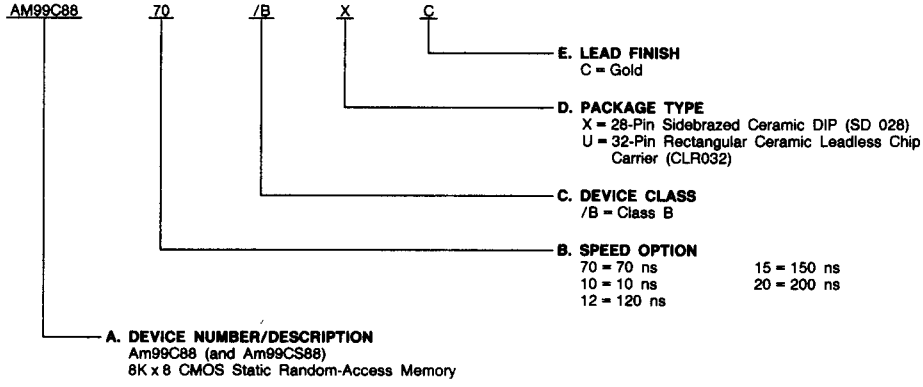
ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM99CS88-70	/BXC, /BUC
AM99CS88-10	
AM99CS88-12	
AM99CS88-15	
AM99CS88-20	
AM99C88-70	/BXC, /BUC
AM99C88-10	
AM99C88-12	
AM99C88-15	
Am99C88-20	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{12}$ Address (Inputs)
The 13 address inputs select one of the 8192 8-bit words in the RAM.

$\overline{E_1}$ Chip Enable1 (Input)

E_2 Chip Enable2 (Input)
$\overline{E_1}$ is active LOW and E_2 is active HIGH. The device can be accessed only when both Chip Enables are active. If either Chip Enable is not active, the device is deselected and will be in a standby power mode. The DQ port will be in a high-impedance state.

$\overline{W}$ Write Enable (Input)
$\overline{W}$ controls read and write operations. When $\overline{W}$ is HIGH and $\overline{G}$ is LOW, data will be output at the DQ port. When $\overline{W}$ is LOW, data present on the DQ port will be written into the selected memory location.

$\overline{G}$ Output Enable (Input)
$\overline{G}$ controls the state of the outputs in conjunction with Chip Enable and $\overline{W}$.

$DQ_1 - DQ_8$ Data Input/Data Output Ports
Eight bidirectional ports used to write into or read data from the RAM.

V_{DD} Power Supply +5 Volts

V_{SS} Ground

FUNCTIONAL DESCRIPTION

Please refer to Table 1 for summary of Mode Select.

TABLE 1. MODE SELECT

$\overline{E_1}$	E_2	$\overline{W}$	$\overline{G}$	Output	Supply Current	Mode
H	X	X	X	Hi-Z	I_{SB}, I_{SB1}	Not Selected
X	L	X	X	Hi-Z	I_{SB}, I_{SB2}	Not Selected
L	H	H	H	Hi-Z	I_{DD}, I_{DD1}	Output Disabled
L	H	H	L	D_{OUT}	I_{DD}, I_{DD1}	Read
L	H	L	X	Hi-Z	I_{DD}, I_{DD1}	Write

H = HIGH
L = LOW
X = Don't Care

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... −0.5 to +7.0 V
All Signal Voltages ..... −0.5 to +7.0 V
DC Output Current ..... 20 mA
Power Dissipation
  Cerdip Packages ..... 1.0 W
  Plastic Packages ..... 1.0 W
Ambient Temperature with Power Applied
  Cerdip Packages ..... −55 to +125°C
  Plastic Packages ..... −10 to +85°C
Storage Temperature
  Cerdip Packages ..... −65 to +150°C
  Plastic Packages ..... −55 to +125°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 2)

Commercial (C) Devices
Supply Voltage ..... +4.5 to +5.5 V
Temperature ..... 0 to +70°C

Military (M) Devices*
Supply Voltage ..... +4.5 to +5.5 V
Temperature ..... −55 to +125°C

Operating ranges define those limits between which the functionality and parameters of the device are guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Am99CS88 Min.	Am99CS88 Max.	Am99C88 Min.	Am99C88 Max.	Am99CL88 Min.	Am99CL88 Max.	Units
I_{OH}	Output HIGH Current	V_{OH} = 2.4 V V_{DD} = 4.5 V		−2		−2		−2		mA
I_{OL}	Output LOW Current	V_{OL} = 0.4 V		4		4		4		mA
V_{IH}	Input HIGH Voltage			2.2	V_{DD} + 1.0	2.2	V_{DD} + 1.0	2.2	V_{DD} + 1.0	V
V_{IL}	Input LOW Voltage			−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	$GND \leq V_{IN} \leq V_{DD}$			2		2		2	μA
I_{OZ}	Output Leakage Current	$GND \leq V_{OUT} \leq V_{DD}$ $\overline{E_1} \geq V_{IH}$ or $E_2 \leq V_{IL}$ or $\overline{G} \geq V_{IH}$			2		2		2	μA
I_{DD}	Operating Supply Current	$\overline{E_1} \leq V_{IL}$ $E_2 \geq V_{IH}$ $I_{I/O}$ = 0 mA			60		60		40	mA
I_{DD1}	Average Operating Supply Current	Cycle = Min., Duty = 100% $\overline{E_1} \leq V_{IL}$, $E_2 \geq V_{IH}$, $I_{I/O}$ = 0 mA			60		60		40	mA
I_{SB}	Standby Power Supply Current	$\overline{E_1} = V_{IH}$ or $E_2 = V_{IL}$			10		5		1	mA
I_{SB1}		$\overline{E_1} \geq V_{DD} - 0.2$ V, $E_2 \geq V_{DD} - 0.2$ V or $E_2 \leq 0.2$ V	COM'L		–		3000		100	μA
			MIL		10000		5000		–	
I_{SB2}		$E_2 \leq 0.2$ V	COM'L		–		3000		100	μA
			MIL		10000		5000		–	

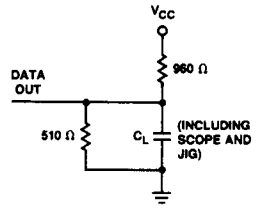
*See the last page of this spec for Group A Subgroup Testing information.

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions		Am99CS88 Min.	Am99CS88 Max.	Am99C88 Min.	Am99C88 Max.	Am99CL88 Min.	Am99CL88 Max.	Units
C_I	Input Capacitance	f = 1 MHz	V_{IN} = 0 V		8		8		8	pF
$C_{I/O}$	Input/Output Capacitance		$V_{I/O}$ = 0 V		8		8		8	pF

Notes: These parameters are not 100% tested, but are evaluated at initial characterisation and at any time the design is modified where capacitance may be affected.

SWITCHING TEST CIRCUITS



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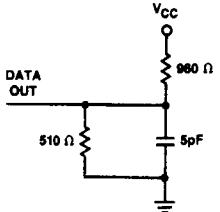
A.



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B.

C_L = 100 pF

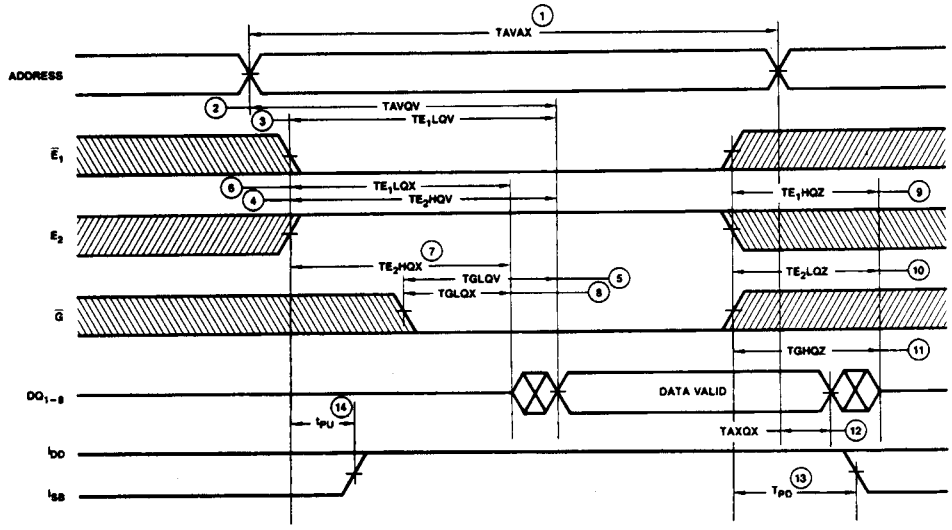
SWITCHING CHARACTERISTICS (Notes 3-7)*

No.	Parameter Symbols		Parameter Description		Am99CS88/ Am99C88/ Am99CL88-70		Am99CS88/ Am99C88/ Am99CL88-10		Am99CS88/ Am99C88/ Am99CL88-12		Am99CS88/ Am99C88/ Am99CL88-15		AM99CS88/ Am99C88-20		Units
					Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE															
1	TAVAX	t_{RC}	Read Cycle Time (Address Valid to Address Don't Care)		70		100		120		150		200		ns
2	TAVQV	t_{AA}	Address Access Time (Address Valid to Data Out Valid)			70		100		120		150		200	ns
3	TE_1LQV	t_{CE1}	Chip Enable Access Time(Chip Enable Valid to Data Out Valid)	$\overline{E_1}$		70		100		120		150		200	ns
4	TE_2HQV	t_{CE2}		E_2		70		100		120		150		200	
5	TGLQV	t_{OE}	Output Enable Valid to Data Out Valid			40		50		60		70		90	ns
6	$\overline{TE_1}LQX$	t_{LZ1}	Chip Enable Valid to Data Out On (Note 7)	$\overline{E_1}$	10		10		10		10		10		ns
7	TE_2HQX	t_{LZ2}		E_2	10		10		10		10		10		
8	TGLQX	t_{OLZ}	Output Enable Valid to Data Out On (Note 7)		5		5		5		5		5		ns
9	TE_1HQZ	t_{HZ1}	Chip Enable Not Valid to Data Out Off (Notes 6 & 7)	$\overline{E_1}$	0	35	0	35	0	40	0	50	0	60	ns
10	TE_2LQZ	t_{HZ2}		E_2	0	35	0	35	0	40	0	50	0	60	
11	TGHQZ	t_{OHZ}	Output Enable Not Valid to Data Out Off (Notes 6 & 7)		0	30	0	35	0	40	0	50	0	60	ns
12	TAXQX	t_{OH}	Output Hold from Address Change		3		3		3		3		3		ns
13		t_{PD}	Chip Disable to Power-Down Delay (Note 3)			40		50		60		70		90	ns
14		t_{PU}	Chip Enable to Power Up (Note 3)		0		0		0		0		0		
WRITE CYCLE															
15	TAVAX	t_{WC}	Write Cycle Time (Address Valid to Addres Don't Care)		70		100		120		150		200		ns
16	TE_1LWH	t_{CW}	Chip Enable to End of Write (Note 5)	$\overline{E_1}$	65		80		85		100		140		ns
17	TE_2HWH	t_{CW}		E_2	65		80		85		100		140		ns
18	TAVWL	t_{AS}	Address Setup Time		0		0		0		0		0		ns
19	TAVWH	t_{AW}	Address Valid to End of Write		65		80		85		100		140		ns
20	TWLWH	t_{WP}	Write Pulse Width (Note 5)		60		60		70		90		120		ns
21	TWHAX	t_{WR1}	End of Write to Address Don't Care	$\overline{E_1}$, $\overline{W}$	5		5		5		10		15		ns
22	TE_2LAX	t_{WR2}		E_2	15		15		15		15		20		
23	TWHQX	t_{OW}	Write Enable LOW to Data Out Off (Notes 6,7)		0	30	0	35	0	40	0	50	0	60	ns
24	TWLQZ	t_{WHZ}	Data in Valid to Write Enable HIGH		30		40		50		60		70		ns
25	TWHDX	t_{DH}	Write Enable HIGH to Data Don't Care		0		0		0		0		0		ns
26	TWHQX	t_{OW}	Write Enable HIGH to Data Out Active (Note 7)		10		10		10		10		10		ns

Notes:
1. Absolute Maximum Ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, ambient temperature is defined as the stabilized case temperature.
3. Parameter not tested, guaranteed by characterization.
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH} and 100 pF load capacitance. Output timing reference is 1.5 V.
5. The internal write time of the memory is defined by the overlap of $\overline{E_1}$ and E_2 active and $\overline{W}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
6. The minimum limit is not tested and is included for design information only.
7. Parameter not tested, guaranteed by characterization using the load shown in B. under Switching Test Circuits.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS (Cont'd.)



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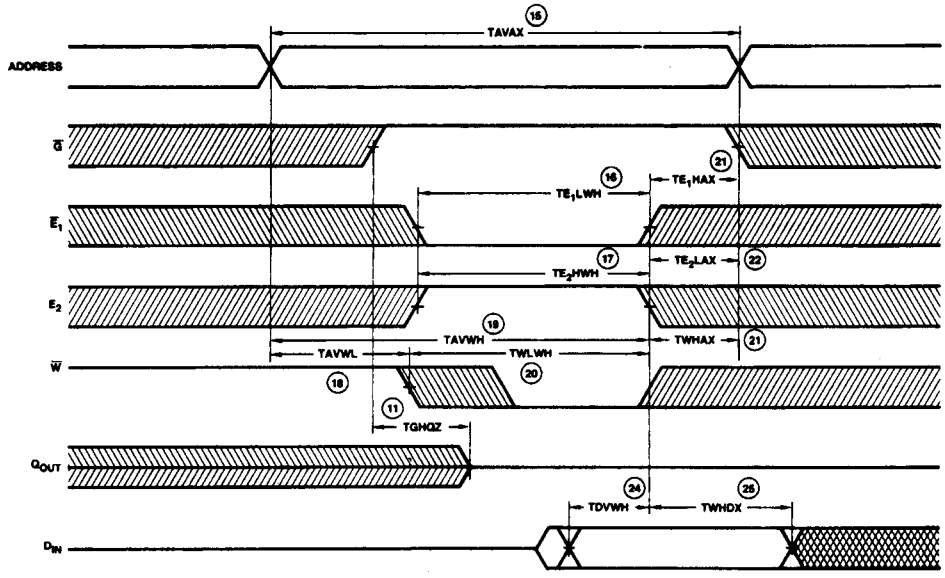
Read Cycle ($\overline{W}$ HIGH)

SWITCHING WAVEFORMS



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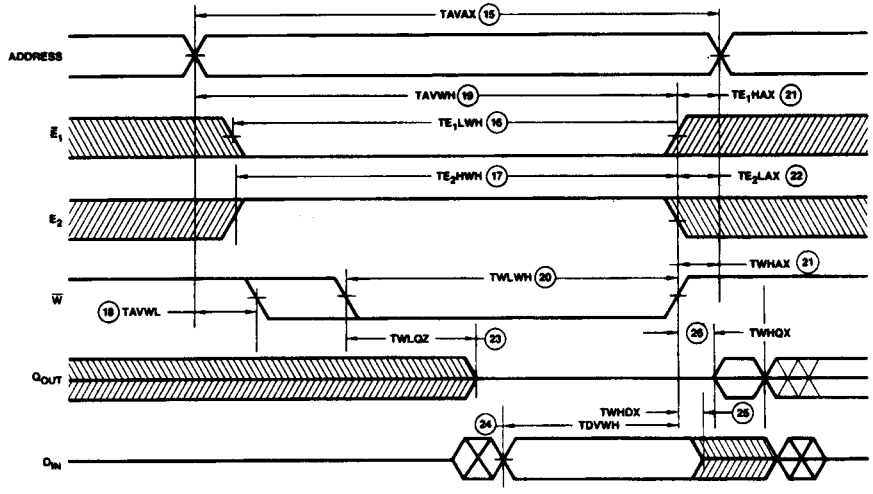
Write Cycle 1



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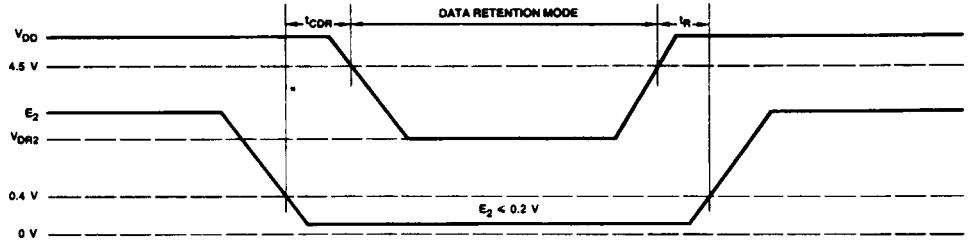
Write Cycle 2 ($\overline{G}$ LOW)

4

LOW V_{DD} DATA RETENTION CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Am99CS88		Am99C88		Am99CL88		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{DR1}	V_{DD} for Data Retention	$\overline{E_1} \geq V_{DD}-0.2$, $E_2 \geq V_{DD}-0.2$ V or $E_2 \leq 0.2$ V	2.0		2.0		2.0		V
V_{DR2}		$E_2 \leq 0.2$ V							
I_{DDR1}	Data Retention Current	$V_{DD}=0.2$ V, $\overline{E_1} \geq V_{DD}-0.2$ V, $E_2 \geq 0.2$ V or $E_2 \leq 0.2$ V		5000		1000		50	µA
I_{DDR2}		$V_{DD}=2.0$ V, $E_2 \leq 0.2$ V		5000		1000		50	µA
t_{CDR}	Chip Deselect to Data Retention Time (Note 1)	See Waveform (Note 2)	0		0		0		ns
t_R	Operating Recovery Time (Note 1)		t_{RC}		t_{RC}		t_{RC}		ns



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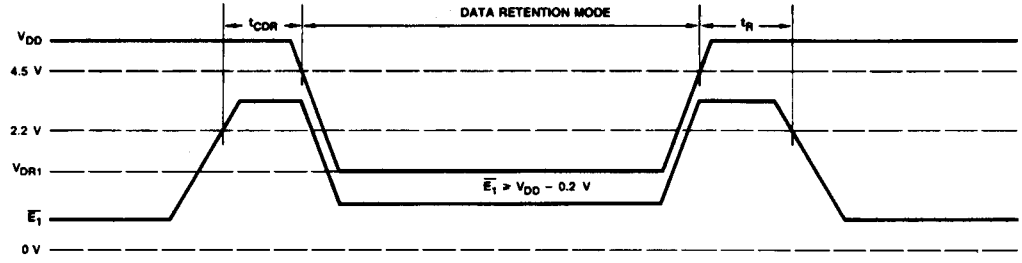
Low V_{DD} Data Retention Waveform 1 (E_2 Controlled)



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Low V_{DD} Data Retention Waveform 2 ($\overline{E_1}$ Controlled, $E_2 \geq V_{DD}-0.2$ V or $E_2 \leq 0.2$ V)

Notes: 1. Parameter not tested, guaranteed by design.
2. Waveforms shown are not actual and may vary in use.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
I_{OH}	1, 2, 3
I_{OL}	1, 2, 3
V_{IH}	7, 8
V_{IL}	7, 8
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{DD}	1, 2, 3
I_{DD1}	1, 2, 3
I_{SB}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	TAVAX (t_{RC})	7, 8, 9, 10, 11	17	TE_2HWH (t_{CW})	7, 8, 9, 10, 11
2	TAVQV (t_{AA})	7, 8, 9, 10, 11	18	TAVWL (t_{AS})	7, 8, 9, 10, 11
3	TE_1LQV (t_{CE1})	7, 8, 9, 10, 11	19	TAVWH (t_{AW})	7, 8, 9, 10, 11
4	TE_2HQV (t_{CE2})	7, 8, 9, 10, 11	20	TWLWH (t_{WP})	7, 8, 9, 10, 11
5	TGLQV (t_{OE})	7, 8, 9, 10, 11	21	TWHAX (t_{WR1})	7, 8, 9, 10, 11
8	TGLQX (t_{OLZ})	7, 8, 9, 10, 11	22	TE_2LAX (t_{WR2})	7, 8, 9, 10, 11
12	TAXQX (t_{OH})	7, 8, 9, 10, 11	24	TWLQZ (t_{WHZ})	7, 8, 9, 10, 11
15	TAVAX (t_{WC})	7, 8, 9, 10, 11	25	TWHDX (t_{DH})	7, 8, 9, 10, 11
16	TE_1LWH (t_{CW})	7, 8, 9, 10, 11			

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.