



Advanced Information

DESCRIPTION — The SN54ALS/74ALS109 consists of two high speed completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D flip-flop by simply connecting the J and \bar{K} pins together.

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	\bar{S}_D	\bar{C}_D	J	\bar{K}	Q	\bar{Q}
Preset	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Underdetermined	L	L	X	X	H	H
Load "1" (Set)	H	H	h	h	H	\bar{L}
Hold	H	H	l	h	q	\bar{q}
Toggle	H	H	h	l	\bar{q}	q
Load "0" (Reset)	H	H	l	l	L	H

*Both outputs will be HIGH while both \bar{S}_D and \bar{C}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{C}_D go HIGH simultaneously.

H, h = HIGH Voltage Level

L, l = LOW Voltage Level

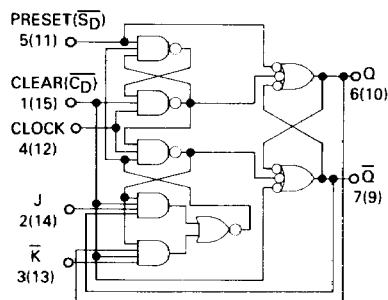
X = Don't Care

l, h(q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

SN54ALS109
SN74ALS109

DUAL JK POSITIVE EDGE-TRIGGERED FLIP-FLOP
ADVANCED LOW POWER SCHOTTKY

LOGIC DIAGRAM



VCC = Pin 16
GND = Pin 8

J Suffix — Case 620-06
N Suffix — Case 648-05

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GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
TA	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
IOH	Output Current — High	54, 74			-0.4	mA
IOL	Output Current — Low	54			4.0	mA
		74			8.0	

This document contains information on a new product. Specifications and information herein are subject to change without notice.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54		0.8	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.4	V	V _{CC} = MIN, I _{OH} = -400 μA, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7	3.4	V	
V _{OL}	Output LOW Voltage	54,74	0.25	0.4	V	I _{OL} = 4.0 mA I _{OL} = I _{OL} 8.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74	0.35	0.5	V	
I _{IH}	Input HIGH Current J, \bar{K} Clock, Set, Clear			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
	J, \bar{K} , Clock, Set, Clear			0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current J, \bar{K} , Clock \bar{S}_D , \bar{C}_D			-0.2 -0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Output Short Circuit Current	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current			4.0	mA	V _{CC} = MAX, V _{CP} = 0 V

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS
		MIN	TYP	MAX	
f _{MAX}	Maximum Clock Frequency	30			MHz
t _{PLH} t _{PHL}	Propagation Delay, Clock to Output			20 30	ns
t _{PLH} t _{PHL}	Propagation Delay, Preset or Clear to Output			15	ns
	CP = L			25	
t _{PHL}	CP = H			35	

AC SETUP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS
		MIN	TYP	MAX	
t _w	Clock Pulse Width (HIGH)	18			ns
t _w	Set or Clear Pulse Width	15			ns
t _s	Setup Time, Data to Clock	20			ns
t _h	Hold Time, Data to Clock	0			ns

