Signetics

74AC/ACT11655

Octal Buffer/Line Driver with 9-Bit Parity Checker/Generator (3-State), INV

ACL Products

Objective Specification

FEATURES

- Inverting 3-State outputs
- Combines '240 and '280 functions in one package
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11655 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11655 device is an octal buffer and line driver with parity generator/checker designed for use with memory address drivers, clock drivers, and bus-oriented transmitters/receivers.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS $T_A = 25°C$; GND = 0V; $V_{CC} = 5.0V$		TYPICAL		UNIT
				AC	ACT	
$t_{PLH}/$ t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	$C_L = 50pF$		4.1	5.8	ns
C_{PD}	Power dissipation capacitance per buffer[1]	$f = 1MHz$;	Enabled	21	23	pF
		$C_L = 50pF$	Disabled	8	8	
C_{IN}	Input capacitance	$V_I = 0V$ or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	$V_O = 0V$ or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O) \text{ where:}$$

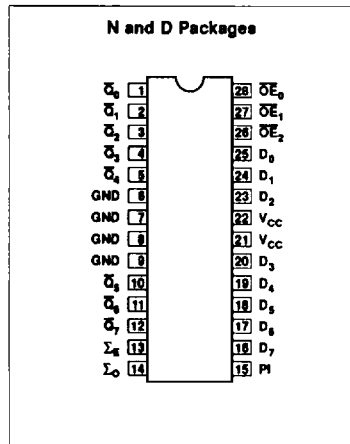f_I = input frequency in MHz, C_L = output load capacitance in pF,

f_O = output frequency in MHz, V_{CC} = supply voltage in V,

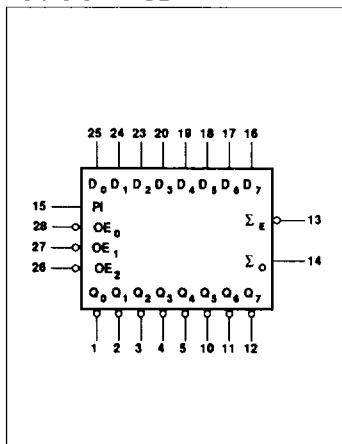$\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

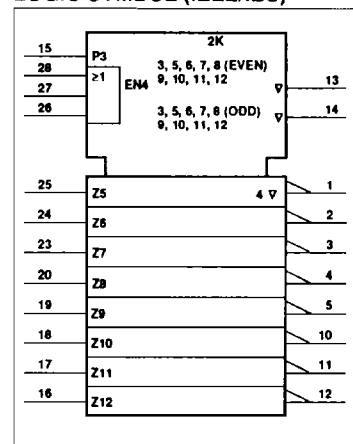| PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11655N 74ACT11655N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11655D 74ACT11655D

PIN CONFIGURATION

N and D Packages

LOGIC SYMBOL

LOGIC SYMBOL (IEEE/IEC)

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PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15	PI	Parity input
28, 27, 26	$\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$	Output enable input (active-Low)
25, 24, 23, 20, 19, 18, 17, 16	D_0 - D_7	Data inputs
1, 2, 3, 4, 5, 10, 11, 12	$\overline{Q}_0$ - $\overline{Q}_7$	Data outputs
13, 14	Σ_E, Σ_O	Parity outputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS
$\overline{OE}_0$	$\overline{OE}_1$	$\overline{OE}_2$	D_n	$\overline{Q}_n$
L	L	L	L	H
L	L	L	H	L
H	X	X	X	Z
X	H	X	X	Z
X	X	H	X	Z

INPUTS	PARITY OUTPUTS	
Number of inputs High (PI, D_0 - D_7)	Σ_E	Σ_O
EVEN—0, 2, 4, 6, 8	H	L
ODD—1, 3, 5, 7, 9	L	H
Any $\overline{OE}$ = High	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance state

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11655			74ACT11655			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	$V_O = 0$ to V_{CC}	±50	mA
I_{CC} or	DC V_{CC} current		±250	mA
I_{GND}	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_CC (V)	74AC11655 T_A=+25°C Min	74AC11655 T_A=+25°C Max	74AC11655 T_A=-40°C to +85°C Min	74AC11655 T_A=-40°C to +85°C Max	74ACT11655 T_A=+25°C Min	74ACT11655 T_A=+25°C Max	74ACT11655 T_A=-40°C to +85°C Min	74ACT11655 T_A=-40°C to +85°C Max	UNIT
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	$V_I = V_{IL}$ or V_{IH}	$I_{OH} = -50\mu A$	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			$I_{OH} = -4mA$	3.0	2.58		2.48						
			$I_{OH} = -24mA$	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			$I_{OH} = -75mA$[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	$V_I = V_{IL}$ or V_{IH}	$I_{OL} = 50\mu A$	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			$I_{OL} = 12mA$	3.0		0.36		0.44					
			$I_{OL} = 24mA$	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			$I_{OL} = 75mA$[1]	5.5				1.65				1.65	
I_I	Input leakage current	$V_I = V_{CC}$ or GND		5.5		±0.1		±1.0		±0.1		±1.0	µA
I_{OZ}	3-State output off-state current	$V_I = V_{IL}$ or V_{IH}, $V_O = V_{CC}$ or GND		5.5		±0.5		±5.0		±0.5		±5.0	µA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$ or GND, $I_O = 0$		5.5		8.0		80		8.0		80	µA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.