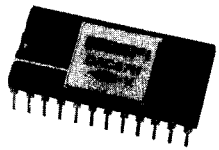
BURR-BROWN®



DAC85H
DAC87H

MILITARY VERSION AVAILABLE

Monolithic 12-Bit DIGITAL-TO-ANALOG CONVERTERS

FEATURES

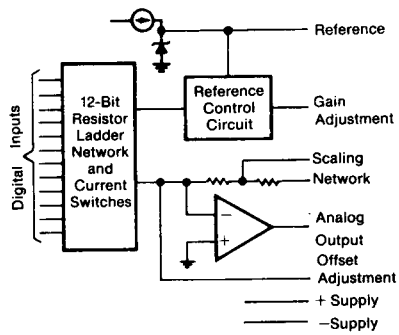
- INDUSTRY STANDARD PINOUT
- LOW POWER DISSIPATION: 345mW
- FULL ±10V SWING WITH V_{CC} = ±12VDC
- DIGITAL INPUTS ARE TTL- AND CMOS-COMPATIBLE
- GUARANTEED SPECIFICATIONS WITH ±12V AND ±15V SUPPLIES
- SINGLE-CHIP DESIGN
- ±1/2LSB MAXIMUM NONLINEARITY, −55°C to +125°C
- GUARANTEED MONOTONICITY, −55°C TO +125°C
- PACKAGE: Hermetic Side-brazed Ceramic DIP
- SETTLING TIME: 4μs max to ±0.01% of Full Scale

DESCRIPTION

These monolithic digital-to-analog converters are pin-for-pin equivalent to the industry standard DAC85 and DAC87 first introduced by Burr-Brown. Their single-chip design includes the output amplifier and provides a highly stable reference capable of supplying up to 2.5mA to an external load without degradation of D/A performance.

These converters use proven circuit techniques to provide accurate and reliable performance over temperature and power supply variations. The use of a buried zener diode as the bias for the internal reference contributes to the high stability and low noise of the device. Advanced methods of laser trimming result in precision output current and output amplifier feedback resistors, as well as low integral and differential linearity errors. Innovative circuit design enables the DAC85 and DAC87 to operate at supply voltages as low as ±11.4V with no loss in performance or accuracy over any range of output voltage. Ease of use has been enhanced by eliminating the need for a +5V logic power supply. The lower power dissipation of the 118 mil by 121 mil chip results in higher reliability and greater long term stability.

Both models are available in a hermetic, side-brazed, ceramic DIP. The DAC85H is specified over the industrial temperature range of −25°C to +85°C. The DAC87H is specified over the entire military temperature range of −55°C to +125°C.



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PDS-681A

SPECIFICATIONS

ELECTRICAL

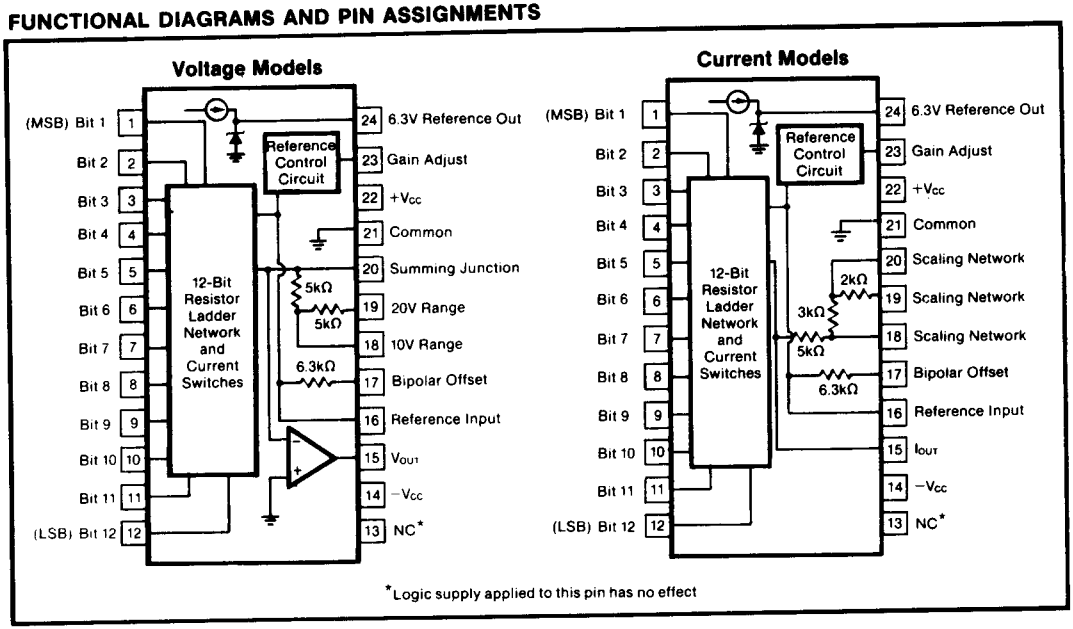
Typical at +25°C and $\pm V_{CC}$ = 12V or 15V unless otherwise noted.

MODEL	DAC85H			DAC87H			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL INPUT							
Resolution			12			*	Bits
Logic Levels (0°C to +70°C)[1]:							
V_{IH} (Logic "1")	+2		+16.5	*		*	VDC
V_{IL} (Logic "0")	0		+0.8	*		*	VDC
I_{IH} (V_{IN} = +2.4V)			+20			*	µA
I_{IL} (V_{IN} = +0.4V)			−180			*	µA
ACCURACY (at 25°C)							
Linearity Error		±1/4	±1/2		*	*	LSB
Differential Linearity Error		±1/2	±3/4		*	*	LSB
Gain Error[2]		±0.1	±0.2			±0.1	%
Offset Error[2]		±0.5	±0.1			±0.05	% of FSR[3]
DRIFT (over specification temperature range)[4]							
Total bipolar drift (incldues gain, offset, and linearity drifts)		±10	±25			±30	ppm of FSR/°C
Total Error (over specification temperature range[5]: Unipolar			±0.2			*	% of FSR
Bipolar			±0.12			±0.2	% of FSR
Gain: Including Internal Reference			±20			*	ppm/°C
Excluding Internal Reference		±5	±10		*	*	ppm/°C
Unipolar Offset			±3			*	ppm of FSR/°C
Bipolar Offset			±10			*	ppm of FSR/°C
Differential Linearity			±3/4			*	LSB
Linearity Error		±1/4	±1/2		*	*	LSB
Monotonicity Guaranteed	−25		+85	−55		+125	°C
CONVERSION SPEED, V_{OUT} models							
Settling Time to ±0.012% of FSR							
For FSR change (2kΩ || 500pF load):							
with 10kΩ Feedback		3	4		*	*	µs
with 5kΩ Feedback		2	3		*	*	µs
For 1LSB Change		1			*		µs
Slew Rate	10			*			V/µs
CONVERSION SPEED, I_{OUT} models							
Settling Time to ±0.01% of FSR							
For FSR change: 10Ω to 100Ω load		300			*		ns
1kΩ load		1			*		µs
ANALOG OUTPUT, V_{OUT} models							
Ranges		±2.5, ±5, ±10, +5, +10			*		V
Output Current[6]	±5			*			mA
Output Impedance (DC)		0.05			*		Ω
Short Circuit to Common, Duration[7]		Indefinite			*		
ANALOG OUTPUT, I_{OUT} models							
Ranges: Bipolar	±0.96	±1.0	±1.04	*	*	*	mA
Unipolar	−1.96	−2.0	−2.04	*	*	*	mA
Output Impedance: Bipolar	2.6	3.2	3.7	*	*	*	kΩ
Unipolar	4.6	6.6	8.6	*	*	*	kΩ
Compliance	−2.5		+2.5	*		*	V
REFERENCE VOLTAGE OUTPUT	+6.23	+6.30	+6.37	*	*	*	V
External Current (constant load)			2.5			*	mA
Drift vs Temperature			±20			±10	ppm/°C
Output Impedance		1			*		Ω
POWER SUPPLY SENSITIVITY							
V_{CC} = ±12VDC or ±15VDC		±0.002	±0.006		*	±0.004	% FSR/ % V_{CC}
POWER SUPPLY REQUIREMENTS							
$\pm V_{CC}$	±11.4		±16.5	*		*	VDC
Supply Drain (no load): $+V_{CC}$		8	12		*	*	mA
$-V_{CC}$		15	20		*	*	mA
Power Dissipation (V_{CC} = ±15VDC)		345	480		*	*	mW
TEMPERATURE RANGE							
Specification	−25		+85	−55		+125	°C
Storage	−65		+150	*		*	°C

*Specification same as DAC85H.

NOTES: (1) Refer to "Logic Input Compatibility" section. (2) Adjustable to zero with external trim potentiometer. (3) FSR means full scale range and is 20V for ±10V range, 10V for ±5V range for V_{OUT} models; 2mA for I_{OUT} models. (4) To maintain drift spec, internal feedback resistors must be used. (5) Includes the effects of gain, offset and linearity drift. Gain and offset errors externally adjusted to zero at +25°C. (6) For $\pm V_{CC}$ less than ±12VDC, limit output current load to ±2.5mA to maintain ±10V full scale output voltage swing. For output range of ±5V or less, the output current is ±5mA over entire $\pm V_{CC}$ range. (7) Short circuit current is 40mA, max.

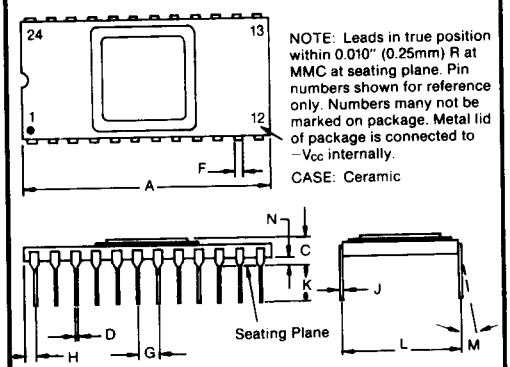
FUNCTIONAL DIAGRAMS AND PIN ASSIGNMENTS



*Logic supply applied to this pin has no effect

MECHANICAL

PACKAGE (Hermetic DIP)



NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers many not be marked on package. Metal lid of package is connected to −Vcc internally.

CASE: Ceramic

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.185	1.215	30.10	30.86
C	.105	.170	2.67	4.32
D	.015	.021	.38	.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.42 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

MATING CONNECTOR: 0245MC

WEIGHT: 4.1 grams (0.15 oz.)

PIN: Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

HERMETICITY: Conforms to Method 1014, Condition A1 or A2 (fine leak) and Condition C (gross leak).

ABSOLUTE MAXIMUM RATINGS

+Vcc to Common	0V to +18V
−Vcc to Common	0V to −18V
Digital Data Inputs to Common	−1V to +18V
Reference Output to Common	±Vcc
Reference Input to Common	±Vcc
Bipolar Offset to Common	±Vcc
10V Range R to Common	±Vcc
20V Range R to Common	±Vcc
External Voltage to DAC Output	−5V to +5V
Max Junction Temperature	165°C
Lead Temperature, Soldering	+300°C, 10s
Thermal Resistance, θ_{JA}	65°C/W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Model	Output
DAC85H-CBI-I	Current
DAC85H-CBI-IBI[1]	Current
DAC85H-CBI-I/QM[2]	Current
DAC85H-CBI-V	Voltage
DAC85H-CBI-VBI	Voltage
DAC85H-CBI-V/QM	Voltage
DAC87H-CBI-V	Voltage
DAC87H-CBI-VBI	Voltage
DAC87H-CBI-V/QM	Voltage

NOTES: (1) BI indicates burn-in screening option at +125°C for 160h or equivalent. See text for details. (2) QM indicates environmental screening. See text for details.

ENVIRONMENTAL SCREENING

/QM Screening

Burr-Brown /QM models are environmentally-screened versions of our standard industrial products, designed to provide enhanced reliability. The screening, tabulated below, is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified below. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

Screening Flow For /QM Models

Screen	MIL-STD-883 Method	Condition	Comments
Internal Visual	2010	B	
High Temperature Storage (Stabilization Bake)	1008	C	+150°C, 24hrs
Temperature Cycling	1010	C	−65 to +150°C, 10 cycles
Burn-in	1015	B	+125°C, 160hrs
Constant Acceleration	2001	E	30,000 Gs
Hermeticity Fine Leak Gross Leak	 1014 1014	 A1 or A2 C	 5×10^{-8} atm cc/sec 60psig, 2hrs
External Visual	2009		

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC85H Series accepts complementary binary digital input codes. The CBI model may be connected by the user for any one of three complementary codes: CSB, COB, or CTC (see Table I).

TABLE I. Digital Input Codes.

Digital Input	Analog Output		
MSB ↓ LSB ↓	CSB Complementary Straight Binary	COB Complemen. Offset Binary	CTC* Complemen. Two's Complement
000000000000	+Full Scale	+Full Scale	−1LSB
011111111111	+1/2 Full Scale	Zero	−Full Scale
100000000000	1/2 Full Scale −1LSB	−1LSB	+Full Scale
111111111111	Zero	−Full Scale	Zero
*Invert the MSB of the COB code with an external inverter to obtain CTC code.			

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC85H Series is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over the specification temperature range is guaranteed in the DAC85H Series to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for each DAC85H Series model at minimum temperature, +25°C and maximum temperature; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications both with and without internal reference.

Offset drift is a measure of the actual change in output over the specification temperature range with all "1"s on the input. The offset is measured at +25°C, minimum temperature and maximum temperature. The maximum change in Offset is referenced to the Offset at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each DAC85H Series model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

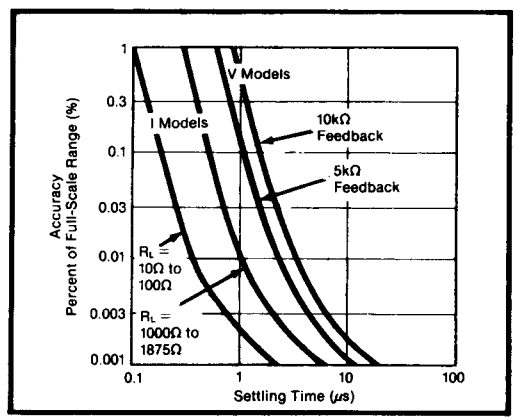


FIGURE 1. Full Scale Range Settling Time vs Accuracy.

Voltage Output Models

Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111 . . . 11 to 1000 . . . 00), the point at which the worst case settling time occurs.

Current Output Models

Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω to 1875Ω. Internal resistors are provided for connecting nominal load resistances of approximately 1000Ω to 1800Ω for output voltage range of ±1V and 0 to −2V. See Figure 11.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is ±2.5V. Maximum safe voltage swing permitted without damage to the DAC85H Series is ±5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltages (see Figure 2).

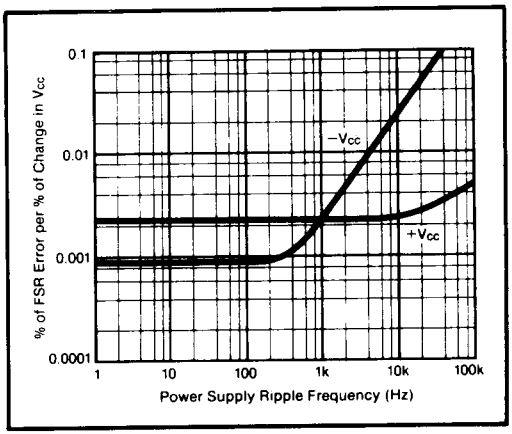


FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

REFERENCE SUPPLY

All DAC85H Series models are supplied with an internal 6.3V reference voltage supply. This voltage (pin 24) has a tolerance of ±1% and must be connected to the Reference Input (pin 16) for specified operation. This reference may be used externally also, but external current drain is limited to 2.5mA.

If a varying load is to be driven, an external buffer amplifier is recommended to drive the load in order to isolate bipolar offset from load variations. Gain and bipolar offset adjustments should be made under constant load conditions.

LOGIC INPUT COMPATIBILITY

DAC85H Series digital inputs are TTL, LSTTL and 4000B, 54/74HC CMOS compatible. The input switching threshold remains at the TTL threshold over the entire supply range.

Logic "0" input current over temperature is low enough to permit driving DAC85H Series directly from outputs of 4000B and 54/74C CMOS devices.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Connect power supply voltages as shown in Figure 3. For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown. These capacitors (1μF tantalum) should be located close to the DAC85H Series.

±12V OPERATION

All DAC85H Series models can operate over the entire power supply range of ±11.4V to ±16.5V. Even with supply levels dropping to ±11.4V, the DAC can swing a full ±10V range, provided the load current is limited to ±2.5mA. With power supplies greater than ±12V, the DAC output can be loaded up to ±5mA. For output swing of ±5V or less, the output current is ±5mA, min. over the entire V_{CC} range.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 3 and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the DAC to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 4, may be substituted.

Existing applications that are converting to the monolithic DAC85H Series must change the gain trim resistor on pin 23 from 18MΩ to 10MΩ to insure sufficient adjustment range. Pin 23 is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Common (pin 21) to prevent noise pickup. Refer to Figure 5 for relationship of Offset and Gain adjustments to unipolar and bipolar D/A operation.

Offset Adjustment

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the Offset potentiometer for zero output.

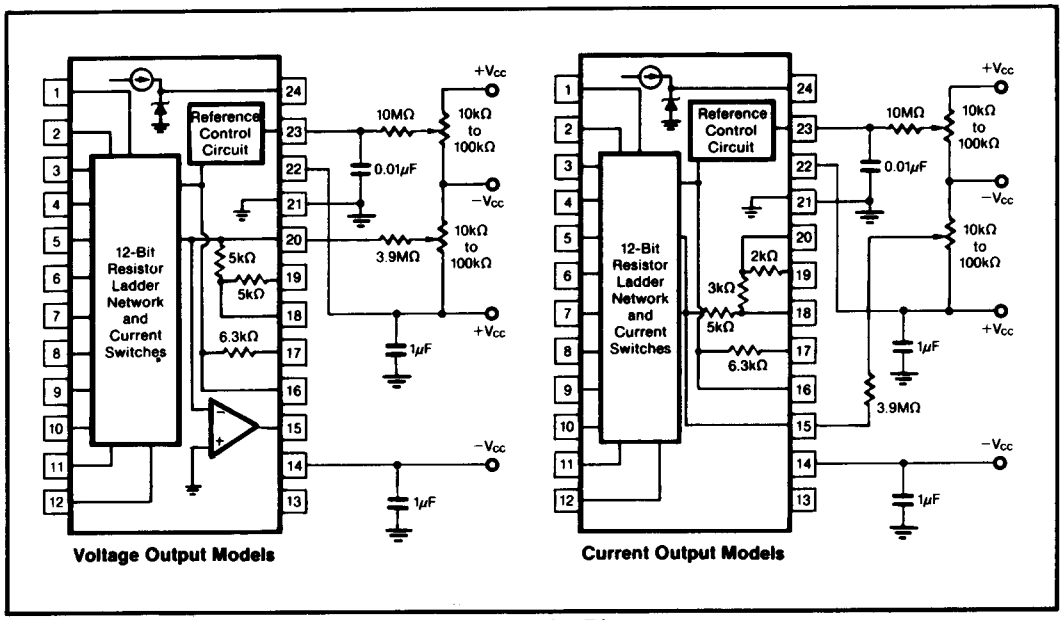


FIGURE 3. Power Supply and External Adjustment Connection Diagrams.

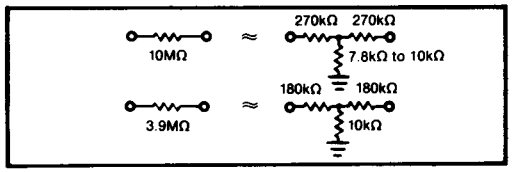


FIGURE 4. Equivalent Resistances.

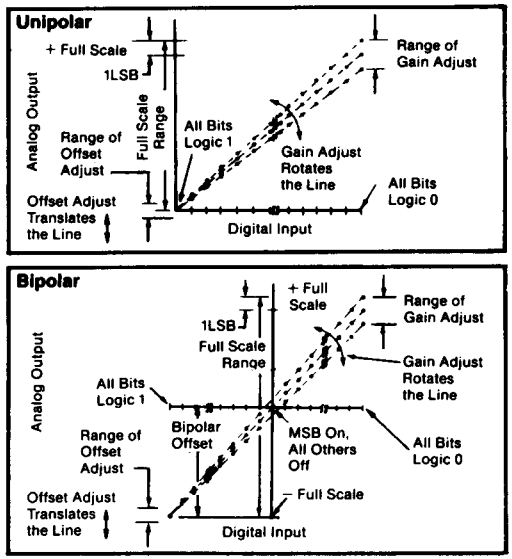


FIGURE 5. Relationship of Offset and Gain Adjustments for a Unipolar and Bipolar D/A Converter.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is −10V. See Table II for corresponding codes.

Gain Adjustment

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output. Adjust the Gain potentiometer for this positive full scale output. See Table II for positive full scale voltages and currents.

TABLE II. Digital Input/Analog Output.

DIGITAL INPUT	ANALOG OUTPUT			
	VOLTAGE*		CURRENT	
MSB LSB	0 to +10V	±10V	0 to -2mA	±1mA
000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
011111111111	+5.0000V	0.0000V	-1.0000mA	0.0000mA
100000000000	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
111111111111	0.0000V	-10.0000V	0.0000mA	+1.000mA
One LSB	2.44mV	4.88mV	0.488μA	0.488μA

*To obtain values for other binary ranges:
0 to +5V range divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

VOLTAGE OUTPUT MODELS

Output Range Connections

Internal scaling resistors provided in the DAC85H Series may be connected to produce bipolar output voltage ranges of ±10V, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V. See Figure 6.

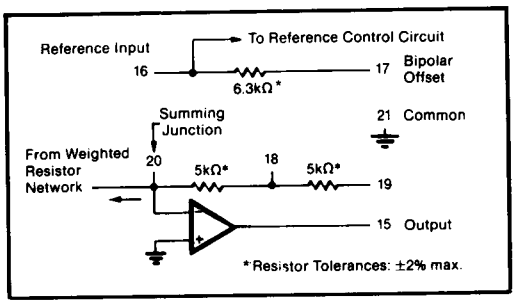


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

Gain and offset drift are minimized because of the thermal tracking of the scaling resistors with other internal device components. Connections for various output voltage ranges are shown in Table III. Settling time for a full-scale range change is specified as 4μs for the 20V range and 3μs for the 10V range.

TABLE III. Output Voltage Range Connections for Voltage Models.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	NC	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	20	24

CURRENT OUTPUT MODELS

The resistive scaling network and equivalent output circuit of the current model differ from the voltage model and are shown in Figures 7 and 8.

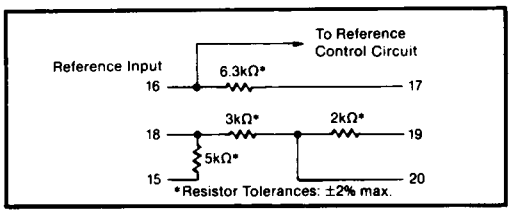


FIGURE 7. Internal Scaling Resistors.

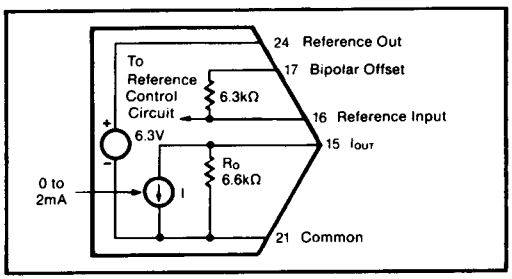


FIGURE 8. Current Output Model Equivalent Output Circuit.

Internal scaling resistors (Figure 7) are provided to scale an external op amp or to configure load resistors for a voltage output. These connections are described in the following sections.

If the internal resistors are not used for voltage scaling, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift.

Driving An External Op Amp

The current output model DAC85H will drive the summing junction of an op amp used as a current-to-voltage converter to produce an output voltage. See Figure 9.

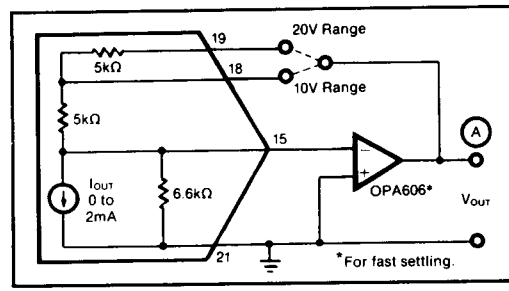


FIGURE 9. External Op Amp—Using Internal Feedback Resistors.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the DAC85H output current and R_F is the feedback resistor. Using the internal feedback resistors of the current output model DAC85H provides output voltage ranges the same as the voltage model DAC85H. To obtain the desired output voltage range when connecting an external op amp, refer to Table IV.

TABLE IV. Voltage Range of Current Output

Output Range	Digital Input Codes	Connect (A) to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	(A)	24
±5V	COB or CTC	18	15	NC	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	15	24

Output Larger Than 20V Range

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and −2mA for unipolar voltage ranges. See Figure 10. Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50ppm/°C plus R_F drift to total drift.

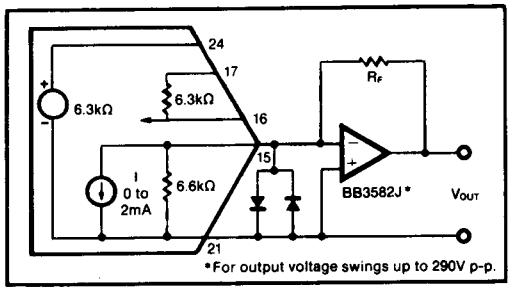


FIGURE 10. External Op Amp—Using External Feedback Resistors.

Driving a Resistive Load Unipolar

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 11 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA\ [(R_L \times R_O) \div (R_L + R_O)]$$

The unipolar output impedance R_O equals 6.6kΩ (typ) and R_{LI} is the internal load resistance of 968Ω (derived by connecting pin 15 to pin 20 and pin 18 to 19). By choosing $R_{LS} = 210\Omega$, $R_L = 1178\Omega$. R_L in parallel with R_O yields 1kΩ total load. This gives an output range of 0 to −2V. Since R_O is not exact, initial trimming per Figure 3 may be necessary; also R_{LS} may be trimmed.

BURN-IN SCREENING

Burn-in screening is an option available for the DAC85BH and DAC87BH. Burn-in duration is 160 hours at +125°C ambient temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "BI" to the base model number.

Driving a Resistive Load Bipolar

The equivalent output circuit for a bipolar output voltage range is similar to Figure 11, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA\ [(R_O \times R_L) \div (R_O + R_L)]$$

By connecting pin 17 to 15, the output current becomes bipolar (±1mA) and the output impedance R_O becomes 3.2kΩ (6.6kΩ || 6.3kΩ). R_{LI} is 1200Ω (derived by connecting pin 15 to 18 and pin 18 to 19). By choosing $R_{LS} = 255\Omega$ (for a bipolar output connect R_{LS} between pin 20 and pin 21), $R_L = 1455\Omega$. R_L in parallel with R_O yields 1kΩ total load. This gives an output range of ±1V. As indicated above, trimming may be necessary.

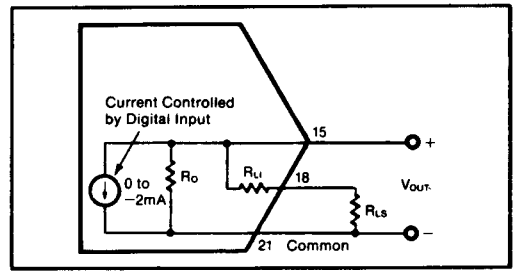


FIGURE 11. Current Output Model Equivalent Circuit Connected for Unipolar Voltage Output with Resistive Load.