

Document No.	853-1503
ECN No.	00732
Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11643

Octal transceiver (3-State) True/INV

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: ± 24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11643 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11643 devices are octal transceivers featuring 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The devices feature an Output Enable (\overline{OE}) input for easy cascading and a Direction (DIR) input for direction control. Note that data transmitted from the A side to the B side is inverted and that data transmitted from the B side to the A side is not inverted.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^\circ\text{C}; \text{GND} = 0\text{V};$ $V_{CC} = 5.0\text{V}$		TYPICAL		UNIT
		AC	ACT	AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A_n to B_n , or B_n to A_n	$C_L = 50\text{pF}$		5.2	5.7	ns
C_{PD}	Power dissipation capacitance per transceiver ¹	$f = 1\text{MHz};$ $C_L = 50\text{pF}$	Enabled	46	41	pF
			Disabled	9.0	9.0	
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}		4.0	4.0	pF
C_{VO}	I/O capacitance	$V_{IO} = 0\text{V}$ or V_{CC} ; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jeduc JC40.2 Standard 17		500	500	mA

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \sum (C_L \times V_{CC}^2 \times f_O) \text{ where:}$$

f_I = input frequency in MHz, C_L = output load capacitance in pF,

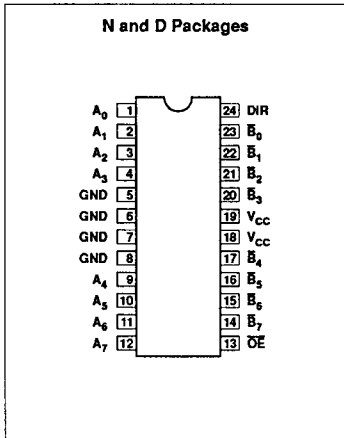
f_O = output frequency in MHz, V_{CC} = supply voltage in V,

$\sum (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

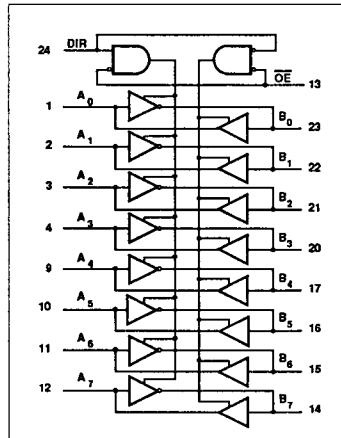
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to $+85^\circ\text{C}$	74AC11643N 74ACT11643N
24-pin plastic SOL (300mil-wide)	-40°C to $+85^\circ\text{C}$	74AC11643D 74ACT11643D

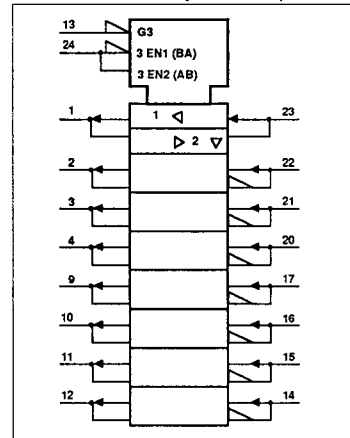
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	DIR	Direction control input
1, 2, 3, 4, 9, 10, 11, 12	A ₀ - A ₇	Data inputs/outputs (A side)
23, 22, 21, 20, 17, 16, 15, 14	B ₀ - B ₇	Data inputs/outputs (B side)
13	\overline{OE}	Output enable
5, 6, 7, 8	GND	Ground (0V)
18, 19	V _{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to \overline{B} bus
H	X	Z

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11643			74ACT11643			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	DC supply voltage	3.0 ¹	5.0	5.5	4.5	5.0	5.5	V
V _I	Input voltage	0		V _{CC}	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	0		V _{CC}	V
$\Delta V/\Delta t$	Input transition rise or fall rate	0		10	0		10	ns/V
T _{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:

- No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 TO +7.0	V
I _{IK} or V _I	DC input diode current ²	V _I < 0	-20	mA
		V _I > V _{CC}	20	
	DC input voltage		-0.5 to V _{CC} + 0.5	V
I _{OK} or V _O	DC output diode current ²	V _O < 0	-50	mA
		V _O > V _{CC}	50	
	DC output voltage		-0.5 to V _{CC} + 0.5	V
I _O	DC output source or sink current per output pin	V _O = 0 to V _{CC}	±50	mA
I _{CC} or I _{GND}	DC V _{CC} current		±200	mA
	DC ground current		±200	
T _{STG}	Storage temperature		-65 to 150	°C
P _{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC} V	74AC11643				74ACT11643				UNIT	
				T _{amb} = +25°C		T _{amb} = -40°C to +85°C		T _{amb} = +25°C		T _{amb} = -40°C to +85°C			
				Min	Max	Min	Max	Min	Max	Min	Max		
V _{IH}	High-level input voltage		3.0	2.10		2.10						V	
			4.5	3.15		3.15		2.0		2.0			
			5.5	3.85		3.85		2.0		2.0			
V _{IL}	Low-level input voltage		3.0		0.90		0.90					V	
			4.5		1.35		1.35		0.8		0.8		
			5.5		1.65		1.65		0.8		0.8		
V _{OH}	High-level output voltage	V _I = V _{IL} or V _{IH}	I _{OH} = -50μA	3.0	2.9		2.9					V	
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I _{OH} = -4mA	3.0	2.58		2.48						
				4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
I _{OH} = -75mA ¹	3.0			3.85				3.85					
	5.5												
V _{OL}	Low-level output voltage	V _I = V _{IL} or V _{IH}	I _{OL} = 50μA	3.0		0.1		0.1				V	
				4.5		0.1		0.1		0.1			0.1
				5.5		0.1		0.1		0.1			0.1
			I _{OL} = 12mA	3.0		0.36		0.44					
				4.5		0.36		0.44		0.36			0.44
			I _{OL} = 24mA	3.0		0.36		0.44		0.36			0.44
				5.5		0.36		0.44		0.36			0.44
I _{OL} = 75mA ¹	3.0				1.65				1.65				
I _I	Input leakage current	V _I = V _{CC} or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA	
I _{OZ}	3-State output off-state current	V _I = V _{IL} or V _{IH} , V _O = V _{CC} or GND	5.5		±0.5		5.0		±0.5		5.0	μA	
I _{CC}	Quiescent supply current	V _I = V _{CC} or GND, I _O = 0mA	5.5		8.0		80		8.0		80	μA	
ΔI _{CC}	Supply current, TTL inputs High ²	One input at 3.4V, other inputs at V _{CC} or GND	5.5						0.9		1.0	mA	

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
- This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

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AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11643					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay A _n to \bar{B}_n , B _n to A _n	1	1.5 1.5	7.4 6.6	10.1 8.7	1.5 1.5	11.3 10.0	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	1.5 1.5	9.4 8.9	11.8 11.4	1.5 1.5	13.3 13.0	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	1.5 1.5	8.3 8.9	10.1 10.9	1.5 1.5	10.9 12.0	ns

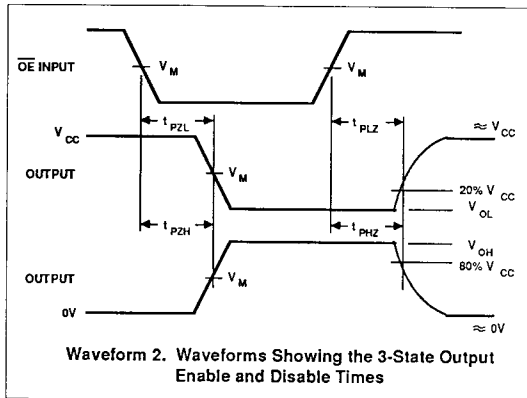
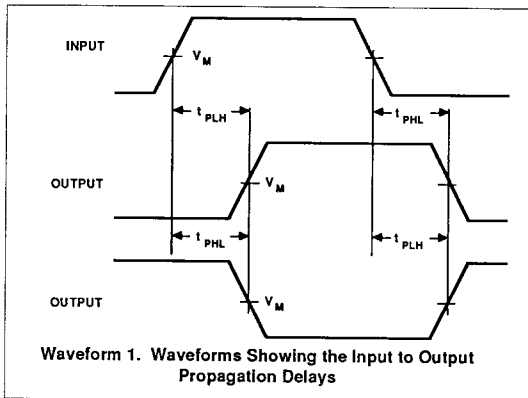
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11643					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay A _n to \bar{B}_n , B _n to A _n	1	1.5 1.5	5.4 5.0	7.7 6.8	1.5 1.5	8.6 7.9	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	1.5 1.5	7.0 6.6	9.2 8.7	1.5 1.5	10.4 10.0	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	1.5 1.5	7.1 7.2	8.8 9.0	1.5 1.5	9.4 9.8	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11643					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay A _n to \bar{B}_n , B _n to A _n	1	1.5 1.5	5.6 5.7	8.3 7.7	1.5 1.5	9.3 8.8	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	1.5 1.5	8.1 7.7	11.5 10.1	1.5 1.5	12.9 11.4	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	1.5 1.5	9.1 9.3	12.0 11.6	1.5 1.5	13.1 12.7	ns

AC WAVEFORMS



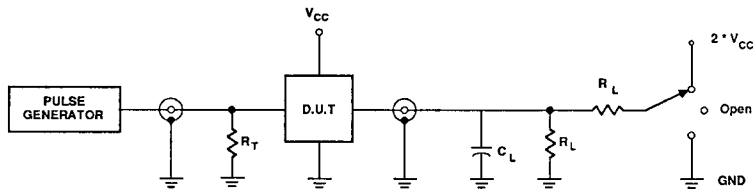
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WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	$V_{IN} = \text{GND to } V_{CC},$ $V_M = 50\% V_{CC}$	$V_{OUT} = V_{OL} \text{ to } V_{OH}$ $V_M = 50\% V_{CC}$
ACT	$V_{IN} = \text{GND to } 3.0V,$ $V_M = 1.5V$	

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \cdot V_{CC}$
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

- C_L = Load capacitance, 50pF; includes jig and probe capacitance
 - R_L = Load resistor, 500Ω
 - R_T = Termination resistance should be equal to Z_{OUT} of pulse generators
- Input pulses: $PRR \leq 10\text{MHz}$
 $t_r = t_f = 3\text{ns}$