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Preliminary Information

1.0 Features

- Single PLL with differential 3.3V LVPECL output driver
- Spread-spectrum modulation for reduced EMI: -0.5% downspread modulation at 31.5kHz
- ROM-based (fixed-frequency) version of the programmable FS71429
- Internal crystal reference oscillator and integrated loop filter require no external components
- Accepts 5MHz to 27MHz crystal resonators
- Available in 28-pin (0.300") SOIC

2.0 Description

The FS61429 is a CMOS clock generator IC with a differential high-speed LVPECL output designed to for a variety of high speed electronic systems. This device is a ROM-based (fixed-frequency) version of the programmable FS71429 clock generator.

Figure 1: Pin Configuration

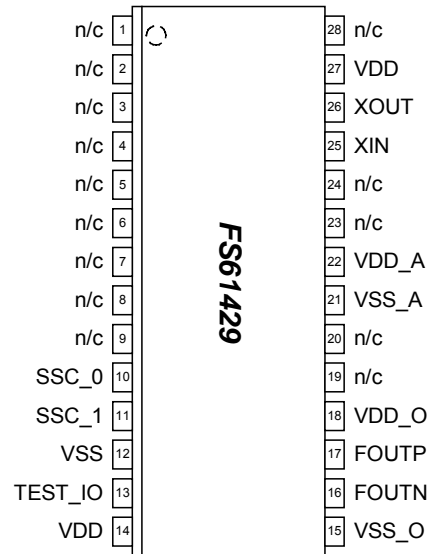
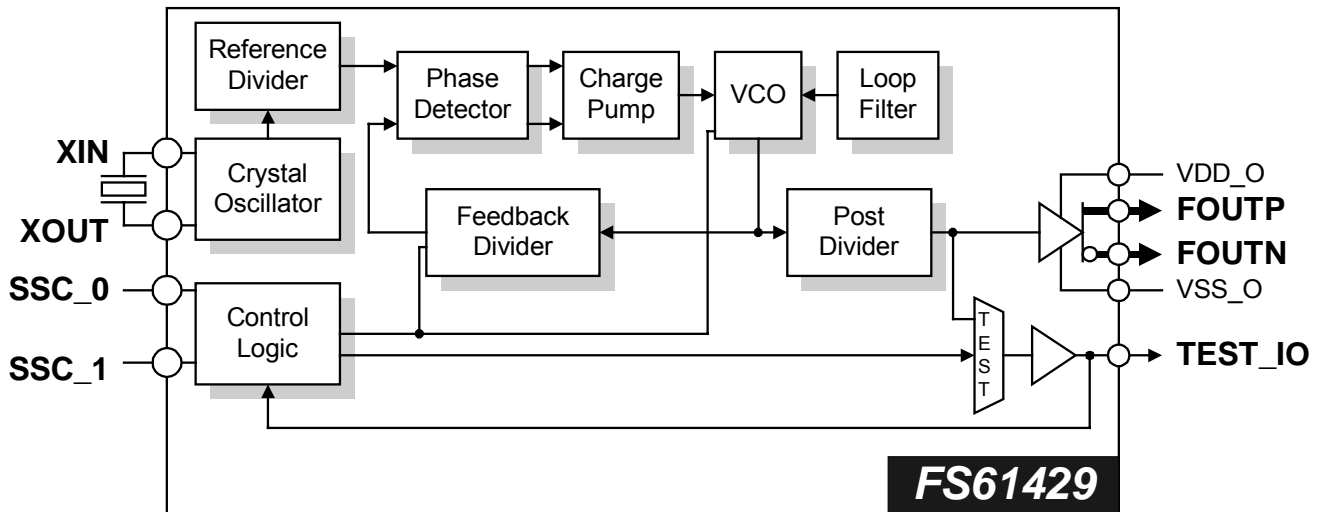


Figure 2: Block Diagram



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Table 1: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI_D = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active Low pin

PIN	TYPE	NAME	DESCRIPTION
1, 2, 3, 4, 5, 6, 7, 8, 9	-	n/c	No connection
10	DI ^U	SSC_0	Function controls
11	DI ^U	SSC_1	Function controls
12	P	VSS	Ground for internal logic
13	DIO	TEST_IO	LVTTTL Test mode output
14	P	VDD	3.3V power supply for internal logic
15	P	VSS_O	Ground for PECL output pins
16	AO	FOUTN	PECL output (complement)
17	AO	FOUTP	PECL output (true)
18	P	VDD_O	3.3V power supply for PECL output pins
19, 20	-	n/c	No connection
21	P	VSS_A	Ground supply for PLL core
22	P	VDD_A	3.3V power supply for PLL core
23, 24	-	n/c	No connection
25	AI	XIN	Crystal oscillator input
26	AO	XOUT	Crystal oscillator feedback This pin may be overdriven with an external reference clock if XIN is left floating
27	P	VDD	3.3V power supply
28	-	n/c	No connection

Table 2: SSC_0:1 Function Table

SSC_0	SSC_1	SPREAD SPECTRUM ENABLED	PLL OPERATION	OUTPUT FREQUENCY (F _{XIN} = 16.667MHz)	TEST_IO OPERATION
0	0	<i>Reserved – Supplier Test Mode</i>			Output
0	1	NO	Stopped	TEST_IO	Input
1	0	YES	Running	200MHz	Tristate
1	1	NO	Running	200MHz	Tristate

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3.0 Electrical Specifications

Table 3: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage, dc ($V_{SS} = \text{ground}$)	V_{DD}	$V_{SS}-0.5$	4	V
Input Voltage, dc	V_I	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	V_O	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Input Clamp Current, dc ($V_I < 0$ or $V_I > V_{DD}$)	I_{IK}	-50	50	mA
Output Clamp Current, dc ($V_I < 0$ or $V_I > V_{DD}$)	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		150	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV



CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 4: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}	$3.3V \pm 10\%$	3	3.3	3.6	V
	V_{DD_O}	$3.3V \pm 10\%$	3	3.3	3.6	
Ambient Operating Temperature Range	T_A	Commercial	0		70	°C
Crystal Resonator Frequency	f_{XIN}		5	16.667	27	MHz
Crystal Resonator Loading Capacitance	C_{XL}	As seen by an external crystal between XIN and XOUT		18		pF

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Table 5: DC Electrical Specifications

Unless otherwise stated, $V_{DD} = 3.3V$, no load on any output, and ambient temperature range $T_A = 0^\circ C$ to $70^\circ C$. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are $\pm 3\sigma$ from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS	
Overall							
Supply Current, Dynamic	I_{DD}	$f_{XIN} = 16.667MHz, f_o = 200MHz$		56		mA	
Control Inputs (SSC_0, SSC_1)							
High-Level Input Voltage	V_{IH}		2.0		$V_{DD}+0.3$	V	
Low-Level Input Voltage	V_{IL}		$V_{SS}-0.3$		0.8	V	
High-Level Input Current	I_{IH}				1	μA	
Low-Level Input Current (pull-up)	I_{IL}	$V_{IL} = 0V$		-26		μA	
Crystal Oscillator Feedback (XIN)							
Threshold Bias Voltage	V_{TH}			1.7		V	
High-Level Input Current	I_{IH}			42		μA	
Low-Level Input Current	I_{IL}			-42		μA	
Crystal Oscillator Drive (XOUT)							
High-Level Output Source Current	I_{OH}	$V_{DD} = V(XIN) = 3.3V, V_o = 0V$		-13		mA	
Low-Level Output Sink Current	I_{OL}	$V_{DD} = 3.3V, V(XIN) = 0V, V_o = 3.3V$		10		mA	
Input Loading Capacitance *	$C_{L(XOUT)}$	As seen by an external clock driver on XOUT; XIN unconnected		36		pF	
Test Input/Output (TEST_IO)							
High-Level Input Voltage	Input	V_{IH}		2.0		$V_{DD}+0.3$	V
Low-Level Input Voltage		V_{IL}		$V_{SS}-0.3$		0.8	V
High-Level Input Current		I_{IH}				1	μA
Low-Level Input Current (pull-up)		I_{IL}	$V_{IL} = 0V$		-26		μA
High-Level Output Source Current	Output	I_{OH}	$V_o = V$		-2.0		mA
Low-Level Output Sink Current		I_{OL}	$V_o = V$		2.0		mA
Tristate Output Current		I_z		-10		10	μA
Short Circuit Source Current *		I_{SCH}	$V_{DD} = 3.3V, V_o = 0V$; shorted for 30s, max.		-5.0		mA
Short Circuit Sink Current *		I_{SCL}	$V_{DD} = V_o = 3.3V$, shorted for 30s, max.		5.0		mA
LVPECL Clock Outputs (FOUPT, FOUTN)							
High-Level Output Voltage	V_{OH}	50Ω to $V_{DD,O} - 2.0V, V_{DD,O} = 3.3V$	$V_{DD,O} - 1.075$		$V_{DD,O} - 0.830$	V	
Low-Level Output Voltage	V_{OL}	50Ω to $V_{DD,O} - 2.0V, V_{DD,O} = 3.3V$	$V_{DD,O} - 1.860$		$V_{DD,O} - 1.570$	V	
Crossover Voltage	V_X	50Ω to $V_{DD,O} - 2.0V, V_{DD,O} = 3.3V$		1.92		V	
Low-Level Output Sink Current	I_{OL}	$V_o = 1.44V$				mA	
Tristate Output Current	I_z		-10		10	μA	
Short Circuit Sink Current *	I_{SCL}	$V_{DD} = V_o = 3.6V$, shorted for 30s, max.		32		mA	

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Table 6: AC Timing Specifications

Unless otherwise stated, $V_{DD} = 3.3V$, no load on any output, and ambient temperature range $T_A = 0^\circ C$ to $70^\circ C$. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are $\pm 3\sigma$ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Modulation Frequency *	f_m	Spread spectrum enabled			31.5	kHz
Modulation Index *	δ_m	Spread spectrum enabled	0		-0.5	%
Clock Stabilization Time *	t_{STB}	Output active from power-up			3	ms
LVPECL Clock Outputs (FOU_{TP}, FOU_{TN})						
Duty Cycle *		Ratio of high pulse width to one clock period, measured at V_X	45	49	55	%
Jitter, Cycle-to-Cycle (peak-peak)*	$t_{j(CC)}$	From rising edge to the next rising edge at V_X	-50		+50	ps
Rise Time *	t_r	20% to 80%, 50Ω to $V_{DD,O} - 2.0V$		420		ps
Fall Time *	t_f	80% to 20%, 50Ω to $V_{DD,O} - 2.0V$		440		ps

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4.0 Package Information

Table 7: 28-pin SOIC (0.300") Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.0926	0.1043	2.35	2.65
A1	0.0040	0.0118	0.10	0.30
b	0.0130	0.0200	0.33	0.51
C	0.0091	0.0125	0.23	0.32
D	0.6969	0.7125	17.70	18.10
E	0.2914	0.2992	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
h	0.010	0.029	0.25	0.75
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Table 8: 28-pin SOIC (0.300") Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	Θ_{JA}	Air flow = 0 m/s, single-layer PCB	77	°C/W
Lead Inductance, Self	L_{11}	Corner lead, plus wire	5.914	nH
		Center lead, plus wire	2.187	
Lead Inductance, Mutual	L_{12}	Corner lead plus wire, to first adjacent lead	2.240	nH
		Center lead plus wire, to first adjacent lead	0.647	
	L_{13}	Corner lead plus wire, to next adjacent lead	1.108	
		Center lead plus wire, to next adjacent lead	0.366	
Lead Capacitance, Bulk	C_{11}	Any corner lead plus wire to V_{SS}	1.173	pF
		Any center lead plus wire to V_{SS}	0.419	
Lead Capacitance, Mutual	C_{12}	Any corner lead plus wire to first adjacent lead	0.463	pF
		Any center lead plus wire to first adjacent lead	0.084	
	C_{13}	Any corner lead plus wire to next adjacent lead	0.045	
		Any center lead plus wire to next adjacent lead	0.013	

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5.0 Ordering Information

5.1 Device Ordering Codes

DEVICE NUMBER	FONT	ORDERING CODE	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
FS61429	-01	13715-101	28-pin (0.300") SOIC (Small Outline Package)	0° C to 70° C (Commercial)	Tape-and-Reel

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American Microsystems, Inc., 2300 Buckskin Rd., Pocatello, ID 83201, (208) 233-4690, FAX (208) 234-6796, WWW Address: <http://www.amis.com> E-mail: tgp@amis.com

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