DG408/409
8-Channel/Dual 4-Channel High Performance CMOS Analog Multiplexers

Siliconix incorporated

FEATURES

- Low $r_{DS(ON)}$ (100 Ω max)
- low Charge Injection (Q < 20 pC typ.)
- Fast Transition Time (250 ns max)
- Low Power (I_{SUPPLY} <75 μA)
- Single Supply Capability

BENEFITS

- Reduced Switching Errors
- Reduced Glitching
- Improved Data Throughput
- Reduced Power Consumption
- Increased Ruggedness

APPLICATIONS

- Data Acquisition Systems
- Audio Signal Routing and Multiplexing/Demultiplexing
- ATE Systems
- Battery Operated Systems
- High Rel Systems
- Single Supply Systems

DESCRIPTION

The DG408 is an 8-channel single-ended analog multiplexer designed to connect 1 of 8 inputs to a common output as determined by a 3-bit binary address (A_0, A_1, A_2). The DG409 is a 4-channel differential analog multiplexer designed to connect 1 of 4 differential inputs to a common dual output as determined by its 2-bit binary address (A_0, A_1). Break-before-make switching action protects against momentary crosstalk between adjacent channels.

An ON channel conducts current equally well in both directions. In the OFF state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches OFF for stacking several devices. All control inputs, address (A_x) and enable (EN) are TTL compatible over the full specified operating temperature range.

Applications for the DG408/409 include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

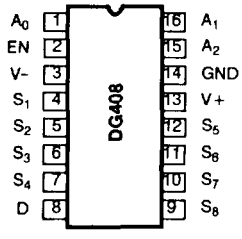
Designed in the 44 V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 volts. Additionally, single supply operation is also allowed. An epitaxial layer prevents latchup.

Both DG408 and DG409 are available in dual-in-line ceramic and plastic packages with small outline for surface mount applications, and are specified for operation over the military, A suffix (-55 to 125°C) and industrial, D suffix (-40 to 85°C) temperature ranges.

For additional information please see App Note AN89-1 and Technical Article TA89-2.

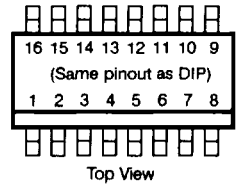
PIN CONFIGURATION

Dual-In-Line Package
Top View



Order Numbers:
CerDIP: DG408AK
DG408AK/883
Plastic: DG408DJ

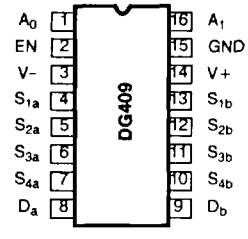
Narrow Body
SO Package



Top View

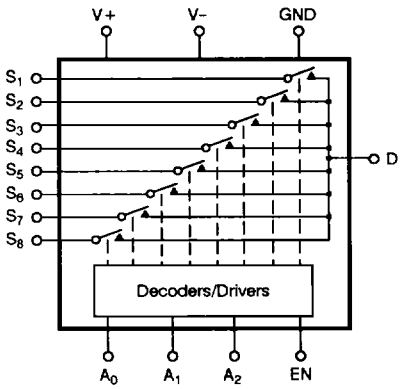
Order Number:
DG408DY
DG409DY

Dual-In-Line Package
Top View

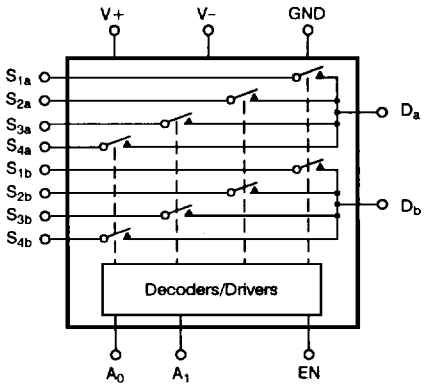


Order Numbers:
CerDIP: DG409AK
DG409AK/883
Plastic: DG409DJ

FUNCTIONAL BLOCK DIAGRAM



DG408
8-Channel Single Ended Multiplexer



DG409
Differential 4-Channel Multiplexer

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ ..... 44 V
GND ..... 25 V
Digital Inputs[h], V_S, V_D ..... (V-) -2 V to (V+) +2 V or 20 mA, whichever occurs first.
Current (Any Terminal, Except S or D) ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 40 mA
Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C
Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C

Power Dissipation (Package)*
16-Pin Ceramic DIP** ..... 900 mW
16-Pin Plastic DIP*** ..... 450 mW
16-Pin Narrow Body SO**** ..... 600 mW

*All leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C.
***Derate 6 mW/°C above 75°C.
****Derate 7.6 mW/°C above 75°C.

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SPECIFICATIONS[a]

PARAMETER		SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_{AL} = 0.8 V, V_{AH} = 2.4 V		TEMP[i]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH											
Analog Signal Range[c]		V_{ANALOG}			Full		-15	15	-15	15	V
Drain-Source ON-Resistance[e]		$r_{DS(ON)}$	V_D = ±10 V I_S = -10 mA		Room Full	40		100 125		100 125	Ω
$r_{DS(ON)}$ Matching Between Channels[f]		$\Delta r_{DS(ON)}$	V_D = 10 V, -10 V		Room			15		15	
Source OFF Leakage Current		$I_{S(OFF)}$	V_{EN} = 0 V	V_S = ±10 V V_D = ∓10 V	Room Full		-0.5 -50	0.5 50	-0.5 -50	0.5 50	nA
Drain OFF Leakage Current	DG408	$I_{D(OFF)}$		V_D = ±10 V V_S = ∓10 V	Room Full		-1 -100	1 100	-1 -100	1 100	
	DG409			V_D = ±10 V V_S = ∓10 V	Room Full		-1 -50	1 50	-1 -50	1 50	
Drain ON Leakage Current	DG408	$I_{D(ON)}$	V_S = V_D = ±10 V Sequence Each Swtich ON		Room Full		-1 -100	1 100	-1 -100	1 100	
	DG409				Room Full		-1 -50	1 50	-1 -50	1 50	

SPECIFICATIONS[a]

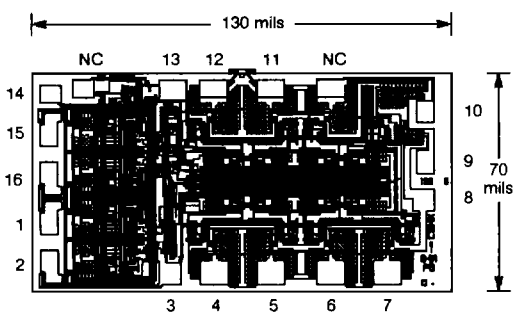
PARAMETER		SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_{AL} = 0.8 V, V_{AH} = 2.4 V	TEMP[j]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
DIGITAL CONTROL										
Logic Input Current Input Voltage High		I_{AH}	V_A = 2.4 V, 15 V	Full		-10	10	-10	10	µA
Logic Input Current Input Voltage Low		I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V	Full		-10	10	-10	10	
DYNAMIC CHARACTERISTICS										
Transition Time		t_{TRANS}	See Figure 1	Full	160		250		250	ns
Break-Before-Make Interval		t_{OPEN}	See Figure 3	Room		10		10		
Enable Turn-ON Time		$t_{ON(EN)}$	See Figure 2	Room Full	115		150 225		150	
Enable Turn-OFF Time		$t_{OFF(EN)}$		Full	105		150		150	
Charge Injection		Qi	C_L = 10 nF, V_S = 0 V	Room	20					pC
OFF Isolation[g]			V_{EN} = 0 V, R_L = 1 kΩ f = 100 kHz	Room	-75					dB
Logic Input Capacitance		C_{in}	f = 1 MHz	Room	8					
Source OFF Capacitance		$C_{S(OFF)}$	V_S = 0 V	Room	11					
Drain OFF Capacitance	DG408	$C_{D(OFF)}$	V_{EN} = 0 V f = 1 MHz, V_D = 0 V	Room	40					pF
	DG409			Room	20					
Drain ON Capacitance	DG408	$C_{D(ON)}$		Room	54					
	DG409			Room	34					
POWER SUPPLIES										
Positive Supply Current		I+	V_{EN} = 0 V, V_A = 0 V	Full			75		75	µA
Negative Supply Current		I-		Full		-75		-75		
Positive Supply Current		I+	V_{EN} = 2.4 V, V_A = 0 V	Room Full			0.5 2		0.5 2	mA
Negative Supply Current		I-		Full		-500		-500		µA

SPECIFICATIONS[a] (Single Supply)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 12 V, V- = 0 V, V_{AL} = 0.8 V, V_{AH} = 2.4 V	TEMP[i]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH									
Drain-Source ON Resistance[e]	$r_{DS(ON)}$	V_D = 3 V, 10 V, I_S = - 1 mA	Room	90					Ω
DYNAMIC CHARACTERISTICS									
Switching Time of Multiplexer	t_{TRANS}	V_{S1} = 8 V, V_{S8} = 0 V, V_{IN} = 2.4 V	Room	180					ns
Enable Turn ON Time	$t_{ON(EN)}$	V_{INH} = 2.4 V, V_{INL} = 0 V	Room	180					ns
Enable Turn OFF Time	$t_{ON(EN)}$	V_{S1} = 5 V	Room	120					ns
Charge Injection	Q	C_L = 10 nF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room	5					pC

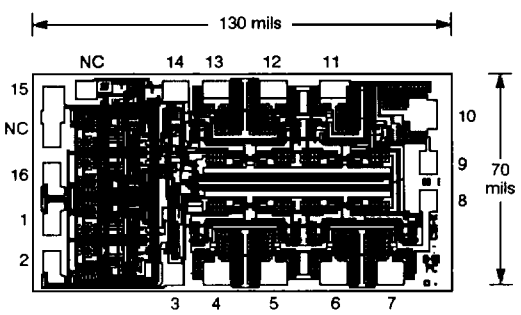
NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Sequence each switch ON.
f. $\Delta r_{DS(ON)} = r_{DS(ON)}$ MAX - $r_{DS(ON)}$ MIN
g. Worst case isolation occurs on channel 4 due to proximity to the drain pin.
h. Signals on S_X, D_X, on IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
i. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

DIE TOPOGRAPHIES



Pad No.	Function DG408	Pad No.	Function DG408
1	A_0	9	S_5
2	EN	10	S_6
3	V-	11	S_7
4	S_1	12	S_8
5	S_2	13	V+ (Substrate)
6	S_3	14	GND
7	S_4	15	A_1
8	D	16	A_2

CSHK-A **DG408**
9 Diodes
5 Resistors
8 p-Channel Enhancement MOSFET's
103 n-Channel Enhancement MOSFET's
2 NPN Bipolar Transistors



Pad No.	Function DG409	Pad No.	Function DG409
1	A_0	9	D_b
2	EN	10	S_{1b}
3	V-	11	S_{2b}
4	S_{1a}	12	S_{3b}
5	S_{2a}	13	S_{4b}
6	S_{3a}	14	V+ (Substrate)
7	S_{4a}	15	GND
8	D_a	16	A_1

CSHK-B **DG409**
9 Diodes
5 Resistors
8 p-Channel Enhancement MOSFET's
103 n-Channel Enhancement MOSFET's
2 NPN Bipolar Transistors

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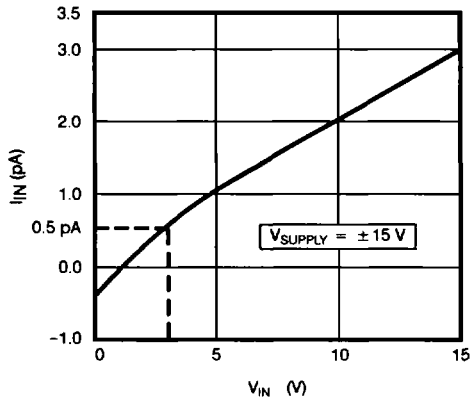
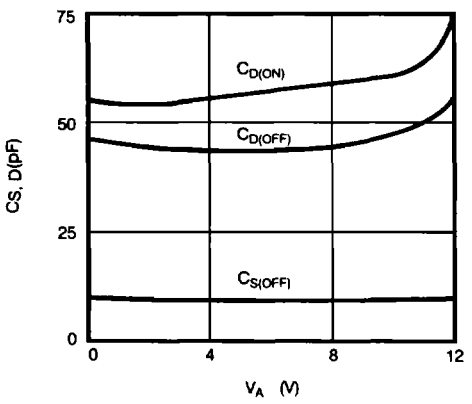
TYPICAL CHARACTERISTICS

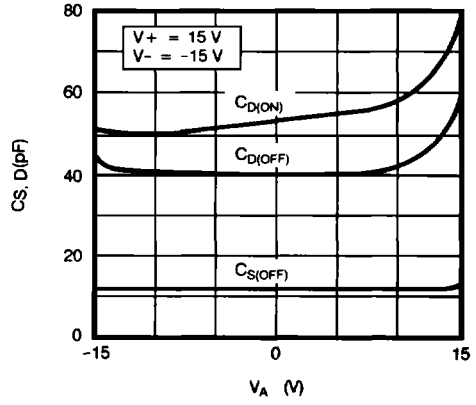
Input Logic Current vs. Logic Input Voltage



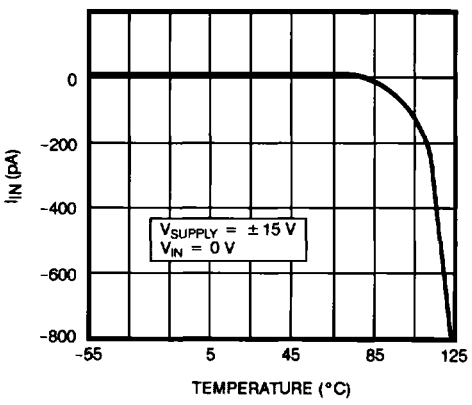
Source/Drain Capacitance vs. Analog Voltage (Single 12 V Supply)



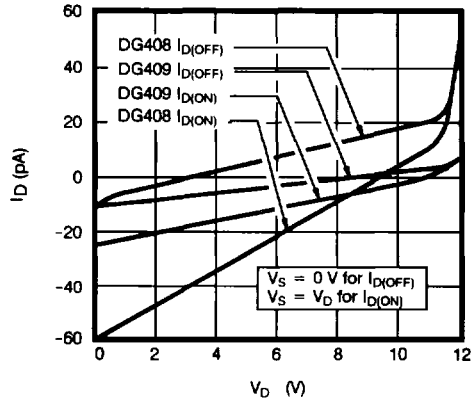
Source/Drain Capacitance vs. Analog Voltage



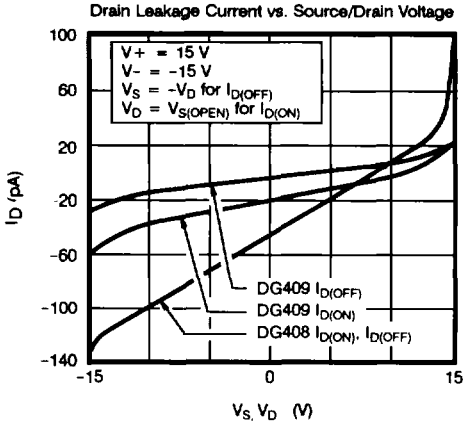
Logic Input Current vs. Temperature



Drain Leakage Current vs. Source/Drain Voltage (Single 12 V Supply)

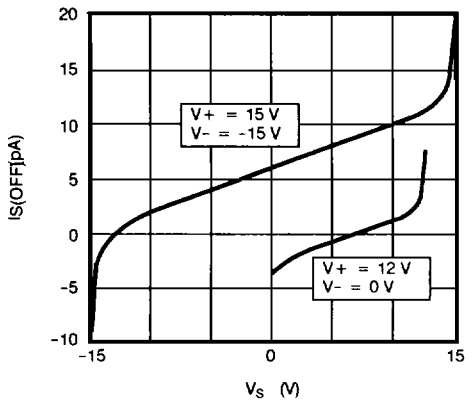


Drain Leakage Current vs. Source/Drain Voltage

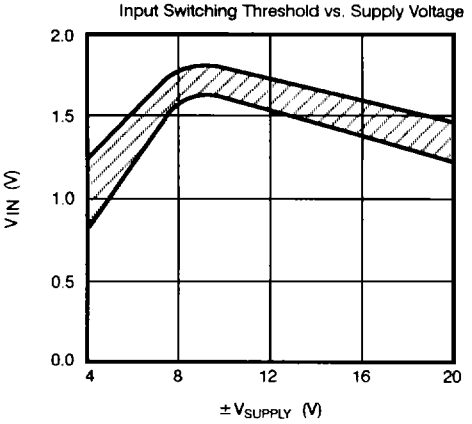


TYPICAL CHARACTERISTICS (Cont'd)

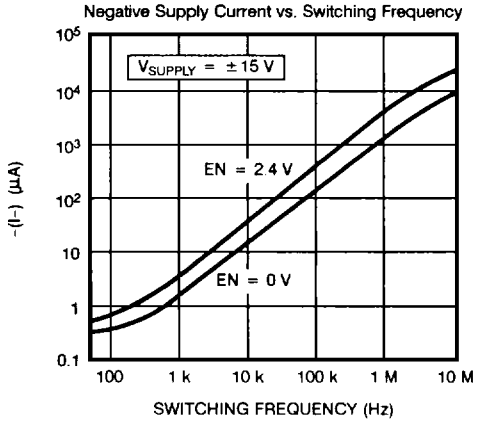
Source Leakage Current vs. Source Voltage



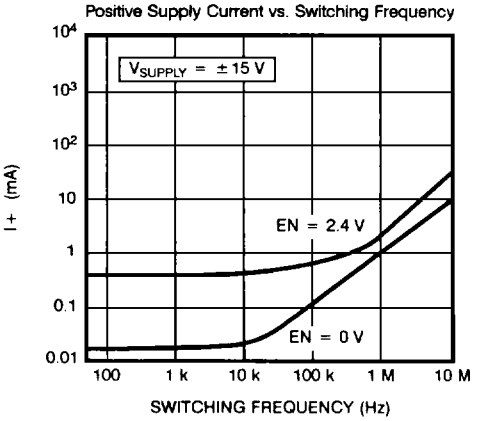
Input Switching Threshold vs. Supply Voltage



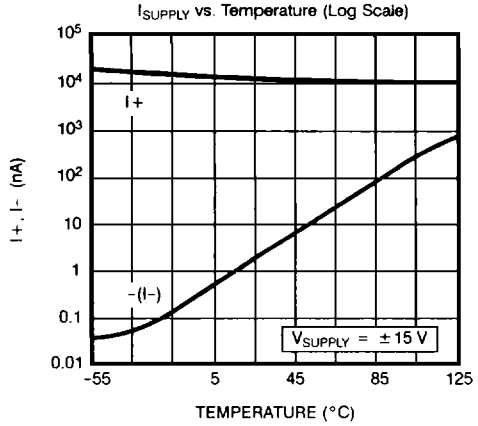
Negative Supply Current vs. Switching Frequency



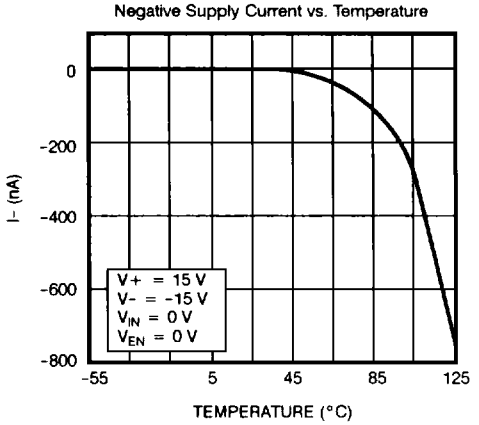
Positive Supply Current vs. Switching Frequency



ISUPPLY vs. Temperature (Log Scale)



Negative Supply Current vs. Temperature



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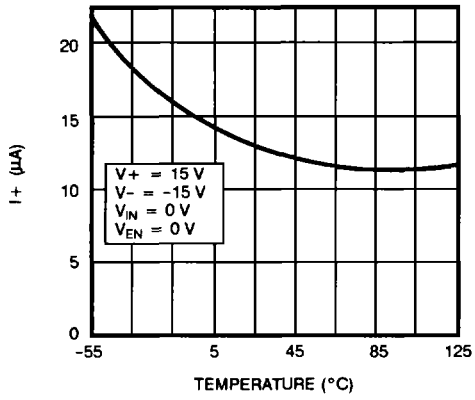
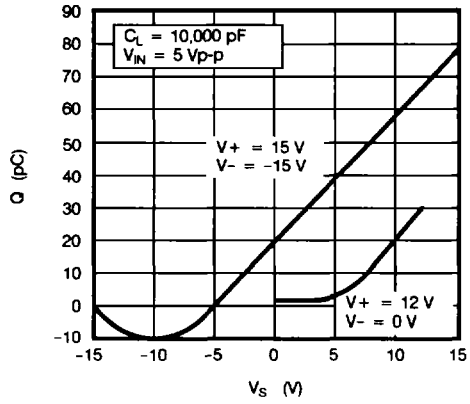
TYPICAL CHARACTERISTICS (Cont'd)

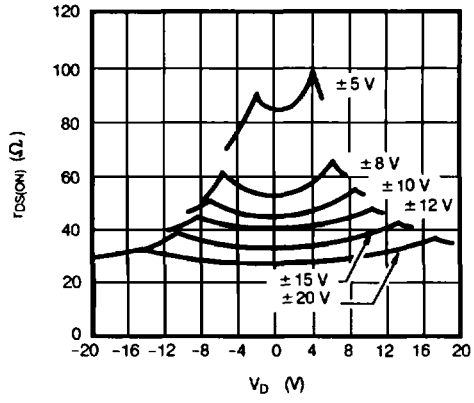
Positive Supply Current vs. Temperature
DG408



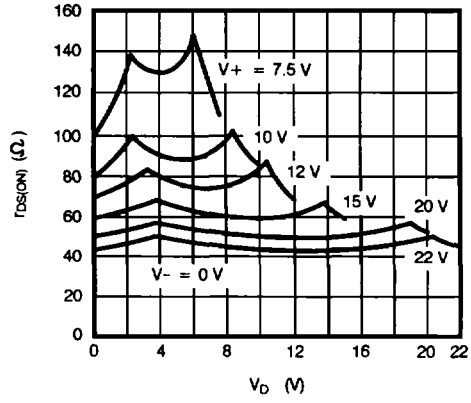
Charge Injection vs. Analog Voltage V_S
DG408/9



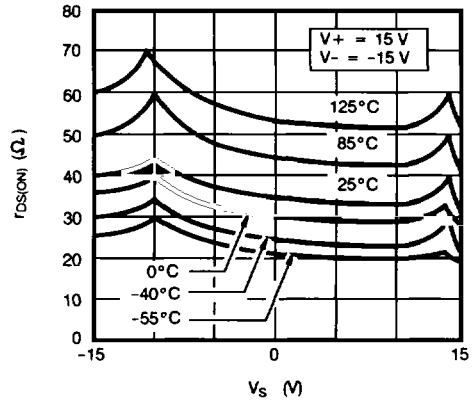
$r_{DS(ON)}$ vs. V_D and Supply



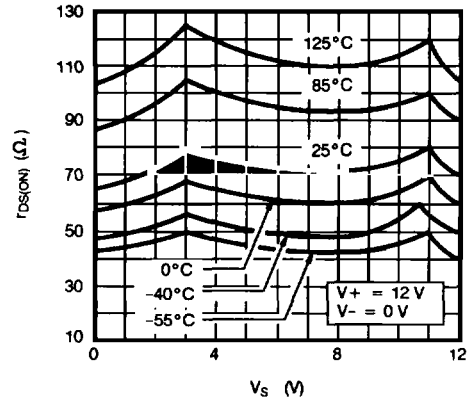
$r_{DS(ON)}$ vs. V_D (Single Supply)



$r_{DS(ON)}$ vs. V_S and Temperature

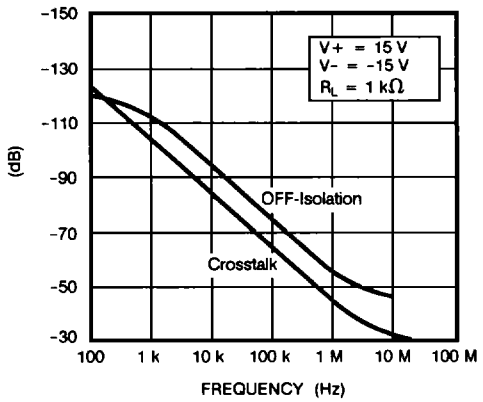


$r_{DS(ON)}$ vs. V_S and Temperature
(Single Supply)

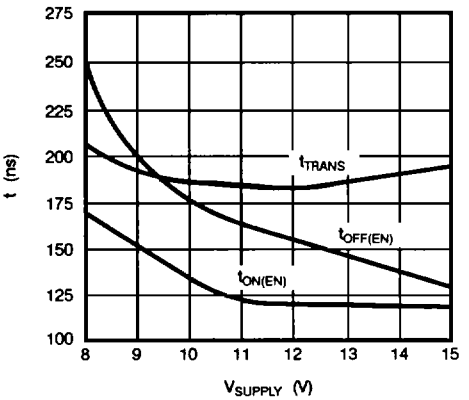


TYPICAL CHARACTERISTICS (Cont'd)

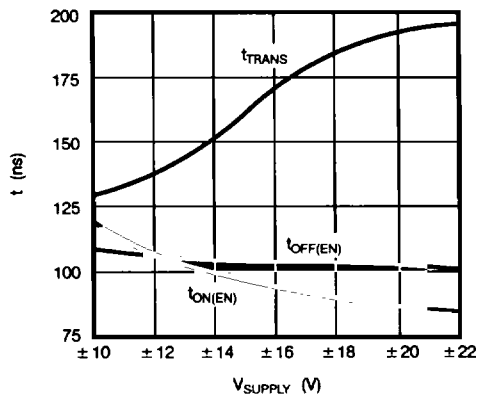
Off Isolation and Crosstalk vs. Frequency



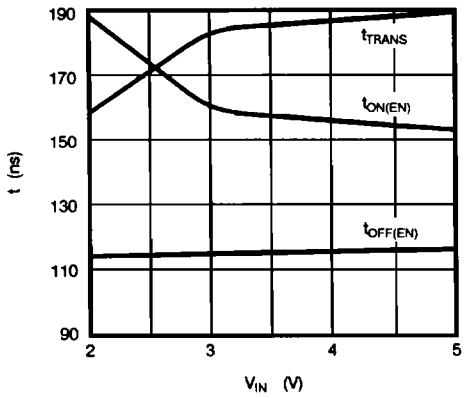
Switching Time vs. Single Supply



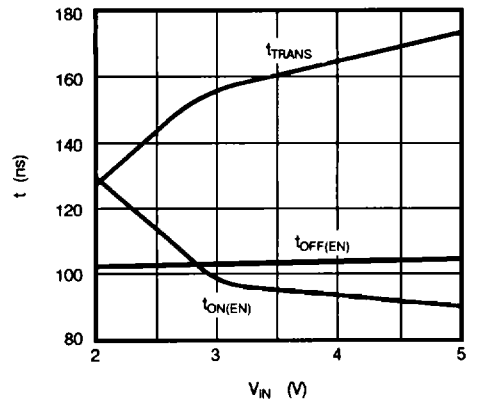
Switching Time vs. Bipolar Supply



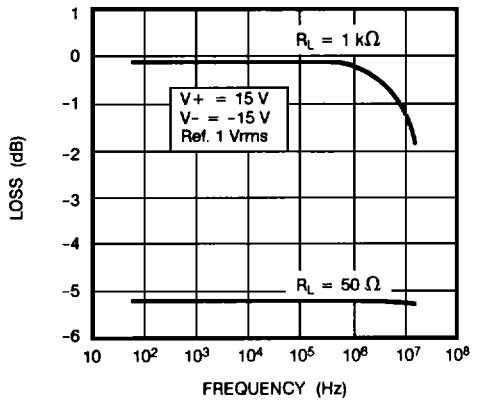
Switching Time vs. V_{IN} (Single Supply)



Switching Time vs. V_{IN} (Bipolar Supply)



Insertion Loss vs. Frequency



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TRUTH TABLES

DG408

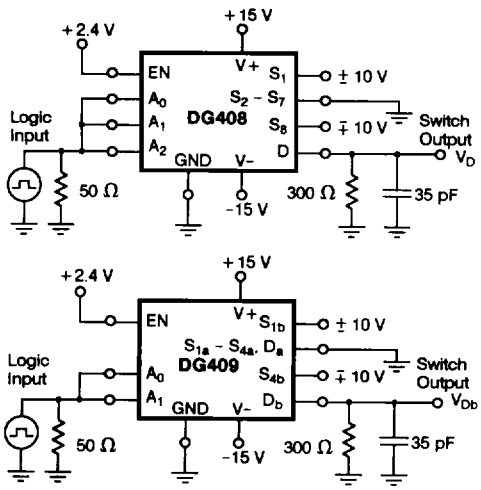
A_2	A_1	A_0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

DG409

A_1	A_0	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" $V_{AL} \leq 0.8$ V, Logic "1" $V_{AH} \geq 2.4$ V

TEST CIRCUITS



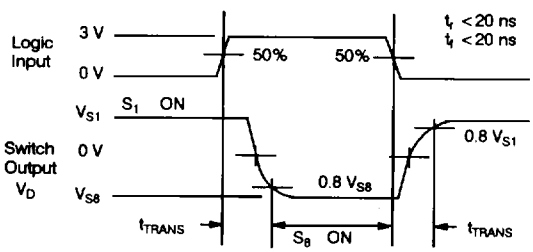


Figure 1. Transition Time

TEST CIRCUITS (Cont'd)

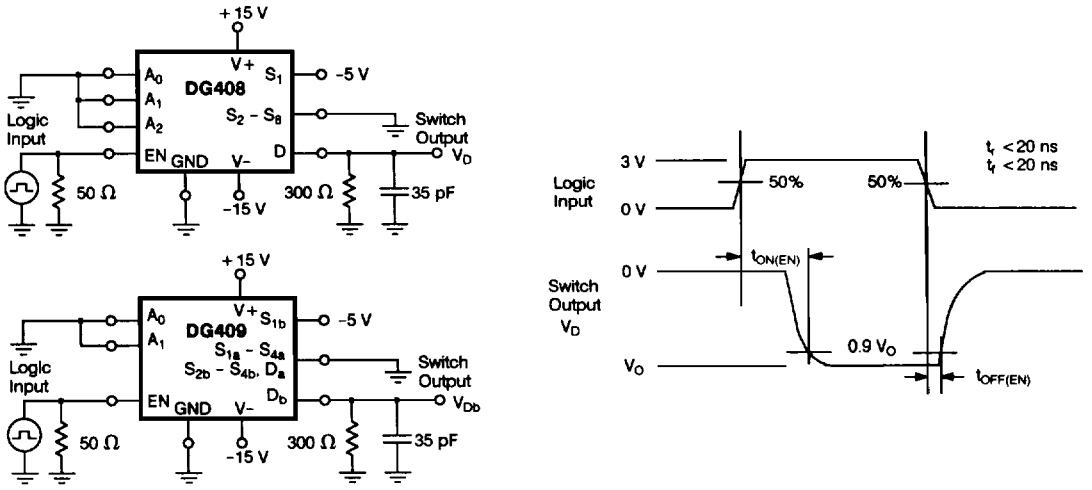


Figure 2. $t_{ON(EN)}$, $t_{OFF(EN)}$

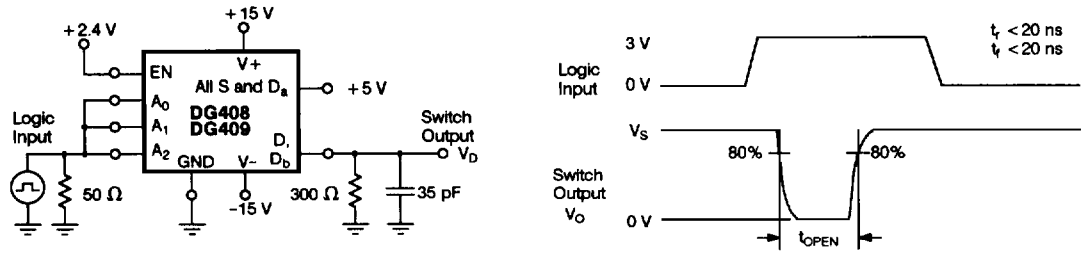


Figure 3. Break-Before-Make Interval

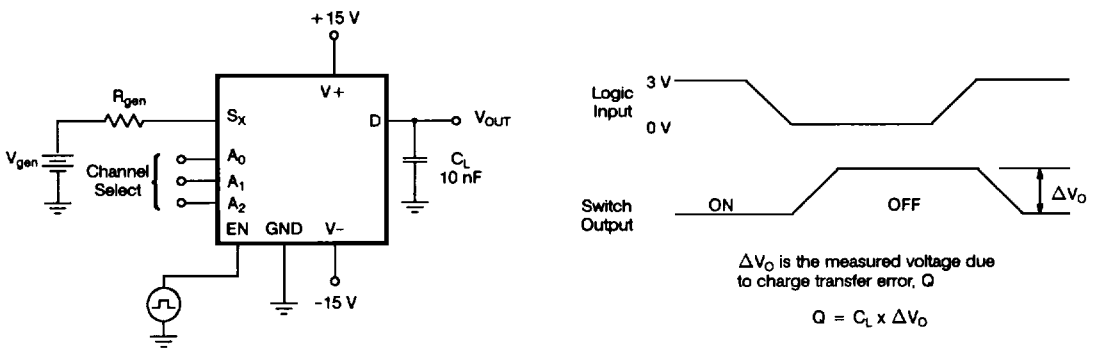


Figure 4. Charge Injection

TEST CIRCUITS (Cont'd)

Frequency Tested	Signal Generator	Analyzer
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

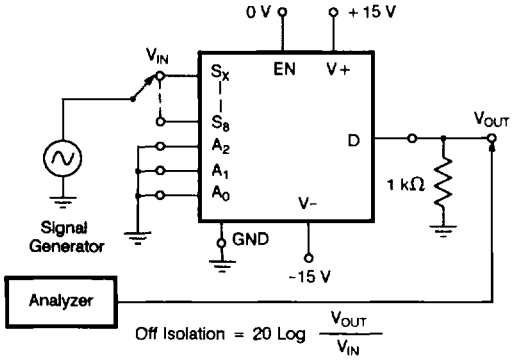


Figure 5. Off Isolation

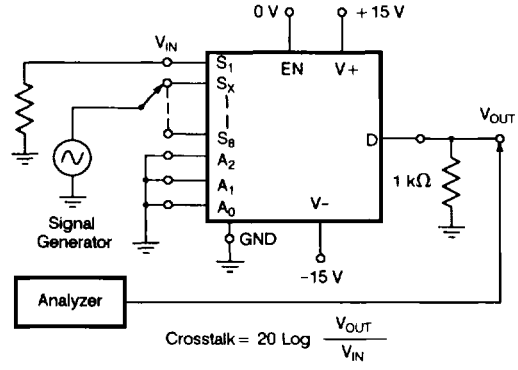


Figure 6. Crosstalk

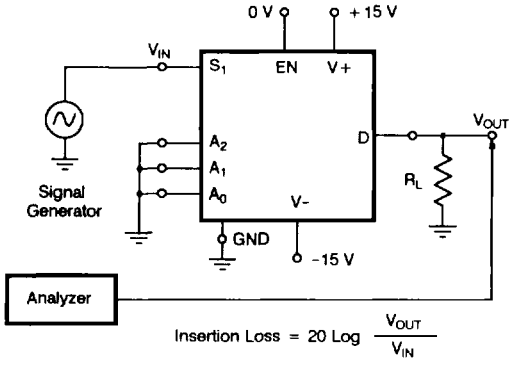


Figure 7. Insertion Loss

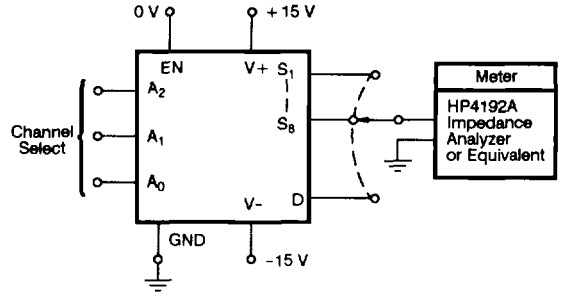


Figure 8. Source/Drain Capacitances

APPLICATION HINTS*

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V_{IN} Logic Input Voltage V_{INH} Min/V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
15**	-15	2.4/0.8	-15 to 15
12	-12	2.4/0.8	-12 to 12
12	0	2.4/0.8	0 to 12
8	-8	2.4/0.4	-8 to 8
5	-5	2.0/0.4	-5 to 5

* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
** Electrical Characteristics chart based on V+ = 15 V, V- = -15 V.

APPLICATION HINTS (Cont'd)*

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see figure). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V- value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference V_S - (V-) doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V-, but it preserves the low channel resistance and low leakage characteristics.

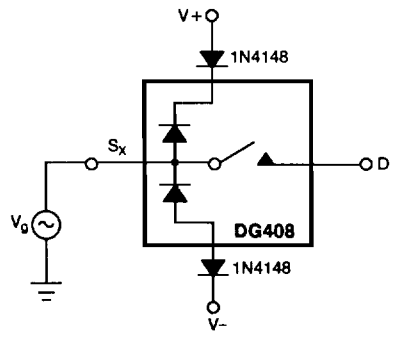
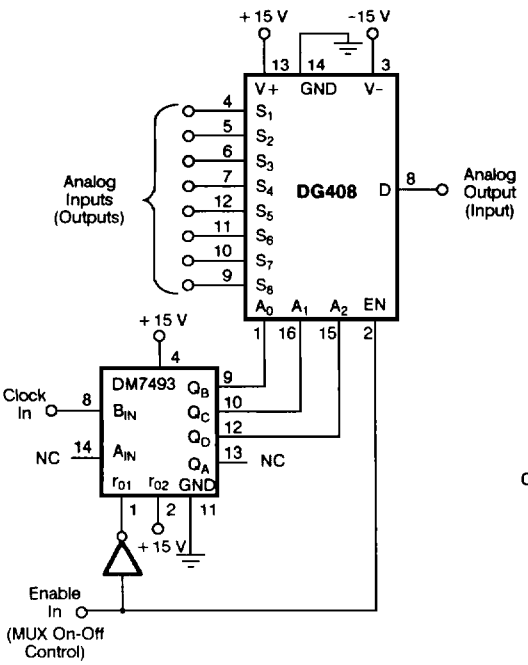


Figure 9. Overvoltage Protection Using Blocking Diodes

* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

APPLICATIONS

8-Channel Sequential Mux/Demux



Differential 4-Channel Sequential Mux/Demux

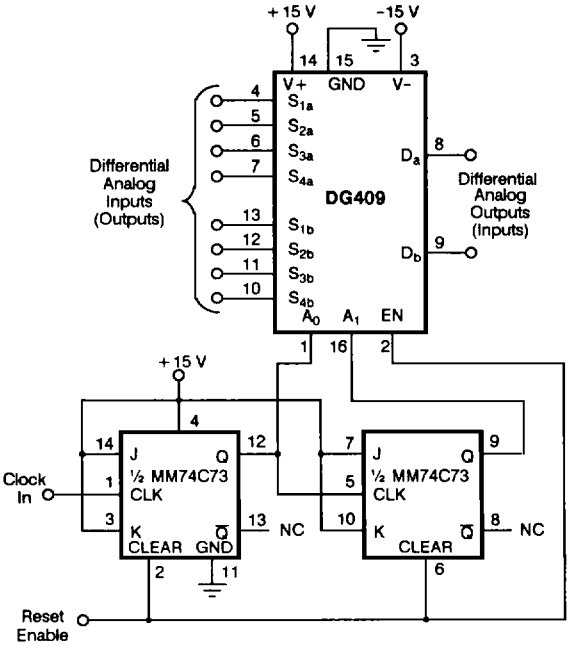


Figure 10.