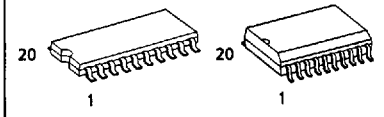
OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

The TC74VHCT373 is an advanced high speed CMOS OCTAL LATCH with 3 - STATE OUTPUT fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
This 8 - bit D - type latch is controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.
The input voltage are compatible with TTL output voltage.
This device may be used as a level converter for interfacing 3.3V to 5V system.
Input protection and output circuit ensure that 0 to 7V can be applied to the input and output pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input / output voltage such as battery back up, hot board insertion, etc.

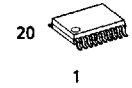
FEATURES :

- High Speed ..... t_{pd} = 7.7ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Compatible with TTL outputs .... V_{IL} = 0.8V (Max.)
  V_{IH} = 2.0V (Min.)
- Power Down Protection is provided on all inputs and outputs.
- Balanced Propagation Delays ..... $t_{pLH} \simeq t_{pHL}$
- Low Noise ..... V_{OLP} = 1.6V (Max.)
- Pin and Function Compatible with 74ALS373



F (SOP20-P-300)
Weight : 0.22g (TYP.)

FW (SOL20-P-300)
Weitht : 0.46g (TYP.)



FS (SSOP20-P-225A)
Weight : 0.09g (TYP.)

APPLICATION NOTE

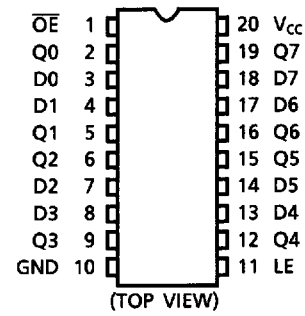
These devices can drive components with CMOS input level by adding a external pull up resistor to output terminal.

TRUTH TABLE

INPUTS			OUTPUT
$\overline{OE}$	LE	D	
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

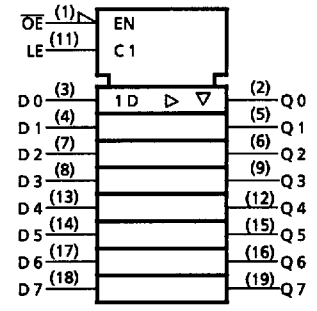
X : Don't Care
Z : High Impedance
Q_n : Q outputs are latched at the time when the LE input is taken to a low logic level.

PIN ASSIGNMENT

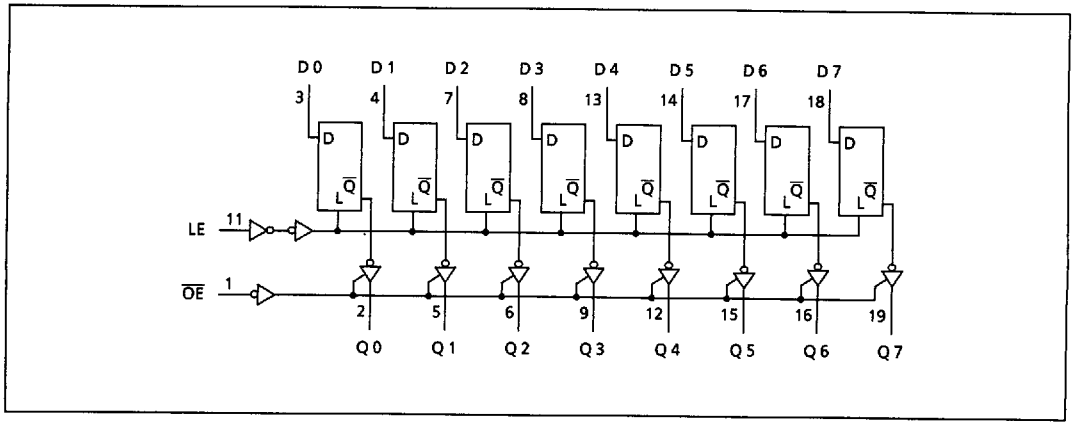


(TOP VIEW)

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~7.0	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	−20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~5.5	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~20	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITON			Ta = 25°C			Ta = −40~85°C		UNIT
				V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			4.5~5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			4.5~5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	4.5	3.15	3.65	—	3.15	—	V
			I_{OH} = −8mA	4.5	2.50	—	—	2.40	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5	—	0.0	0.10	—	0.10	V
			I_{OL} = 8mA	4.5	—	—	0.36	—	0.44	
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.25	—	±2.50	μA
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		0~5.5	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	
	I_{CCT}	PER INPUT : V_{IN} = 3.4V OTHER INPUT : V_{CC} or GND		5.5	—	—	1.35	—	1.50	mA
Output Leakage Current	I_{OPD}	V_{OUT} = 5.5V		0	—	—	+0.5	—	+5.0	μA

TIMING REQUIREMENTS (Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		Ta = −40~85°C	UNIT
			V_{CC}	TYP .	LIMIT	LIMIT	
Minimum Pulse Width (LE)	$t_{W(H)}$		5.0 ± 0.5	—	6.5	8.5	ns
Minimum Set - up Time	t_s		5.0 ± 0.5	—	1.5	1.5	
Minimum Hold Time	t_h		5.0 ± 0.5	—	3.5	3.5	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (LE-Q)	t_{pLH} t_{pHL}		5.0 ± 0.5	15	—	7.7	12.3	1.0	13.5	ns
				50	—	8.5	13.3	1.0	14.5	
Propagation Delay Time (D-Q)	t_{pLH} t_{pHL}		5.0 ± 0.5	15	—	5.1	8.5	1.0	9.5	
				50	—	5.9	9.5	1.0	10.5	
3-State Output Enable Time	t_{pZL} t_{pZH}	RL = 1kΩ	5.0 ± 0.5	15	—	6.3	10.9	1.0	12.5	
				50	—	7.1	11.9	1.0	13.5	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	RL = 1kΩ	5.0 ± 0.5	50	—	8.8	11.2	1.0	12.0	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input Capacitance	C_{IN}				—	4	10	—	10	pF
Output Capacitance	C_{OUT}				—	6	—	—	—	
Power Dissipation Capacitance	C_{PD}	(Note 2)			—	25	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per latch)}$$

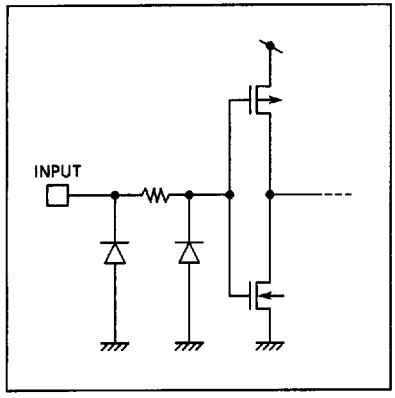
And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

$$C_{PD} \text{ (total)} = 14 + 11 \cdot n$$

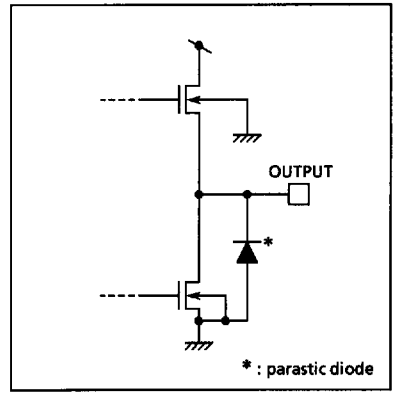
NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
			V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	C_L = 50pF	5.0	1.2	1.6	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	C_L = 50pF	5.0	−1.2	−1.6	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	C_L = 50pF	5.0	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	C_L = 50pF	5.0	—	0.8	V

INPUT EQUIVALENT CIRCUIT



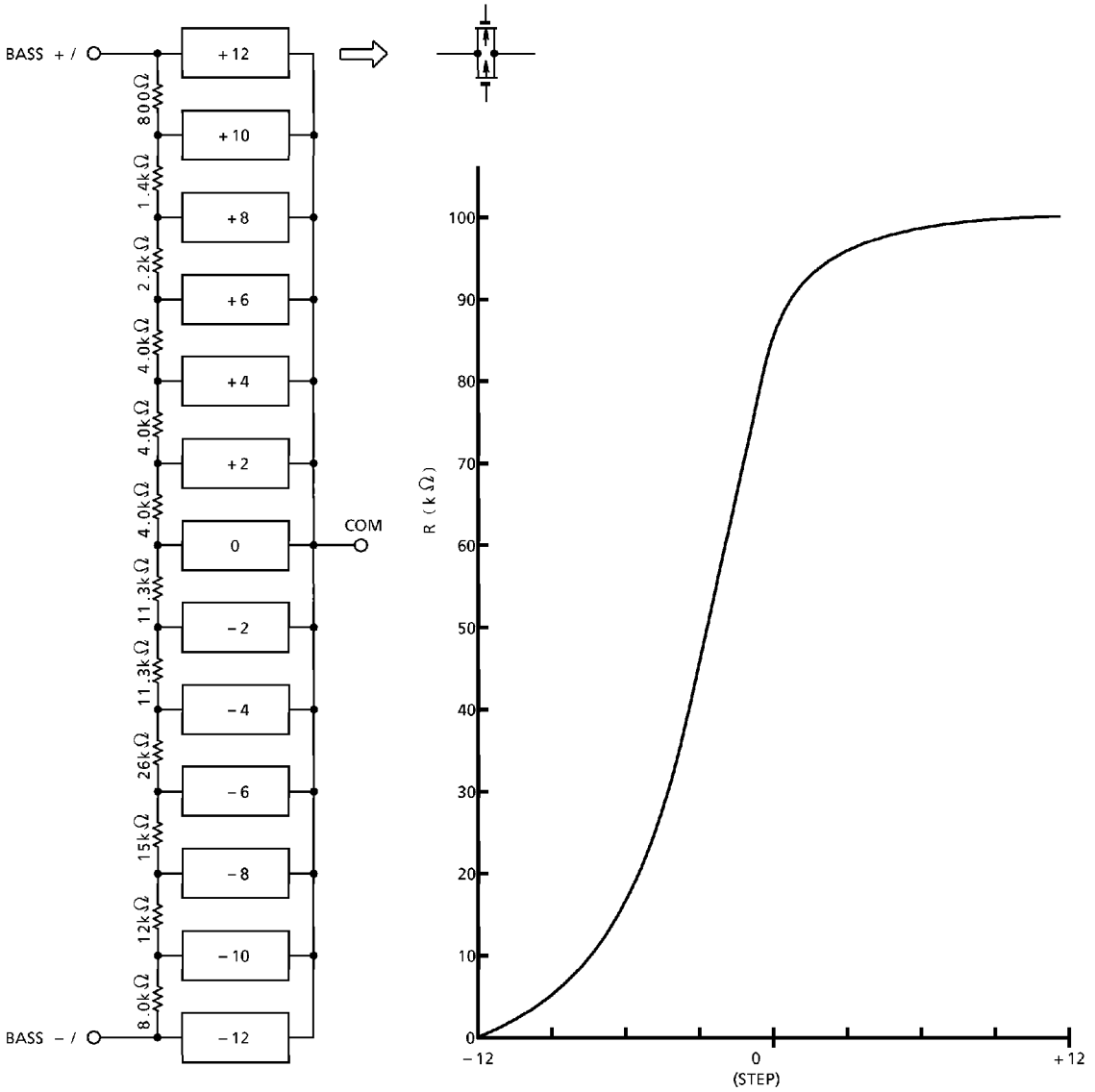
OUTPUT EQUIVALENT CIRCUIT



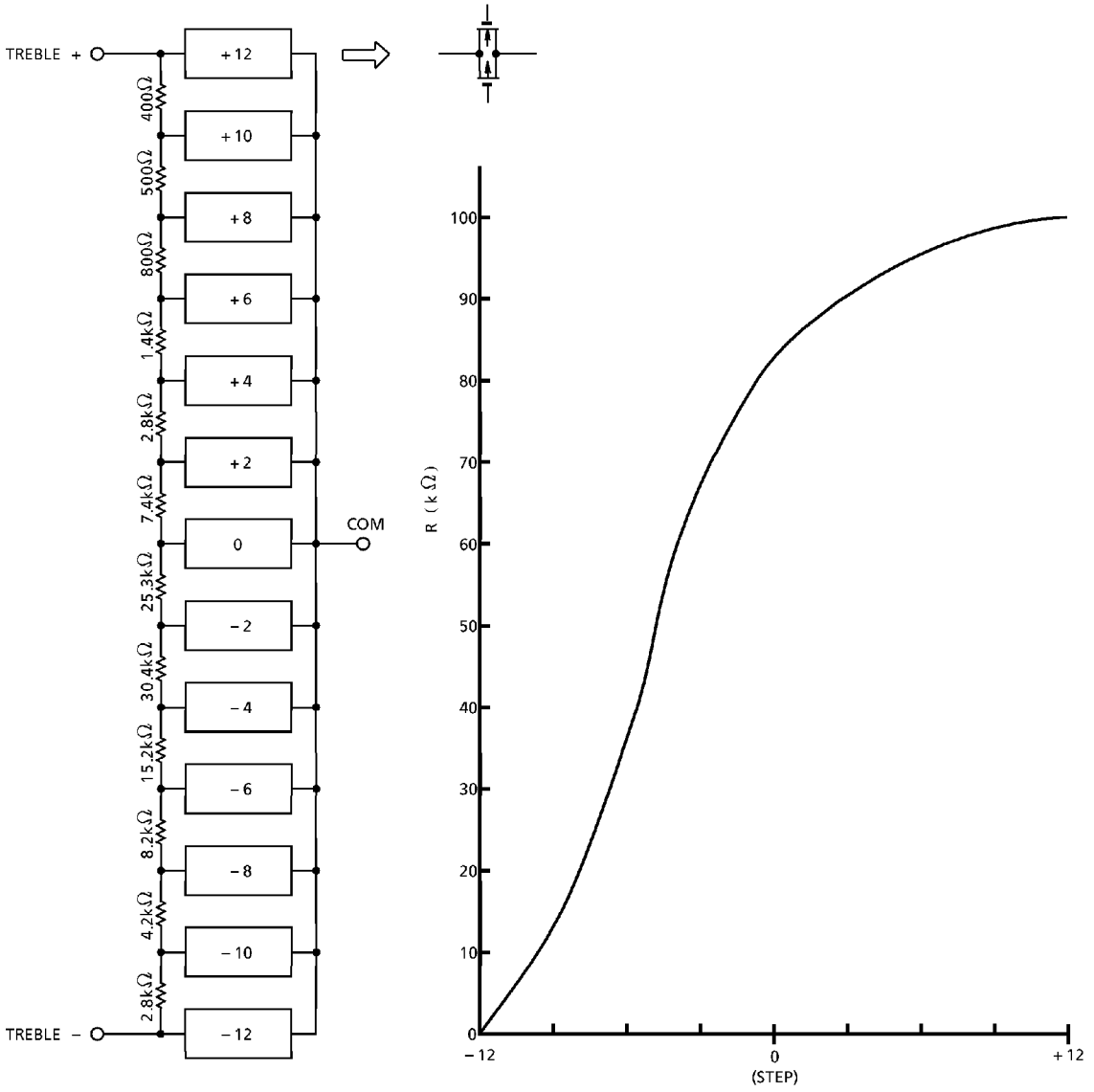
4. Variable resistance

The tone control volume consists of diffused resistors and analog switches.
Two sets of BASS / TREBLE VOLUME, in total four volumes, are built-in.

BASS Volume



TREBLE Volume



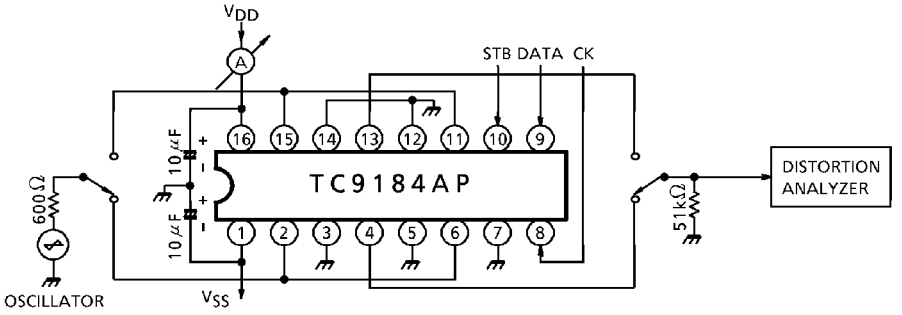
MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage (1)	V_{DD}-V_{SS}	−0.3~36	V
Power Supply Voltage (2)	V_{DD}-GND	−0.3~20	V
GND Block Input Voltage	V_{IN} (1)	−0.3~V_{DD} +0.3	V
V_{SS} Block Input Voltage	V_{IN} (2)	V_{SS} −0.3~V_{DD} +0.3	V
Power Dissipation	P_D	300	mW
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−65~150	°C

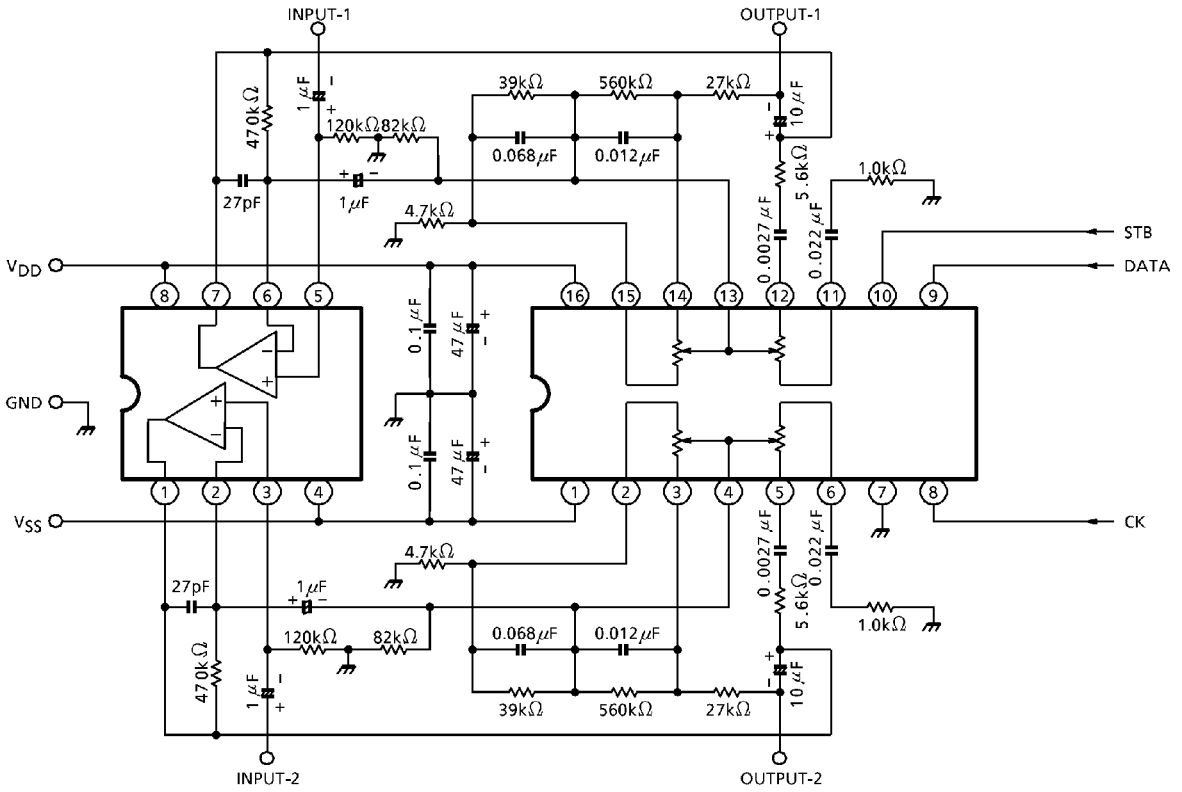
ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{DD} = 15V、V_{SS} = −15V、Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage (1)		V_{DD} − V_{SS}	—	—		12	~	34	V
Operating Supply Voltage (2)		V_{DD} − GND	—	—		6.0	~	18	V
Operating Supply Current		I_{DD}	1	No input, No load		—	0.5	1.0	mA
Input Voltage	"H" Level	V_{IH}	—	CK, DATA, STB		4.0	—	V_{DD}	V
	"L" Level	V_{IL}		V_{DD} = 6.0~18V		GND	—	1.0	
Input Current	"H" Level	I_{IH}	—	CK, DATA STB	V_{IH} = V_{DD}	−1.0	—	1.0	μA
	"L" Level	I_{IL}			V_{IL} = 0V	−1.0	—	1.0	
Volume Resistance		R	—	—		70	100	130	kΩ
Relative Resistance Error		ΔR	—	—		−5.0	—	5.0	%
Max. Input Amplitude		V_{IN}	—	—		—	—	10	V_{rms}
Max. Clock Frequency		f_{CK}	—	—		—	—	500	kHz
Min. Clock Pitch		T_{CK}	—	—		2.0	—	—	μs
Total Harmonic Distortion		THD	1	STEP = 12dB, f_{IN} = 1kHz V_{IN} = 1.0V_{p-p}		—	0.005	0.01	%

TEST CIRCUIT

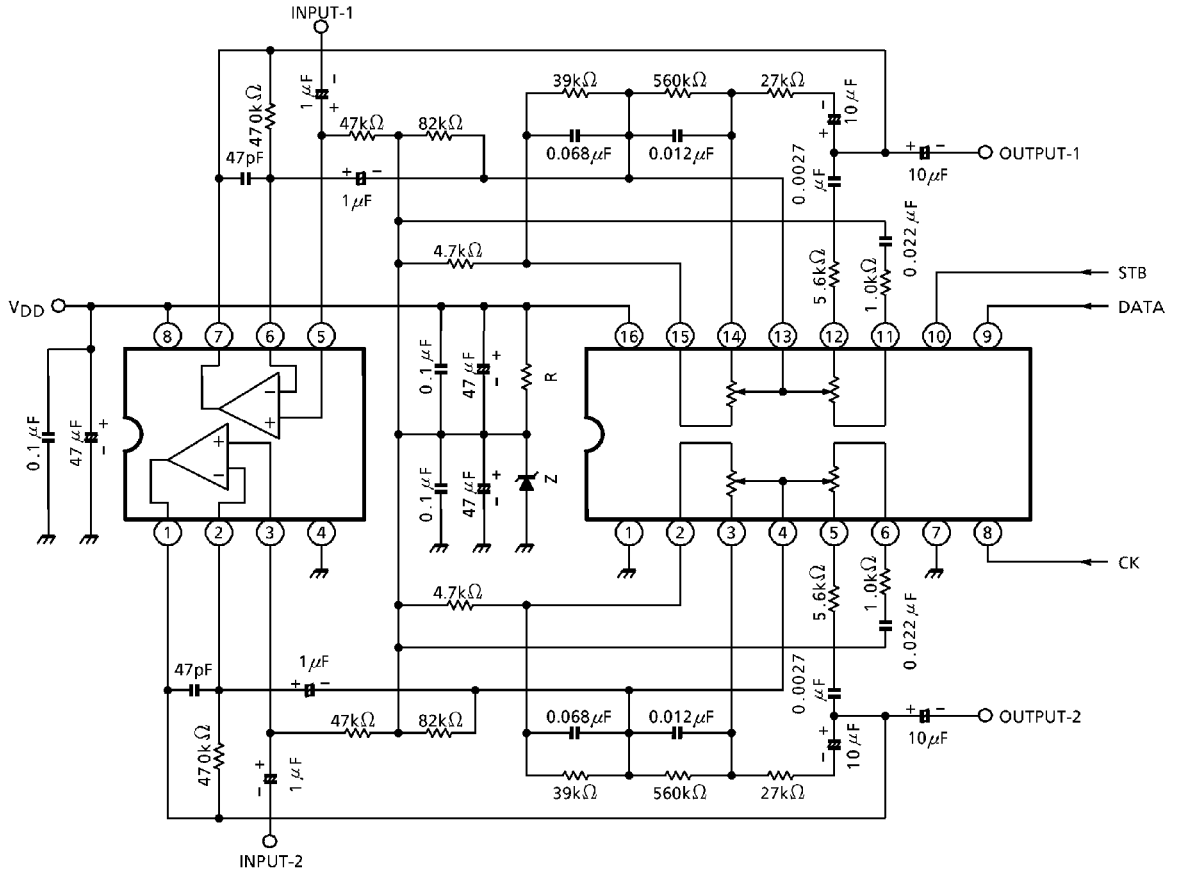


APPLICATION CIRCUIT (Dual power supply)



OP AMP : TA75558P, TA75559P or equivalent

APPLICATION CIRCUIT (Single power supply)



OP AMP : TA75558P, TA75559P or equivalent
V_Z (Zener voltage) = 1 / 2 V_{DD}