24-V Input Voltage, 150-mA, Ultralow I_Q Low-Dropout Regulators

FEATURES

- **Wide Input Voltage Range: 2.5 V to 24 V**
- **Low 3.2-μA Quiescent Current**
- **Ground Pin Current: 3.4 μA at 100-mA I_{OUT}**
- **Stable with Any Capacitor (> 0.47 μF)**
- **Available in SOT23-5 and SOT89 Packages**
- **Operating Junction Temperature: –40°C to +125°C**

APPLICATIONS

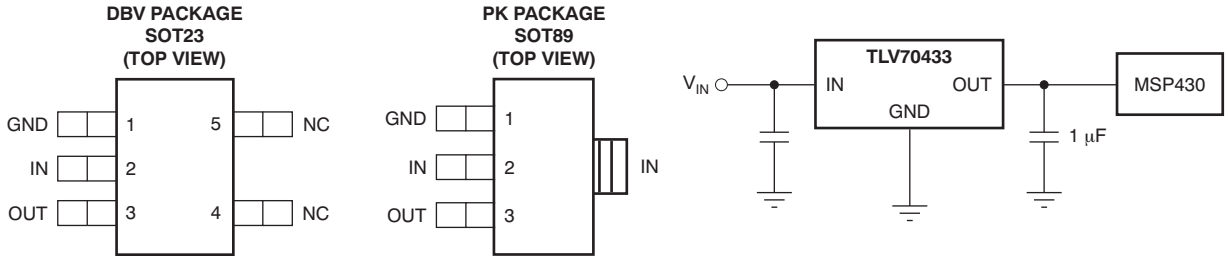
- **Ultralow Power Microcontrollers**
- **E-Meters**
- **Fire Alarms/Smoke Detector Systems**
- **Handset Peripherals**
- **Industrial/Automotive Applications**
- **Remote Controllers**
- **Zigbee™ Networks**
- **PDAs**
- **Portable, Battery-Powered Equipment**

DESCRIPTION

The TLV704xx series of low dropout (LDO) regulators are ultralow quiescent current devices designed for extremely power-sensitive applications. Quiescent current is virtually constant over the complete load current and ambient temperature range. These devices are an ideal power management attachment to low-power microcontrollers, such as the MSP430.

The TLV704xx operate over a wide operating input voltage of 2.5 V to 24 V. Thus, it is an excellent choice for both battery-powered systems as well as industrial applications that see large line transients.

The TLV704xx is available in a 3-mm × 3-mm SOT23-5 package and a 4.5-mm x 4-mm SOT89 package, both of which are ideal for cost-effective board manufacturing.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS(1)

PRODUCT	V_{OUT}
TLV704**xxyyyz**	**XX** is nominal output voltage (for example 33 = 3.3 V) **YYY** is Package Designator **Z** is Package Quantity

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	IN	–0.3	24	V
Current source	OUT	Internally limited		
Temperature	Operating junction, T_J	–40	+150	°C
	Storage, T_{stg}	–65	+150	°C
Electrostatic Discharge Rating(3)	Human body model (HBM) QSS 009-105 (JESD22-A114A)		2	kV
	Charge device model (CDM) QSS 009-147 (JESD22-C101B.01)		500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)		TLV70433PK	TLV70433DGK	UNITS
		PK	DBV	
		3 PINS	5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	119.9	213.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	145	110.9	
θ_{JB}	Junction-to-board thermal resistance	68.2	97.4	
ψ_{JT}	Junction-to-top characterization parameter	44.9	22.0	
ψ_{JB}	Junction-to-board characterization parameter	64.7	78.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	18.1	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

POWER DISSIPATION RATING TABLE

BOARD	PACKAGE	$R_{\theta JA}$	$T_A \le 25°C$ POWER RATING	$T_A = +70°C$ POWER RATING	$T_A = +85°C$ POWER RATING
High-K(1)	DBV	213.1 °C/W	470 mW	258 mW	188 mW
High-K (1)	PK	119.1 °C/W	839.6 mW	461.8 mW	335.8 mW

(1) The JEDEC High-K (2s2p) board design used to derive this data was a 3-inch × 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

All values are at T_A = +25°C, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, and C_{OUT} = 1 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLV704xx			UNIT
			MIN	TYP	MAX	
V_O	Input voltage range				24	V
	Output voltage range		1.2		5	V
V_{OUT}	DC output accuracy		–2		2	%
ΔV_O for ΔV_{IN}	Line regulation	$V_{OUT(NOM)}$ + 1 V < V_{IN} < 24 V		20	50	mV
ΔV_O for ΔI_{OUT}	Load regulation	0 mA < I_{OUT} < 10 mA		10		mV
		0 mA < I_{OUT} < 50 mA		25		mV
		0 mA < I_{OUT} < 100 mA		33	50	mV
V_{DO}	Dropout voltage(1)	I_{OUT} = 10 mA		75		mV
		I_{OUT} = 50 mA		400		mV
		I_{OUT} = 100 mA		850	1100	mV
I_{CL}	Output current limit	V_{OUT} = 0 V	160		1000	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA		3.2	4.5	µA
		I_{OUT} = 100 mA		3.4	5.5	µA
PSRR	Power-supply rejection ratio	f = 100 kHz, C_{OUT} = 10 µF		60		dB
T_J	Operating junction temperature		–40		+125	°C

(1) V_{IN} = $V_{OUT(NOM)}$ – 0.1 V.

FUNCTIONAL BLOCK DIAGRAM

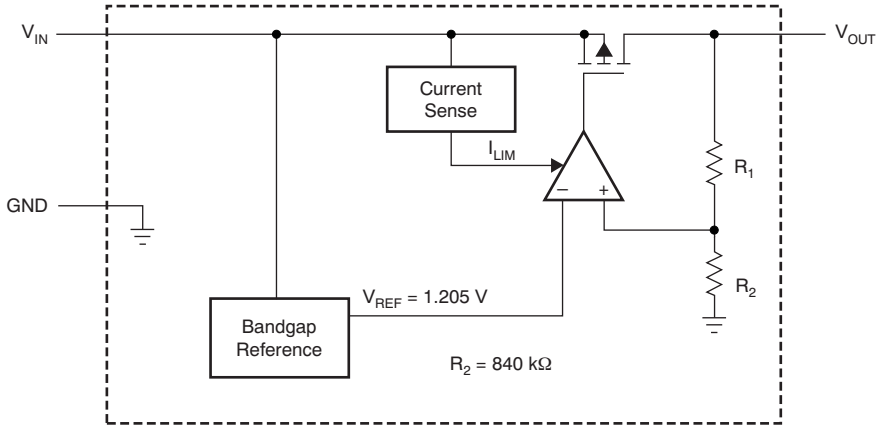


Table 1. Pin Descriptions

TLV704xx			DESCRIPTION
NAME	DBV	PK	
GND	1	1	Ground
IN	2	2, Tab	Unregulated input voltage.
OUT	3	3	Regulated output voltage. Any capacitor greater than 1 µF between this pin and ground is needed for stability.
NC	4, 5	—	No connection. This pin can be left open or tied to ground for improved thermal performance.

TYPICAL CHARACTERISTICS

LINE REGULATION

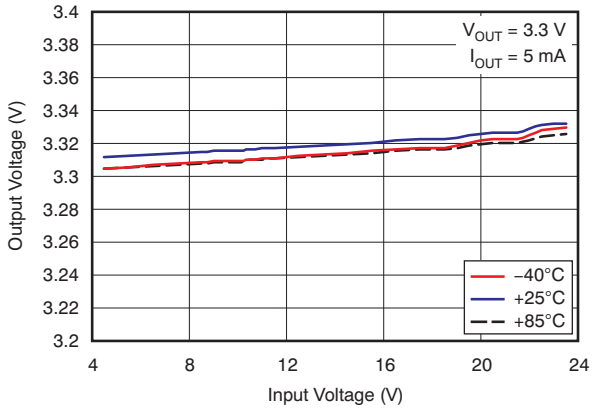


Figure 1.

LOAD REGULATION (V_{OUT} = 3.3 V)

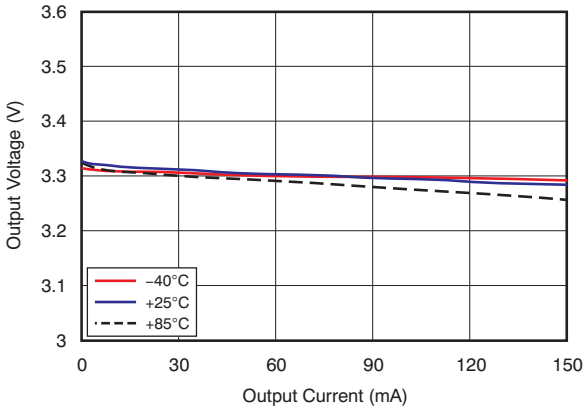


Figure 2.

OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

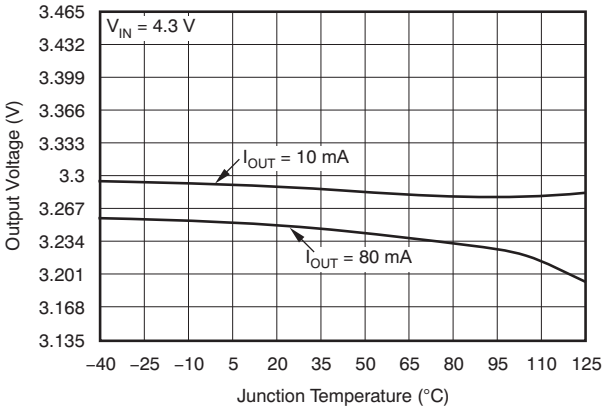


Figure 3.

DROPOUT VOLTAGE vs INPUT VOLTAGE TLV70433

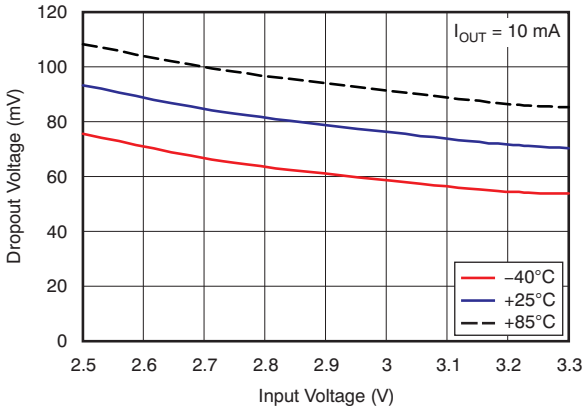


Figure 4.

DROPOUT VOLTAGE vs OUTPUT CURRENT

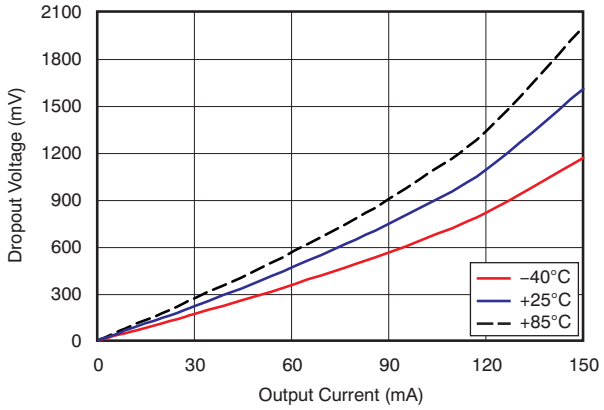


Figure 5.

GROUND CURRENT vs JUNCTION TEMPERATURE

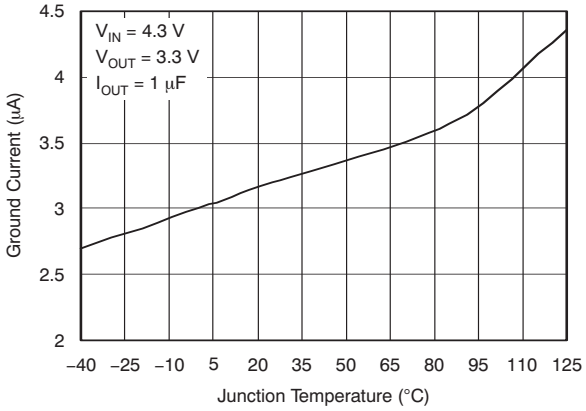


Figure 6.

TYPICAL CHARACTERISTICS (continued)

GROUND PIN CURRENT vs INPUT VOLTAGE

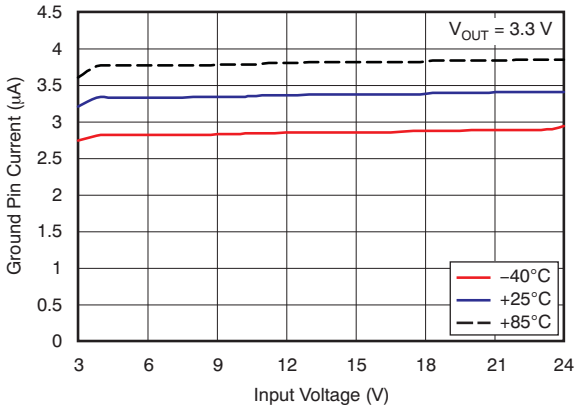


Figure 7.

GROUND PIN CURRENT vs LOAD CURRENT

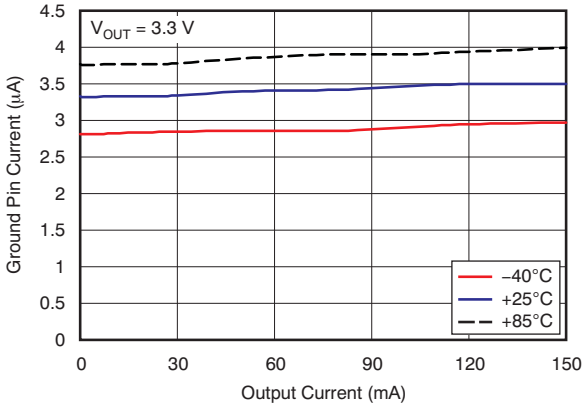


Figure 8.

CURRENT LIMIT vs JUNCTION TEMPERATURE

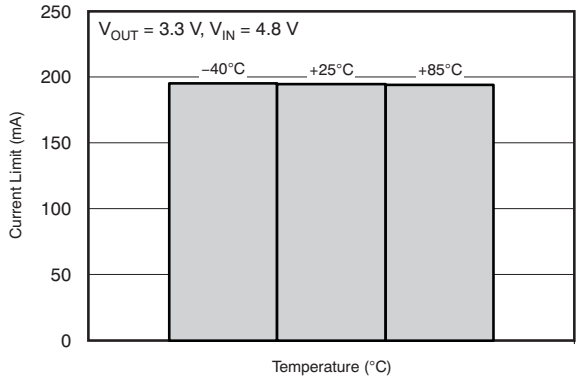


Figure 9.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

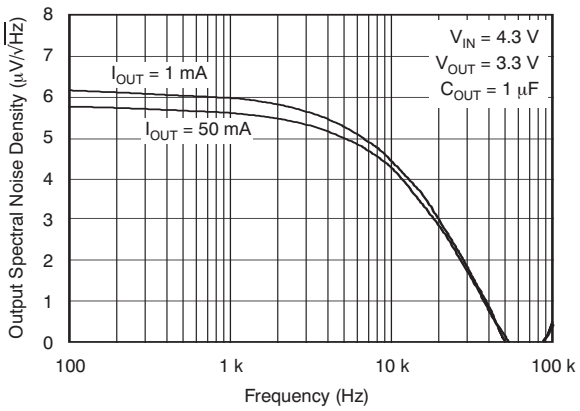


Figure 10.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

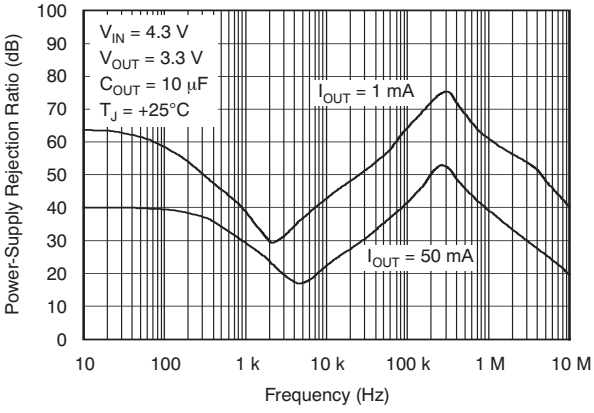


Figure 11.

POWER-UP/POWER-DOWN

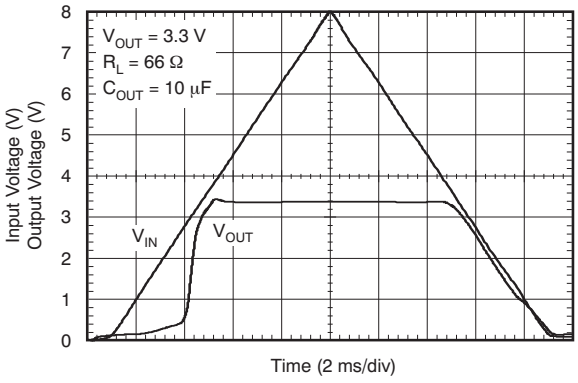


Figure 12.

TYPICAL CHARACTERISTICS (continued)

LINE TRANSIENT RESPONSE

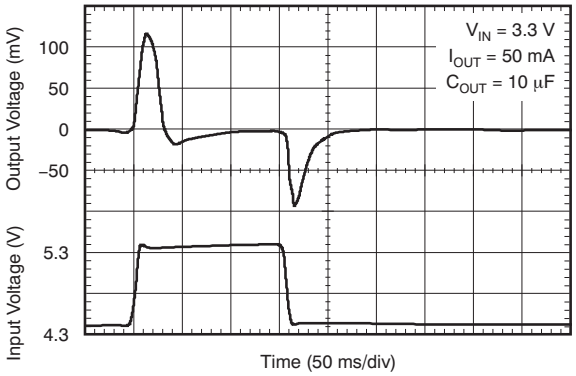


Figure 13.

LOAD TRANSIENT RESPONSE

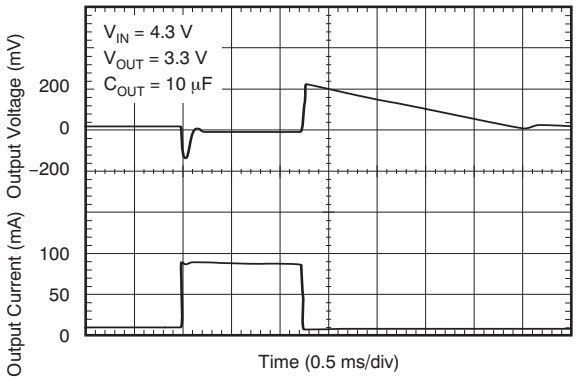


Figure 14.

APPLICATION INFORMATION

The TLV704xx series belong to a family of ultralow I_Q LDO regulators. I_Q remains fairly constant over the complete output load current and temperature range. The devices are ensured to operate over a temperature range of –40°C to +125°C.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

The TLV704 requires a 1-µF or larger capacitor connected between OUT and GND for stability. Ceramic or tantalum capacitors can be used. Larger value capacitors result in better transient and noise performance.

Although an input capacitor is not required for stability, when a 0.1-µF or larger capacitor is placed between IN and GND, it counteracts reactive input sources and improves transient and noise performance. Higher value capacitors are necessary if large, fast rise time load transients are anticipated.

BOARD LAYOUT RECOMMENDATIONS

Input and output capacitors should be placed as close to the device pins as possible. To avoid interference of noise and ripple on the board, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the device GND pin. In addition, the ground connection for the output capacitor should be connected directly to the device GND pin.

POWER DISSIPATION AND JUNCTION TEMPERATURE

To ensure reliable operation, worst-case junction temperature should not exceed +125°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum power dissipation limit is determined using Equation 1:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (1)$$

where:

- $T_J$max is the maximum allowable junction temperature.
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the Power Dissipation Rating table).
- T_A is the ambient temperature.

The regulator dissipation is calculated using Equation 2:

$$P_D = \left(V_{IN} - V_{OUT}\right) \times I_{OUT} \quad (2)$$

Power dissipation resulting from quiescent current is negligible.

REGULATOR PROTECTION

The TLV704xx series of LDO regulators use a PMOS-pass transistor that has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

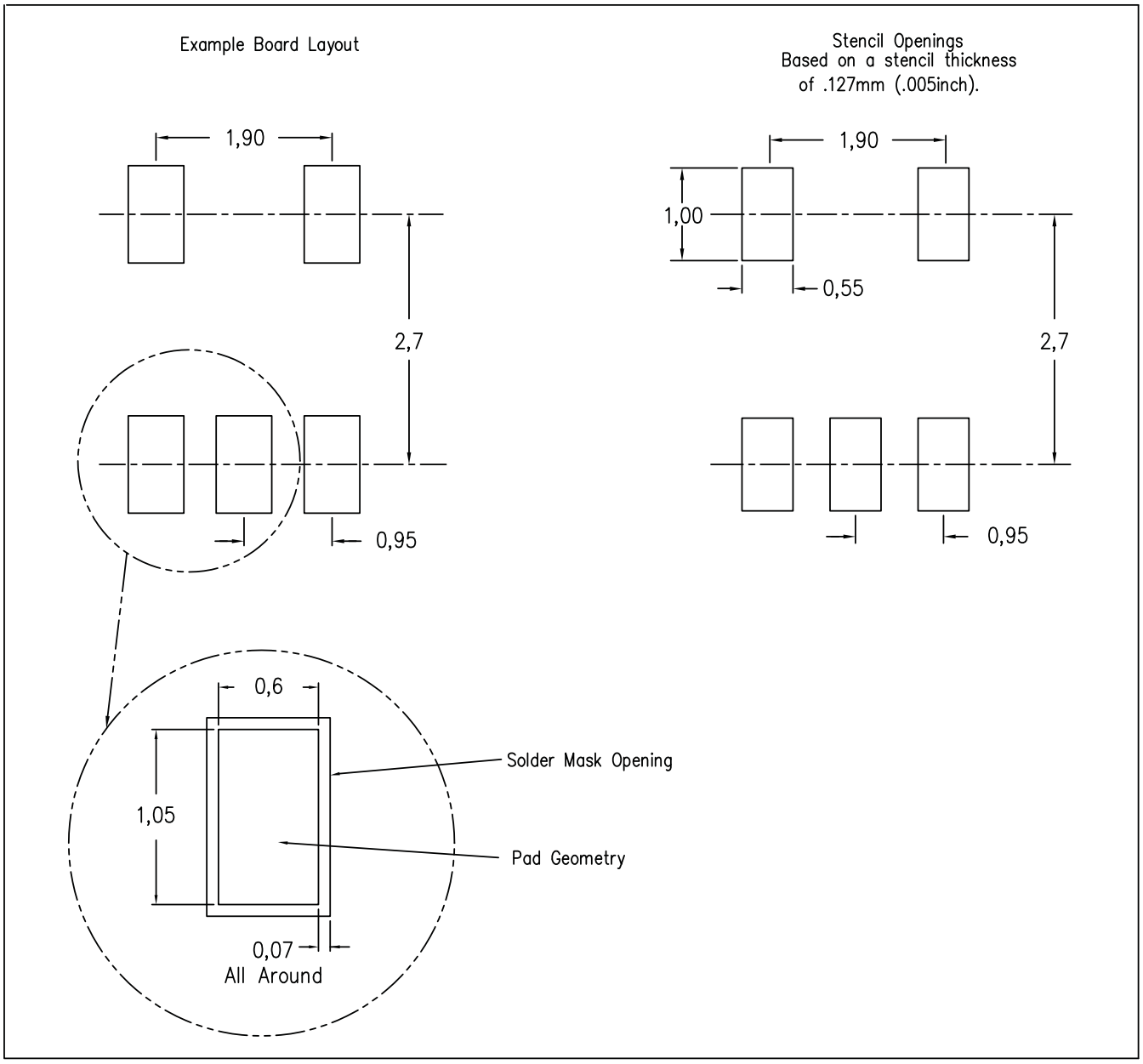
The TLV704xx features internal current limiting. During normal operation, the TLV704xx limits output current to approximately 250 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. Take care not to exceed the rated maximum operating junction temperature of +125°C. Continuously running the device under conditions where the junction temperature exceeds +125°C degrades device reliability.

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC high-K boards are given in the Power Dissipation Rating table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness. Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 2.

PACKAGE MOUNTING

Solder pad footprint recommendations for the TLV704xx are available from the Texas Instruments web site at www.ti.com through the TLV704 series product folders. The recommended land pattern for the DBV and PK packages are shown in Figure 15 and Figure 16, respectively.

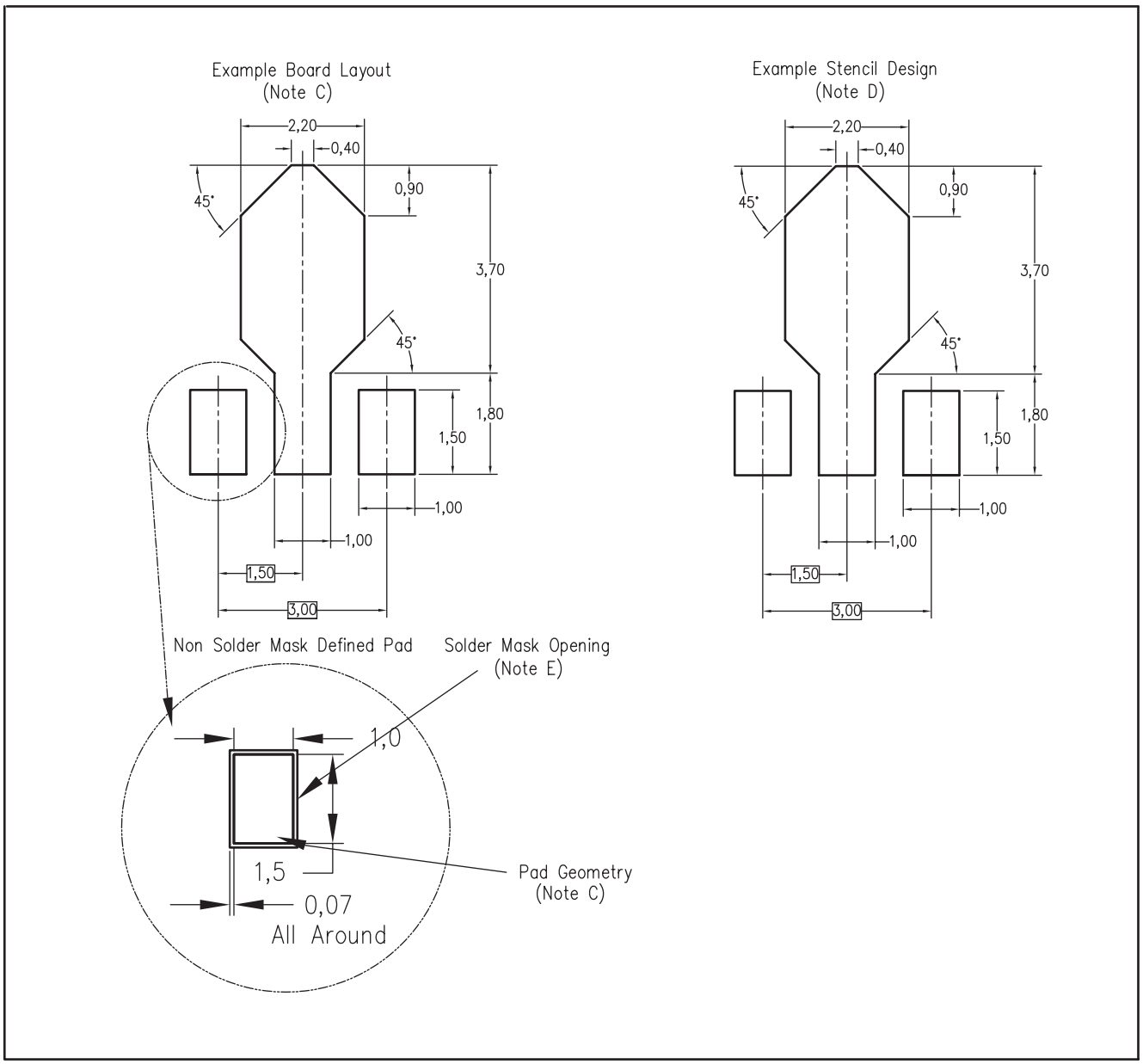
DBV (R-PDSO-G5)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

Figure 15. DBV (SOT23-5) Land Pad Pattern Drawing

PK (R–PDSO–G3)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

Figure 16. PK (SOT89) Land Pad Pattern Drawing

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October, 2010) to Revision B **Page**

- Updated document to reflect availability of PK package option 1
- Corrected typo in front-page figure 1
- Added PK package information to *Thermal Information* and *Dissipation Ratings* tables 2
- Changed *Pin Descriptions* table to correct pin numbering for PK package option 3
- Revised Typical Characteristics section; added and removed graphs 4
- Updated format of *Application Information* section 7
- Added *Package Mounting* section and Figure 16 7

Changes from Original (October, 2010) to Revision A **Page**

- Updated DBV graphic in front-page figure 1
- Updated Table 1 to reflect pin out diagram changes 3

PACKAGING INFORMATION

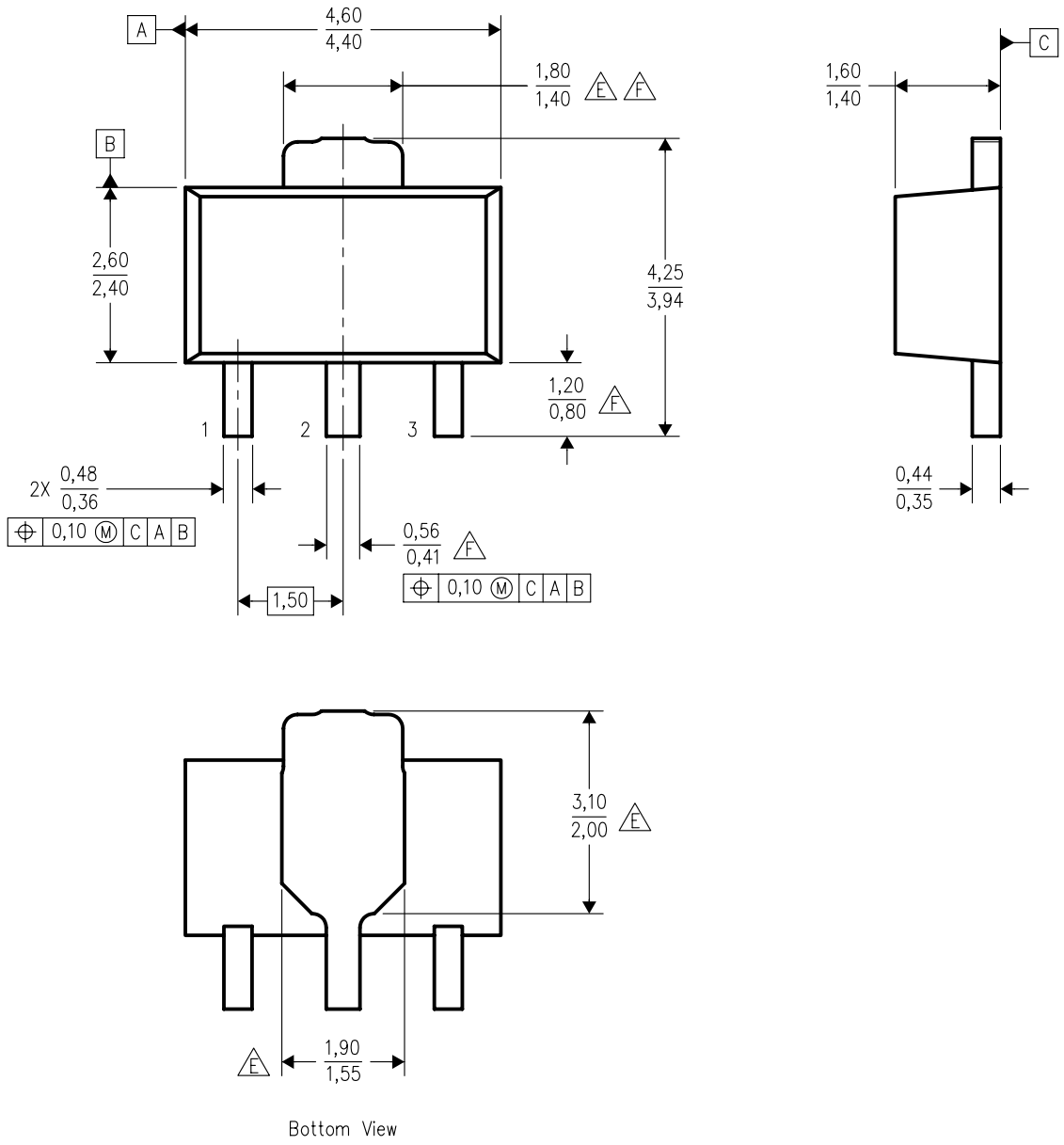
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLV70430DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TLV70430DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
TLV70430PKR	PREVIEW	SOT-89	PK	3	1000	TBD	Call TI	Call TI	Samples Not Available
TLV70430PKT	PREVIEW	SOT-89	PK	3	250	TBD	Call TI	Call TI	Samples Not Available
TLV70433DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
TLV70433DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TLV70433PKR	PREVIEW	SOT-89	PK	3	1000	TBD	Call TI	Call TI	Samples Not Available
TLV70433PKT	PREVIEW	SOT-89	PK	3	250	TBD	Call TI	Call TI	Samples Not Available
TLV70450DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
TLV70450DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

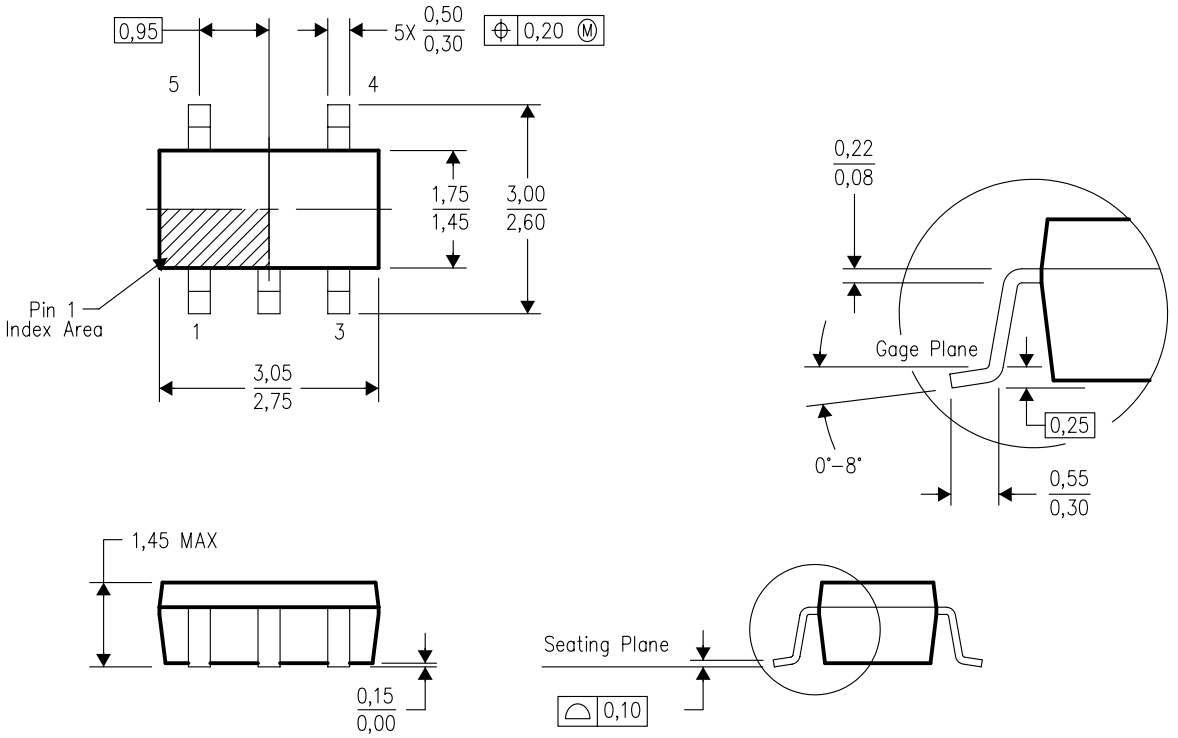
PK (R–PSSO–F3) PLASTIC SINGLE–IN–LINE PACKAGE



4040234/D 02/2006

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the tab.
D. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.15 per side.
E. Thermal pad contour optional within these dimensions.
F. Falls within JEDEC TO–243 variation AA, except minimum lead length, pin 2 minimum lead width, minimum tab width.

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

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