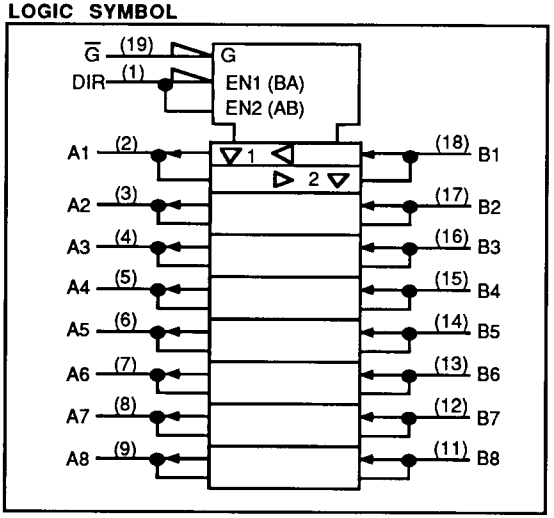
V54ACT645
V74ACT645
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

FEATURES
- CMOS Replacement for ALS
- High Speed, 5ns Typical
- TTL Levels, I_{OL}/I_{OH} = 48/24mA Commercial, 32/24mA Military
- Low Input Current, 1μA Max
- Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max Over Temperature

FUNCTIONAL DESCRIPTION
These 8-bit transceivers allow synchronous two way communication between data buses A and B. The DIR signal controls the directio nof data flow. When DIR is high, data flows from A to B. When DIR is low, data flows from B to A. The G signal enables the transceiver.

These parts are designed to interface with 3-state buses and I/O ports.

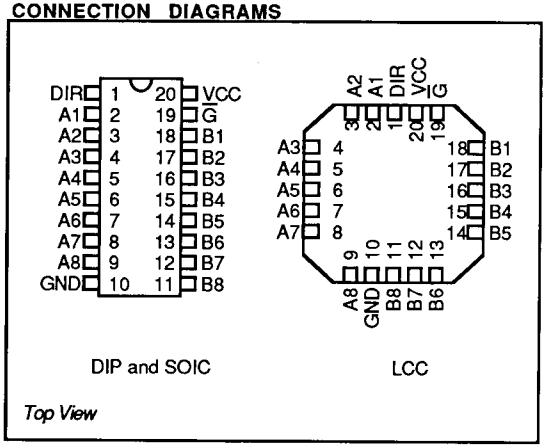
LOGIC SYMBOL



FUNCTION TABLE

ENABLE	DIRECTION CONTROL	OPERATION
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

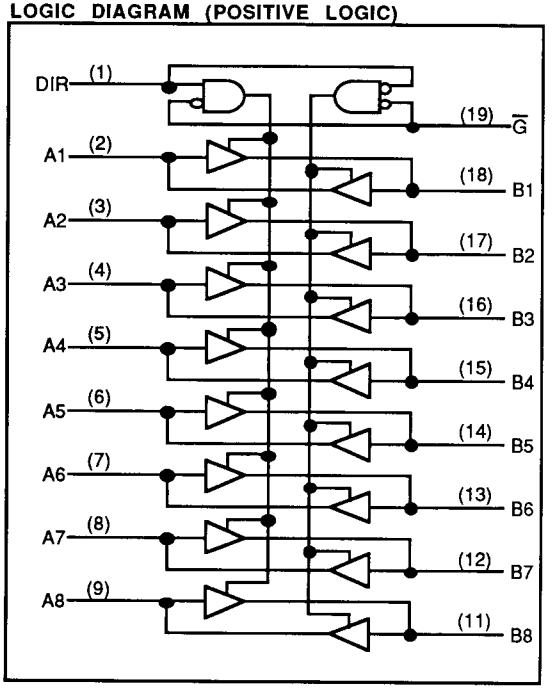
CONNECTION DIAGRAMS



DIP and SOIC LCC

Top View

LOGIC DIAGRAM (POSITIVE LOGIC)



ACT FAMILY DATA SHEETS

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r, t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC} + 5V	V_{CC} + 5V	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: **Input t_r, t_f ≤3nsec**

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC} = 5V 25°C Typ	V_{CC} = 5V ± 10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop Delay A to B or B to A	50	1	5	7	10	12	ns	3
		300	1	8	11	13	15	ns	3
t_{PHL}		50	1	5	9	12	14	ns	3
		300	1	11	15	19	22	ns	3
t_{PZH}	Prop Delay Output Enable to A or B	50	1	7	11	13	15	ns	2
		300	1	9	14	18	21	ns	2
t_{PZL}		50	1	8	12	15	17	ns	2
		300	1	12	17	21	24	ns	2
t_{PHZ}	Prop Delay Output Disable to A or B	10	1	7	9	12	14	ns	2
		50	1	7	10	13	15	ns	2
t_{PLZ}		10	1	7	9	12	14	ns	2
		50	1	7	10	13	15	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300	1	9	13	17	19	ns	4
t_{THL}		50	1	2	3	4	5	ns	4
		300	1	7	9	12	13	ns	4
C_{IN}	Input Capacitance			10	12	12	12	pF	
C_{OUT}	Output Capacitance			10	12	12	12	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			35	45	45	45	pF	

*$P_T = (C_{PD}+C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation when n = # of buffers

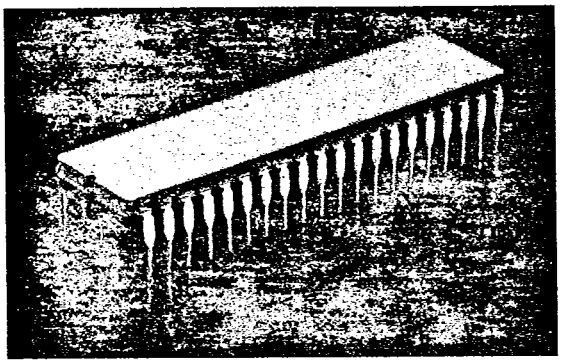
PACKAGING

T-90-20

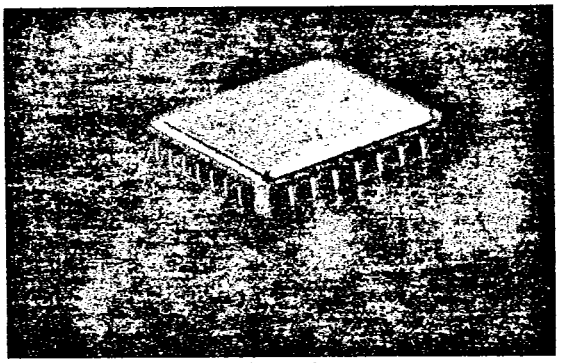
VTC offers a wide variety of industry-standard packages for its products. These include plastic and ceramic dual in-line, side brazed ceramic, plastic small outline, plastic leaded chip carrier, ceramic leadless chip carrier, surface mount plastic, ceramic flatpacks and pin grid array packages.

Pin counts to 172 pins are used in volume manufacturing and pin counts up to 300 are in development.

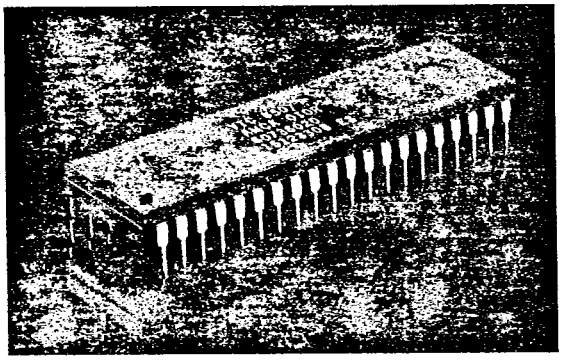
The packages dimensions given in this section are offered for VTC's advanced CMOS logic products. The ACL products are available compliant to MIL-STD-883.



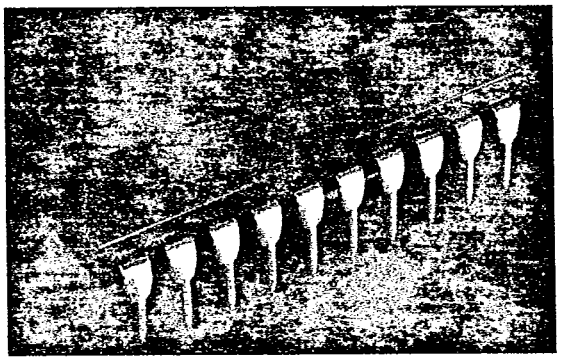
Ceramic DIP (Cerdip)



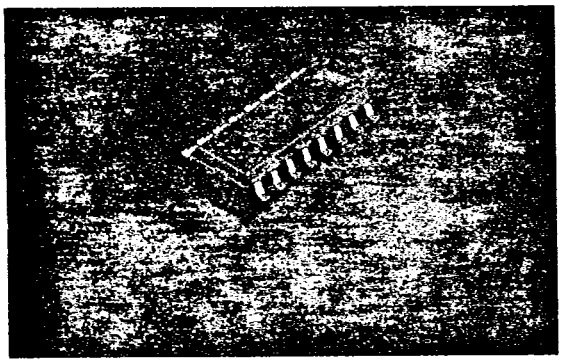
Ceramic Leadless Chip Carrier (LCC)



Plastic DIP



Plastic Slimline DIP

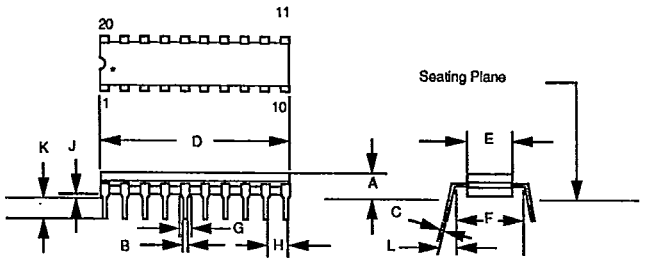


Plastic SOIC

CERAMIC DIP (CERDIP)

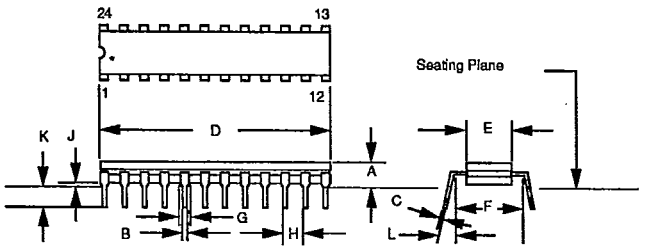
T-90-20

20 PIN CERAMIC DIP				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.155	0.200	3.94	5.08
B	0.014	0.023	0.36	0.58
C	0.008	0.015	0.20	0.38
D	0.940	0.960	23.87	24.39
E	0.220	0.300	5.59	7.62
F	0.300 BSC		7.62 BSC	
G	0.030	0.070	0.76	1.78
H	0.100 BSC		2.54 BSC	
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	0°	15°	0°	15°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

24 PIN CERAMIC DIP				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.155	0.200	3.94	5.08
B	0.014	0.023	0.36	0.58
C	0.008	0.015	0.20	0.38
D	1.150	1.350	29.21	34.29
E	0.220	0.300	5.59	7.62
F	0.300 BSC		7.62 BSC	
G	0.030	0.070	0.76	1.78
H	0.100 BSC		2.54 BSC	
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	0°	15°	0°	15°



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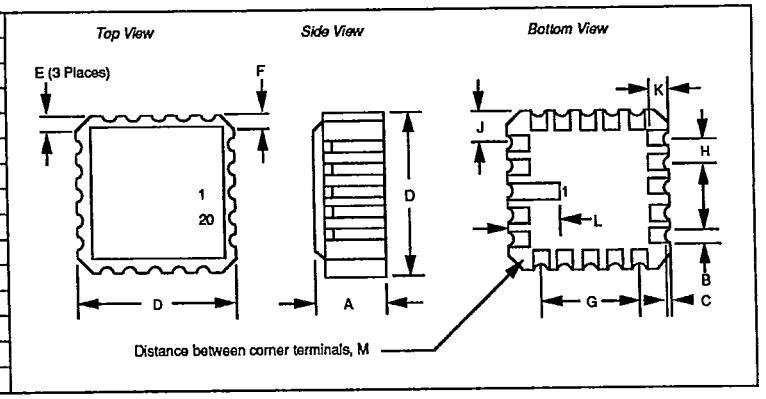
PACKAGING AND ORDERING

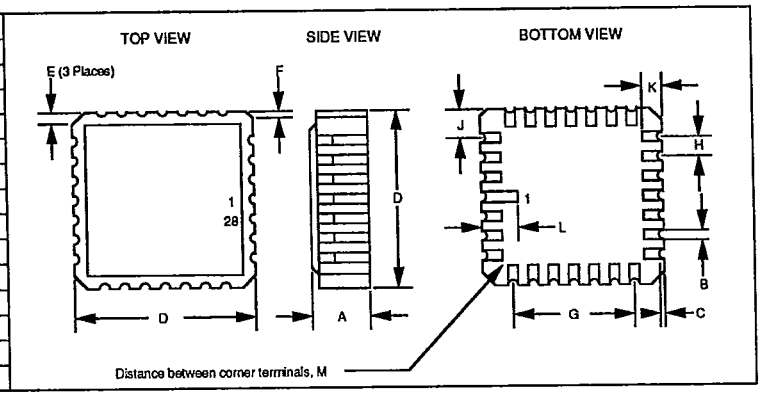
CERAMIC LEADLESS CHIP CARRIER (LCC)

T-90-20

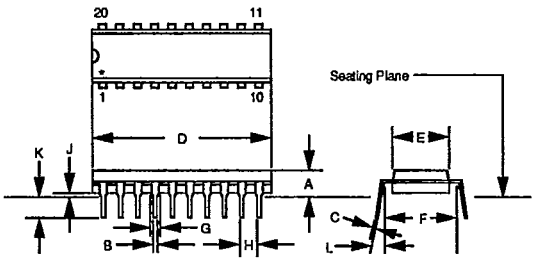
20 PIN CERAMIC LEADLESS CHIP CARRIER (LCC)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.054	0.085	1.37	2.15
B	0.022	0.028	0.55	0.71
C	0.004	0.017	0.10	0.43
D	0.345	0.356	8.76	9.04
E	0.035	0.045	0.89	1.14
F	0.015	0.025	0.38	0.63
G	0.195	0.205	4.95	5.21
H	0.045	0.055	1.14	1.39
J	0.065	0.085	1.65	2.15
K	0.045	0.055	1.14	1.39
L	0.077	0.093	1.95	2.36
M	0.015	—	0.38	—



28 PIN CERAMIC LEADLESS CHIP CARRIER (LCC)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.054	0.085	1.37	2.15
B	0.022	0.028	0.55	0.71
C	0.004	0.017	0.10	0.43
D	0.442	0.458	11.22	11.63
E	0.035	0.045	0.89	1.14
F	0.015	0.025	0.38	0.63
G	0.295	0.305	7.53	7.75
H	0.050 BSC		1.27 BSC	
J	0.065	0.085	1.65	2.15
K	0.045	0.055	1.14	1.39
L	0.077	0.093	1.95	2.36
M	0.015	—	0.38	—



20 PIN PLASTIC DIP				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	—	0.210	—	5.33
B	0.014	0.022	0.356	0.558
C	0.008	0.015	0.204	0.381
D	0.925	1.060	23.5	26.9
E	0.240	0.280	6.10	7.11
F	0.300	0.325	7.62	8.25
G	0.045	0.070	1.15	1.77
H	0.100 BSC		2.54 BSC	
J	0.015	—	0.39	—
K	0.115	0.160	2.93	4.06
L	0°	15°	0°	15°



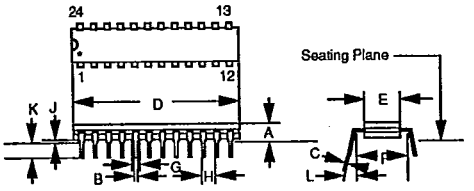
*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

PACKAGING AND ORDERING

PLASTIC SLIMLINE DIP

T-90-20

24 PIN 'SLIMLINE' PLASTIC DIP				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	—	0.210	—	5.33
B	0.014	0.022	0.356	0.558
C	0.008	0.015	0.204	0.381
D	1.125	1.275	29.3	32.3
E	0.240	0.280	6.10	7.11
F	0.300 BSC		7.62 BSC	
G	0.045	0.070	1.15	1.77
H	0.100 BSC		2.54 BSC	
J	0.015	—	0.39	—
K	0.115	0.160	2.93	4.06
L	0°	15°	0°	15°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

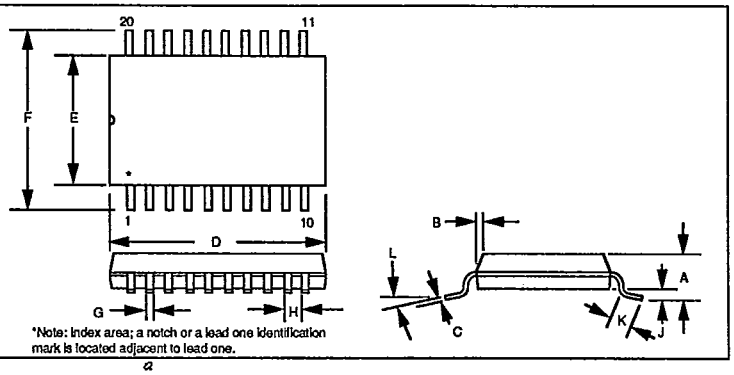
PACKAGING AND ORDERING

PLASTIC SOIC

T-90-20

20 PIN SOIC

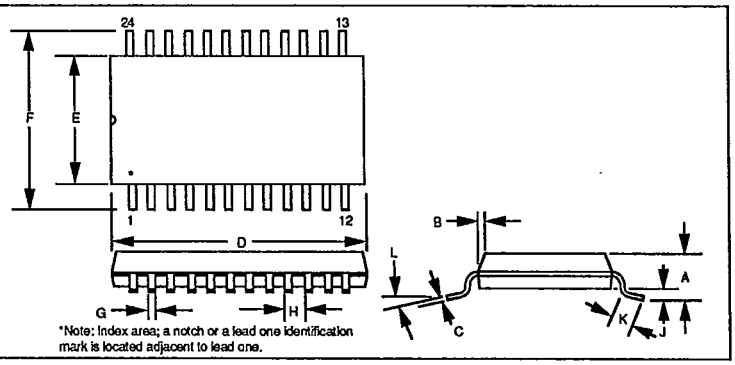
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.092	0.110	2.35	2.75
B	0.009	0.030	0.25	0.75
C	0.007	0.013	0.18	0.32
D	0.496	0.512	12.60	13.00
E	0.291	0.300	7.40	7.60
F	0.393	0.420	10.00	10.65
G	0.013	0.020	0.35	0.49
H	0.050 BSC		1.27 BSC	
J	0.003	0.012	0.10	0.30
K	0.015	0.050	0.40	1.27
L	0°	8°	0°	8°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

24 PIN SOIC

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.092	0.110	2.35	2.75
B	0.009	0.030	0.25	0.75
C	0.007	0.013	0.18	0.32
D	0.598	0.615	15.20	15.62
E	0.291	0.300	7.40	7.60
F	0.393	0.420	10.00	10.65
G	0.013	0.020	0.35	0.49
H	0.050 BSC		1.27 BSC	
J	0.003	0.012	0.10	0.30
K	0.015	0.050	0.40	1.27
L	0°	8°	0°	8°



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PACKAGING AND ORDERING