

MC54/74HCT643

Octal 3-State Inverting and Noninverting Bus Transceiver with LSTTL-Compatible Inputs
High-Performance Silicon-Gate CMOS

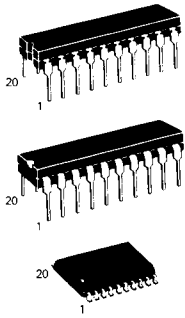
The MC54/74HCT643 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT643 is identical in pinout to the LS643.

The HCT643 is a 3-state transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

The HCT643 performs functions similar to those of the HCT245 and the HCT640.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 342 FETs or 85.5 Equivalent Gates



J SUFFIX CERAMIC CASE 732

N SUFFIX PLASTIC CASE 738

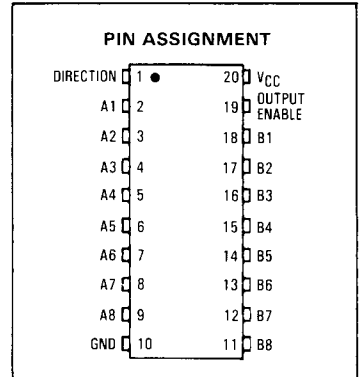
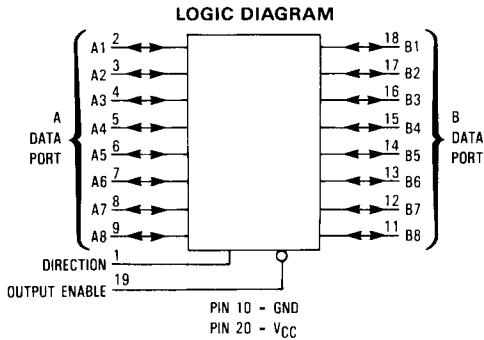
DW SUFFIX SOIC CASE 751D

ORDERING INFORMATION

MC74HCTXXXN	Plastic
MC54HCTXXXJ	Ceramic
MC74HCTXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

5



FUNCTION TABLE

Control Inputs		Operation
Output Enable	Direction	
L	L	Data transmitted from Bus B to Bus A (not inverted)
L	H	Data transmitted from Bus A to Bus B (inverted)
H	X	Buses Isolated (high-impedance state)

X = don't care

MC54/74HCT643

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND), Pin 1 or 19	-1.5 to V _{CC} +1.5	V
V _{I/O}	DC I/O Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{I/O}	DC I/O Current, per Pin	±35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA	4.5	3.98	3.84	3.70	V
			5.5	0.1	0.1	0.1	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND, Pin 1 or 19	4.5	0.1	0.1	0.1	μA
			5.5	0.1	0.1	0.1	
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND, I/O Pins	4.5	±0.1	±1.0	±1.0	μA
			5.5	±0.5	±5.0	±10.0	
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	5.5	8	80	160	μA

ΔI _{CC}	Additional Quiescent Supply Current	V _{in} = 2.4 V, Any One Input V _{in} = V _{CC} or GND, Other Inputs I _{out} = 0 μA	5.5	≥ -55°C	25°C to 125°C	mA
				2.9	2.4	

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- Total Supply Current = I_{CC} + ΣΔI_{CC}.

MC54/74HCT643

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{ pF}$, Input $t_r=t_f=6\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A to B or B to A (Figures 1 and 3)	22	28	33	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	30	38	45	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	30	38	45	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
C_{in}	Maximum Input Capacitance, Pin 1 or 19	10	10	10	pF
C_{out}	Maximum Three-State I/O Capacitance (Output in High-Impedance State)	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Transceiver Channel) Used to determine the no-load dynamic power consumption: $P_D = CPD V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC}=5.0\text{ V}$	pF
		45	

SWITCHING WAVEFORMS

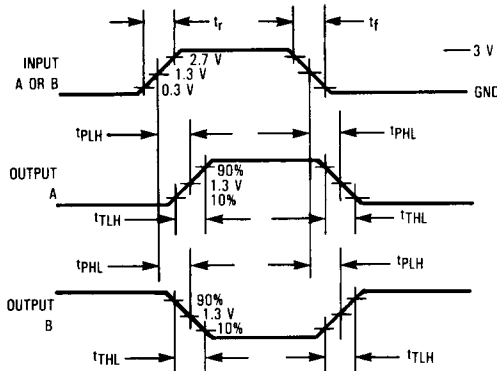


Figure 1

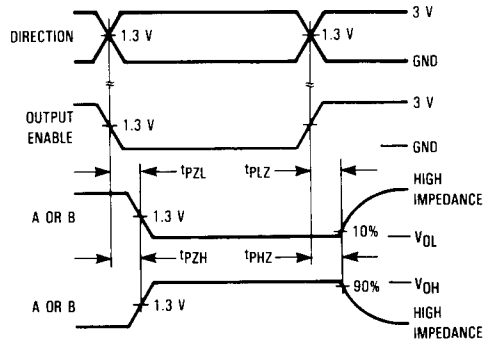
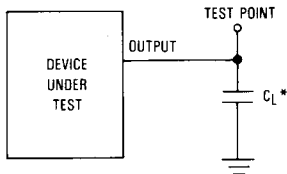
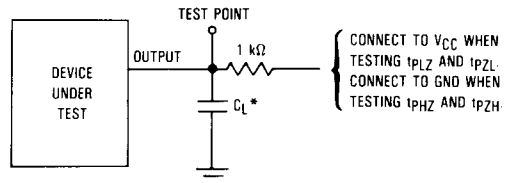


Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

MC54/74HCT643

EXPANDED LOGIC DIAGRAM

